

# TCAN1043N-Q1 Automotive CAN FD Transceiver With Sleep Mode

## 1 Features

- · AEC Q100 Qualified for automotive applications
- · Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Meets the requirements of ISO 11898-2:2024
- · Wide input operational voltage range
- Supports classic CAN and CAN FD up to 8 Mbps
- V<sub>IO</sub> level shifting supports: 1.7V to 5.5V
- Operating modes:
  - Normal mode
  - Silent mode
  - Standby mode
  - Low-power sleep mode
- · High-voltage INH output for system power control
- · Local wake-up support via the WAKE pin
- · Defined behavior when unpowered
  - Bus and IO terminals are high impedance (no load to operating bus or application)
- Protection features:
  - ±58V CAN bus fault tolerant
  - Load dump support on V<sub>SUP</sub>
  - IEC ESD protection
  - Under-voltage protection
  - Thermal shutdown protection
  - TXD dominant state timeout (TXD DTO)
- Available in 14-pin leaded (SOT and SOIC)
   packages and leadless (VSON) package with
   wettable flanks for improved automated optical
   inspection (AOI) capability

# 2 Applications

- Body electronics and lighting
- · Automotive gateway
- Advanced driver assistance systems (ADAS)
- Infotainment and cluster
- · Hybrid, electric & powertrain systems
- · Personal transport vehicles electric bike
- Industrial transportation

## 3 Description

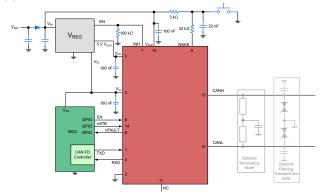
The TCAN1043N-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 high-speed CAN specification. The device supports both classical CAN and CAN FD data rates up to 8 megabits per second (Mbps).

The TCAN1043N-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system via the INH output pin. This allows a low-current sleep state in which power is gated to all system components except for the TCAN1043N-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN1043N-Q1 initiates system start-up by driving INH high.

## **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
	SOT (DYY) (3)	4.2mm x 3.26mm
TCAN1043N-Q1	SOIC (D) (3)	8.65mm x 6mm
	VSON (DMT)	4.5mm x 3mm

- (1) For more information, see Section 11.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) Product Preview



Simplified Schematic



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# **4 Pin Configuration and Functions**

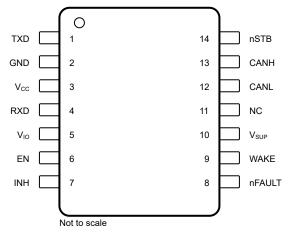


Figure 4-1. D and DYY Packages, 14 Pin (SOIC) and (SOT) (Top View)

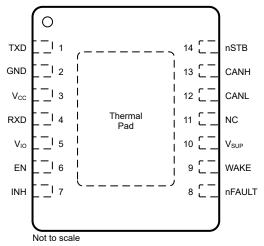


Figure 4-2. DMT Package, 14 Pin (VSON) (Top View)

PINS	3	<b>7.75</b> (1)	DECODINE CO.	
NAME	NO.	TYPE (1)	DESCRIPTION	
TXD	1	I	CAN transmit data input, integrated pull-up	
GND	2	GND	Ground connection	
V <sub>CC</sub>	3	Р	5 V transceiver supply	
RXD	4	0	CAN receive data output, tri-state when V <sub>IO</sub> < UV <sub>IO</sub>	
V <sub>IO</sub>	5	Р	I/O supply voltage	
EN	6	I	Enable input for mode control, integrated pull-down	
INH	7	0	Inhibit pin to control system voltage regulators and supplies, high-voltage	
nFAULT	8	0	Fault output, inverted logic	
WAKE	9	I	Local WAKE input terminal, high voltage	
V <sub>SUP</sub>	10	Р	High-voltage supply from battery	
NC	11	NC	No connect, internally not connected	
CANL	12	I/O	Low-level CAN bus input/output line	
CANH	13	I/O	High-level CAN bus input/output line	
nSTB	14	I	Standby mode control input, integrated pull-down	
Thermal Pad		<u> </u>	Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief	

(1) I = input, O = output, P = power, GND = ground, NC = not connected

# **5 Specifications**

# 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V <sub>SUP</sub>	Supply voltage <sup>(2)</sup>	-0.3	45	V
V <sub>CC</sub>	Supply voltage	-0.3	6	V
V <sub>IO</sub>	Supply voltage I/O level shifter	-0.3	6	V
V <sub>BUS</sub>	CAN bus I/O voltage (CANH, CANL)	-58	58	V
V <sub>DIFF</sub>	CAN bus differential voltage (V <sub>DIFF</sub> = V <sub>CANH</sub> - V <sub>CANL</sub> )	-58	58	V
V <sub>WAKE</sub>	WAKE input voltage	-45	45 and V <sub>I</sub> ≤ V <sub>SUP</sub> +0.3	V
V <sub>INH</sub>	INH pin voltage	-0.3	45 and V <sub>O</sub> ≤ V <sub>SUP</sub> +0.3	V
V <sub>LOGIC</sub>	Logic pin voltage	-0.3	6	V
I <sub>O(LOGIC)</sub>	Logic pin output current		8	mA
I <sub>O(INH)</sub>	Inhibit pin output current		6	mA
I <sub>O(WAKE)</sub>	WAKE pin output current		3	mA
TJ	Junction temperature	-40	165	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

<sup>(1)</sup> Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

# 5.2 ESD Ratings

				VALUE	UNIT
V <sub>ESD</sub> Electrostatic discharge	Human body model (HBM), per AEC	V <sub>SUP</sub> , CANH, CANL, and WAKE with respect to ground	± 8000	٧	
	Q100-002 <sup>(1)</sup>	All pins except $V_{\text{SUP}}$ , CANH, CANL, and WAKE	± 4000	V	
		Charged device model (CDM), per AEC Q100-011	All pins	± 750	V

<sup>(1)</sup> AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

# 5.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
V <sub>ESD</sub>	Electrostatic discharge	CANH, CANL, V <sub>SUP</sub> , and WAKE terminal to GND	Unpowered Contact Discharge per ISO 10605 (1)	± 8000	V
V <sub>ESD</sub>	Electrostatic discharge	CANH and CANL terminal to GND	SAE J2962-2 per ISO 10605 Powered Contact Discharge <sup>(2)</sup>	± 8000	V
V <sub>ESD</sub>	Electrostatic discharge	CANH and CANL terminal to GND	SAE J2962-2 per ISO 10605 Powered Air discharge <sup>(2)</sup>	± 15000	V
			Pulse 1	- 100	V
	Transient voltage per		Pulse 2	75	V
	ISO-7637-2 <sup>(1)</sup>		Pulse 3a	- 150	V
V <sub>TRAN</sub>	V <sub>TRAN</sub>		Pulse 3b	100	V
	Transient voltage per ISO-7637-3 <sup>(2)</sup>	CAN terminal to GND	Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	± 30	V

<sup>(1)</sup> Results given here are specific to the IEC 62228-3 Integrated circuits – EMC evaluation of transceivers – Part 3: CAN transceivers. Testing performed by IBEE Zwickau, EMC report available upon request.

<sup>(2)</sup> Able to support load dumps of up to 45 V for 300ms

(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM-approved independent 3<sup>rd</sup> party, EMC report available upon request.

## **5.4 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM I	IAX	UNIT
V <sub>SUP</sub>	Supply voltage	4.5		40	V
V <sub>IO</sub>	I/O supply voltage	1.7		5.5	V
V <sub>CC</sub>	CAN transceiver supply voltage	4.5		5.5	V
I <sub>OH(DO)</sub>	Digital output high-level current	-2			mA
I <sub>OL(DO)</sub>	Digital output low-level current			2	mA
I <sub>O(INH)</sub>	Inhibit output current			1	mA
TJ	Operating junction temperature	-40		150	°C
T <sub>SDR</sub>	Thermal shutdown	175			°C
T <sub>SDF</sub>	Thermal shutdown release	160			°C
T <sub>SD(HYS)</sub>	Thermal shutdown hysteresis		10		°C

## 5.5 Thermal Information

THERMAL METRIC (1)					
		D (SOIC)	DMT (VSON)	DYY (SOT)	UNIT
		14 PINS	14 PINS	14 PINS	
R <sub>⊙JA</sub>	Junction-to-ambient thermal resistance	87.1	39.7	91.0	°C/W
R <sub>OJC(top)</sub>	Junction-to-case (top) thermal resistance	41.8	41.1	41.7	°C/W
R <sub>⊙JB</sub>	Junction-to-board thermal resistance	43.7	15.9	25.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	8.5	0.9	25.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	43.3	15.9	1.1	°C/W
R <sub>OJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	6.6	N/A	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.6 Power Dissipation Ratings

	PARAMETER	TEST CONDITIONS	POWER DISSIPATION	UNIT
P <sub>D</sub> Average power dissipation	$\begin{array}{l} V_{SUP} = 14 \text{ V, } V_{CC} = 5 \text{ V, } V_{IO} = 5 \text{ V, } T_{J} = 27^{\circ}\text{C, } R_{L} = 60 \\ \Omega, \text{ nSTB} = 5 \text{ V, EN} = 5 \text{ V, } C_{L,RXD} = 15 \text{ pF. Typical CAN} \\ \text{operating conditions at } 500 \text{ kbps with } 25\% \text{ transmission} \\ \text{(dominant) rate.} \end{array}$	65	mW	
	Average power dissipation	$\begin{split} &V_{SUP} = 14 \text{ V, } V_{CC} = 5.5 \text{ V, } V_{IO} = 5.5 \text{ V, } T_J = 150^{\circ}\text{C, } R_L = \\ &50  \Omega, \text{ nSTB} = 5.5 \text{ V, } EN = 5.5 \text{ V, } C_{L,RXD} = 15 \text{ pF. Typical} \\ &\text{high load CAN operating conditions at 1 Mbps with 50\%} \\ &\text{transmission (dominant) rate and loaded network.} \end{split}$	140	mW

## 5.7 Power Supply Characteristics

Over recommended operating conditions with  $T_J$  = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C,  $V_{SUP}$  = 12 V,  $V_{IO}$  = 3.3 V,  $V_{CC}$  = 5 V and  $R_L$  = 60  $\Omega$ 

23 0, VSUP - 12 V, VIO - 3.5 V, VCC - 3 V and TL - 30 12							
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Supply Voltage and Current Characteristics							
I <sub>SUP_NORMAL</sub>	Supply current CAN active	Normal mode, silent mode, and go-to-sleep mode			140	μΑ	
I <sub>SUP_STBY-85C</sub>	Supply current, Standby mode CAN autonomous: inactive (2)	$V_{SUP}$ = 12V, $T_{J}$ = -40 °C to 85 °C <sup>(3)</sup>		27	33	μΑ	
I <sub>SUP_STBY</sub>	Supply current, Standby mode CAN autonomous: inactive (2)				60	μA	

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## 5.7 Power Supply Characteristics (continued)

Over recommended operating conditions with  $T_J$  = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C,  $V_{SUP}$  = 12 V,  $V_{IO}$  = 3.3 V,  $V_{CC}$  = 5 V and  $R_L$  = 60  $\Omega$ 

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>SUP_SLEEP-85C</sub>	Supply current, Sleep mode CAN autonomous: inactive (2)	T <sub>J</sub> = -40 °C to 85 °C V <sub>SUP</sub> = 12V <sup>(3)</sup>		23	26	μA
I <sub>SUP_SLEEP</sub>	Supply current, Sleep mode CAN autonomous: inactive (2)			23	30	μA
I <sub>SUP_BIAS</sub>	Additional supply current when in CAN autonomous: active (I <sub>SUP(BIAS)</sub> )	5.5 V < V <sub>SUP</sub> ≤ 28 V <sup>(1)</sup>			60	μA
UV <sub>SUP(R)</sub>	Undervoltage V <sub>SUP</sub> threshold rising		3.85		4.4	٧
UV <sub>SUP(F)</sub>	Undervoltage V <sub>SUP</sub> threshold falling		3.5		4.25	٧
	Supply current CAN active: dominant	Normal mode $TXD = 0 \text{ V, } R_L = 60  \Omega,  C_L = \text{open}$ Normal mode			60	mA
		TXD = 0 V, $R_L$ = 50 $\Omega$ , $C_L$ = open			70	mA
I <sub>CC_NORMAL</sub>	V <sub>CC</sub> supply current normal mode Dominant with bus fault	Normal mode TXD = 0 V, R <sub>L</sub> = open, C <sub>L</sub> = open, CANH = -25 V			110	mA
	Supply current CAN active: recessive	Normal mode TXD = $V_{IO}$ , $R_L$ = 50 $\Omega$ , $C_L$ = open			5	mA
1	Supply current, Standby mode CAN autonomous: inactive	$T_J = -40$ °C to 85 °C <sup>(3)</sup> EN = nSTB = 0 V			2	μА
Ісс_ѕтву		Standby mode EN = nSTB = 0 V			5	μΑ
I <sub>CC_SILENT</sub>	Supply current, Silent and go-to-sleep mode	Silent and go-to-sleep mode TXD = nSTB = $V_{IO}$ , $R_L$ = 50 $\Omega$ , $C_L$ = open			3	mA
I	Supply current, Sleep mode CAN autonomous: inactive	Sleep mode $T_J$ = -40 °C to 85 °C (3) EN = 0 V or $V_{IO}$ , nSTB = 0 V			2	μА
ICC_SLEEP		Sleep mode EN = 0 V or V <sub>IO</sub> , nSTB = 0 V			5	μΑ
UV <sub>CC(R)</sub>	Undervoltage V <sub>CC</sub> threshold rising			4.1	4.4	V
UV <sub>CC(F)</sub>	Undervoltage V <sub>CC</sub> threshold falling		3.5	3.9		V
V <sub>HYS(UVCC)</sub>	Hysteresis voltage on UV <sub>CC</sub>		50	240	320	mV
	I/O supply current	Normal mode RXD floating, TXD = 0 V			200	μΑ
I <sub>IO_NORMAL</sub>	I/O supply current	Normal mode, standby mode, or go-to-sleep mode RXD floating, TXD = V <sub>IO</sub>			5	μА
h	I/O supply current	Sleep mode T <sub>J</sub> = -40 °C to 85 °C <sup>(3)</sup> nSTB = 0 V			2.5	μΑ
I <sub>IO_SLEEP</sub>	I/O supply current	Sleep mode nSTB = 0 V			5	μΑ
UV <sub>IO(R)</sub>	Under voltage V <sub>IO</sub> threshold rising	Ramp up		1.4	1.65	V
UV <sub>IO(F)</sub>	Under voltage V <sub>IO</sub> threshold falling	Ramp down	1	1.25		V
V <sub>HYS(UVIO)</sub>	Hysteresis voltage on UV <sub>IO</sub>		30	60	160	mV

<sup>(1)</sup> I<sub>SUP(BIAS)</sub> is calculated by subtracting the supply current in CAN autonomous inactive mode from the total supply current in CAN autonomous active mode

<sup>(2)</sup> After a valid wake-up, the CAN transceiver switches to CAN autonomous active mode and the I<sub>SUP(BIAS)</sub> current needs to be added to the specified I<sub>SUP</sub> current in CAN autonomous inactive mode.

<sup>(3)</sup> Specified by design and verified via bench characterization



# 5.8 Electrical Characteristics

Over recommended operating conditions with  $T_J$  = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C,  $V_{SLIP}$  = 12 V,  $V_{IO}$  = 3.3 V,  $V_{CC}$  = 5 V and  $R_I$  = 60  $\Omega$ 

, V SUP	= 12 V, V <sub>IO</sub> = 3.3 V, V	CC C V dild [1]		BAILI	TVD MAY	HAUT
	PARAMETER		TEST CONDITIONS	MIN	TYP MAX	UNIT
CAN Driver (	Characteristics	Т				
V	Dominant output voltage	CANH	$ TXD = 0 \text{ V}, 50 \le R_L \le 65 \Omega, C_L = \text{open}, R_{CM} =  $	2.75	4.5	V
V <sub>CANH(D)</sub>	Bus biasing active	CANL	See Figure 6-1 and Figure 6-4	0.5	2.25	V
V <sub>CANH(R)</sub> V <sub>CANL(R)</sub>	Recessive output voltage Bus biasing active, terminated	Recessive output voltage Bus biasing active, terminated	TXD = $V_{IO}$ , $R_L$ = 60 $\Omega$ , $R_{CM}$ = open See Figure 6-1 and Figure 6-4	2.137	2.887	V
V <sub>CANH(R)</sub> V <sub>CANL(R)</sub>	Recessive output voltage Bus biasing active		TXD = V <sub>IO</sub> , R <sub>L</sub> = open (no load), R <sub>CM</sub> = open See Figure 6-1 and Figure 6-4	2	3	V
$V_{SYM}$	Driver symmetry Bus biasing active (V <sub>O(CANH)</sub> + V <sub>O(CANL)</sub> ) / V <sub>CC</sub>	:	nSTB= $V_{IO}$ , $R_L$ = 60 $\Omega$ , $C_{SPLIT}$ = 4.7 nF, $C_L$ = Open, $R_{CM}$ = Open, TXD = 250 kHz, 1 MHz, 2.5 MHz See Figure 6-1 and Figure 6-4	0.9	1.1	V/V
V <sub>SYM_DC</sub>	DC Driver symmetry Bus biasing active $V_{CC} - V_{O(CANH)} - V_{O(CANL)}$		nSTB= $V_{IO}$ , $R_L$ = 60 $\Omega$ , $C_L$ = open See Figure 6-1 and Figure 6-4	-400	400	mV
V <sub>DIFF(D)</sub>		CANH - CANL	nSTB = V <sub>IO</sub> , TXD = 0 V, 50 $\Omega$ ≤ R <sub>L</sub> ≤ 65 $\Omega$ , C <sub>L</sub> = open See Figure 6-1 and Figure 6-4	1.5	3	٧
	Differential output voltage Bus biasing active Dominant	CANH - CANL	nSTB = V <sub>IO</sub> , TXD = 0 V, 45 $\Omega$ ≤ R <sub>L</sub> ≤ 70 $\Omega$ , CL = open See Figure 6-1 and Figure 6-4	1.4	3.3	٧
		CANH - CANL	nSTB = $V_{IO}$ , TXD = 0 V, $R_L$ = 2240 $\Omega$ , $C_L$ = open See Figure 6-1 and Figure 6-4	1.5	5	٧
$V_{DIFF(R)}$	Differential output voltage Bus biasing active Recessive	CANH - CANL	nSTB = $V_{IO}$ , TXD = $V_{IO}$ , $R_L$ = open $\Omega$ , $C_L$ = open See Figure 6-1 and Figure 6-4	-50	50	mV
	Bus output voltage with bus biasing inactive	CANH	nSTB = 0 V, TXD = V <sub>IO</sub> , R <sub>L</sub> = open (no load), C <sub>L</sub> = open See Figure 6-1 and Figure 6-4	-0.1	0.1	V
V <sub>CANH(INACT)</sub>		CANL	nSTB = 0 V, TXD = V <sub>IO</sub> , R <sub>L</sub> = open (no load), C <sub>L</sub> = open See Figure 6-1 and Figure 6-4	-0.1	0.1	V
		CANH - CANL	nSTB = 0 V, TXD = V <sub>IO</sub> , R <sub>L</sub> = open (no load), C <sub>L</sub> = open See Figure 6-1 and Figure 6-4	-0.2	0.2	V
I	Short-circuit steady-state ou Bus biasing active	utput current	nSTB = $V_{IO}$ , TXD = 0 V -15 V $\leq$ $V_{(CANH)} \leq$ 40 V See Figure 6-1 and Figure 6-8	-100		mA
I <sub>CANL(OS)</sub>	Dominant		nSTB = $V_{IO}$ , TXD = 0 V -15 V $\leq$ $V_{(CANL)} \leq$ 40 V See Figure 6-1 and Figure 6-8		100	mA
I <sub>OS(REC)</sub>	Short-circuit steady-state output current Bus biasing active Recessive		$\begin{split} \text{nSTB} = \text{V}_{\text{IO}}, \text{V}_{\text{BUS}} = \text{CANH} = \text{CANL} \\ -27 \text{ V} \leq \text{V}_{\text{BUS}} \leq 42 \text{ V} \\ \text{See Figure 6-1}  \text{and Figure 6-8} \end{split}$	-3	3	mA
CAN Receive	er Characteristics					
V <sub>IT(DOM)</sub>	Receiver dominant state inp Bus biasing active	out voltage range	nSTB = V <sub>IO</sub> , -12 V ≤ V <sub>CM</sub> ≤ 12 V	0.9	8	٧
V <sub>IT(REC)</sub>	Receiver recessive state input voltage range Bus biasing active		See Figure 6-5 and Table 7-6	-3	0.5	V
V <sub>HYS</sub>	Hysteresis voltage for input Bus biasing active	threshold	nSTB = V <sub>IO</sub> See Figure 6-5 and Table 7-6		140	mV
V <sub>DIFF(DOM)</sub>	Receiver dominant state inp Bus biasing inactive	out voltage range	nSTB = 0 V, -12 V ≤ V <sub>CM</sub> ≤ 12 V	1.150	8	V
V <sub>DIFF(REC)</sub>	Receiver recessive state inp Bus biasing inactive	out voltage range	See Figure 6-5 and Table 7-6	-3	0.4	V



# **5.8 Electrical Characteristics (continued)**

Over recommended operating conditions with  $T_J$  = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C,  $V_{SUP}$  = 12 V,  $V_{IO}$  = 3.3 V,  $V_{CC}$  = 5 V and  $R_I$  = 60  $\Omega$ 

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CM</sub>			nSTB = V <sub>IO</sub> See Figure 6-5 and Table 7-6	-12		12	V
I <sub>OFF(LKG)</sub>	Power-off (unpowered) input leakage current CANH, CANL pins		V <sub>SUP</sub> = 0 V, CANH = CANL = 5 V			4.5	μA
Cı	Input capacitance to ground	(CANH or CANL)				20	pF
C <sub>ID</sub>	Differential input capacitanc	e <sup>(1)</sup>				10	pF
R <sub>ID</sub>	Differential input resistance		TXD = V <sub>CC</sub> = V <sub>IO</sub> = 5 V, nSTB = 5 V	50		100	kΩ
R <sub>IN</sub>	Input resistance (CANH or C	CANL)	-12 V ≤ V <sub>CM</sub> ≤ 12 V	25		50	kΩ
R <sub>IN(M)</sub>	Input resistance matching: [1 - R <sub>IN(CANH)</sub> / R <sub>IN(CANL)</sub> ] ×	100%	V <sub>(CANH)</sub> = V <sub>(CANL)</sub> = 5 V	-1		1	%
R <sub>CBF</sub>	Valid differential load impedation fault circuitry	ance range for bus	R <sub>CM</sub> = R <sub>L</sub> , C <sub>L</sub> = open	45		70	Ω
TXD Chara	cteristics					'	
V <sub>IH</sub>	High-level input voltage			0.7			V <sub>IO</sub>
V <sub>IL</sub>	Low-level input voltage					0.3	V <sub>IO</sub>
I <sub>IH</sub>	High-level input leakage cur	rent	TXD = V <sub>IO</sub> = 5.5 V	-2.5	0	1	μA
I <sub>IL</sub>	Low-level input leakage curr	ent	TXD = 0 V, V <sub>IO</sub> = 5.5 V	-137		-2.5	μA
I <sub>LKG(OFF)</sub>	Unpowered leakage current		TXD = 5.5 V, V <sub>SUP</sub> = V <sub>IO</sub> = 0 V	-1	0	1	μA
R <sub>PU</sub>	Pull-up resistance to V <sub>IO</sub>			40	60	80	kΩ
Cı	Input Capacitance		$V_{IN} = 0.4 \times \sin(2 \times \pi \times 2 \times 10^6 \times t) + 2.5 \text{ V}$		5		pF
RXD Chara	cteristics						
V <sub>OH</sub>	High-level output voltage	High-level output voltage	I <sub>O</sub> = - 1.5mA, V <sub>IO</sub> =1.7V See Figure 6-5	0.8			V <sub>IO</sub>
V <sub>OH</sub>	High-level output voltage		$I_O = -2$ mA, $V_{IO} >= 2.5$ V See Figure 6-5	0.8			V <sub>IO</sub>
V <sub>OL</sub>	Low-level output voltage		I <sub>O</sub> = 2 mA See Figure 6-5			0.2	$V_{\text{IO}}$
I <sub>LKG(OFF)</sub>	Unpowered leakage current		RXD = 5.5 V, V <sub>SUP</sub> = V <sub>IO</sub> = 0 V	-1		1	μΑ
nSTB Char	acteristics						
V <sub>IH</sub>	High-level input voltage			0.7			V <sub>IO</sub>
V <sub>IL</sub>	Low-level input voltage					0.3	V <sub>IO</sub>
I <sub>IH</sub>	High-level input leakage cur	rent	nSTB = V <sub>IO</sub> = 5.5 V	0.5		137	μΑ
I <sub>IL</sub>	Low-level input leakage curr	ent	nSTB = 0 V, V <sub>IO</sub> = 5.5 V	-1		1	μΑ
I <sub>LKG(OFF)</sub>	Unpowered leakage current		nSTB = 5.5 V, V <sub>IO</sub> = 0 V	-1	0	1	μΑ
R <sub>PD</sub>	Pull-down resistance			40	60	80	kΩ
nFAULT Ch	aracteristics				,	I	
V <sub>OH</sub>	High-level output voltage		I <sub>O</sub> = -2 mA	0.8			V <sub>IO</sub>
V <sub>OL</sub>	Low-level output voltage		I <sub>O</sub> = 2 mA			0.2	V <sub>IO</sub>
I <sub>LKG(OFF)</sub>	Unpowered leakage current		nFAULT = 5.5 V, V <sub>IO</sub> = 0 V	-1	0	1	μA
EN Charac	teristics						
V <sub>IH</sub>	High-level input voltage			0.7			V <sub>IO</sub>
V <sub>IL</sub>	Low-level input voltage					0.3	V <sub>IO</sub>
I <sub>IH</sub>	High-level input leakage current		EN = V <sub>CC</sub> = V <sub>IO</sub> = 5.5 V	0.5		137	μA
I <sub>IL</sub>	Low-level input leakage current		EN = 0 V, V <sub>CC</sub> = V <sub>IO</sub> = 5.5 V	-1		1	μA
I <sub>LKG(OFF)</sub>	Unpowered leakage current		EN = 5.5 V, V <sub>CC</sub> = V <sub>IO</sub> = 0 V	-1		1	<u>.</u> μΑ
R <sub>PD</sub>	Pull-down resistance			40	60	80	kΩ
	racteristics						

## 5.8 Electrical Characteristics (continued)

Over recommended operating conditions with  $T_J$  =  $-40^{\circ}$ C to 150°C, unless otherwise noted. All typical values are taken at 25°C,  $V_{SUP}$  = 12 V,  $V_{IO}$  = 3.3 V,  $V_{CC}$  = 5 V and  $R_L$  = 60  $\Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>IH</sub>	High-level input voltage	Sleep mode	V <sub>SUP</sub> - 2			V	
V <sub>IL</sub>	Low-level input voltage	Sieep mode		V	<sub>SUP</sub> - 3.5	V	
I <sub>IH</sub>	High-level input leakage current (2)	WAKE = V <sub>SUP</sub> – 1 V	-3			μA	
I <sub>IL</sub>	Low-level input leakage current (2)	WAKE = 1 V			3	μA	
INH Chara	INH Characteristics						
ΔV <sub>H</sub>	High-level voltage drop from VSUP to INH (V <sub>SUP -</sub> V <sub>INH)</sub>	I <sub>INH</sub> = -6 mA		0.5	1	V	
I <sub>LKG(INH)</sub>	Sleep mode leakage current	INH = 0 V	-0.5		0.5	μA	
R <sub>PD</sub>	Pull-down resistance	Sleep mode	2.5	4	6	МΩ	

<sup>(1)</sup> Specified by design and verified via bench characterization

## 5.9 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Charac	teristics						
t <sub>PWRUP</sub>	Time required for INH active after V <sub>SUP</sub> ≥ UV <sub>SUP(R)</sub>		See Figure 6-10		500		μs
t <sub>UV</sub>	Undervoltage filt	er time V <sub>CC</sub> and V <sub>IO</sub> <sup>(1)</sup>	V <sub>CC</sub> ≤ UV <sub>CC</sub> or V <sub>IO</sub> ≤ UV <sub>IO</sub>	100		350	ms
t <sub>UV(RE-ENABLE)</sub>	Re-enable time	after undervoltage event (1)	Time for device to return to normal operation from a UV <sub>CC</sub> or UV <sub>IO</sub> undervoltage event			200	μs
Device Charac	teristics						
t <sub>PROP(LOOP1)</sub>		driver input (TXD) to receiver ecessive to dominant	$R_L$ = 60 $\Omega$ , $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF See Figure 6-6		115	215	ns
t <sub>PROP(LOOP2)</sub>		driver input (TXD) to receiver ominant to recessive	$R_L$ = 60 $\Omega$ , $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF See Figure 6-6		115	205	ns
t <sub>WK(TIMEOUT)</sub>	Bus wake-up tim	neout value (1)		0.8		2	ms
t <sub>WK(FILTER)</sub>	Bus time to meet filtered bus requirements for wake-up request (1)			0.5		1.8	μs
t <sub>SILENCE</sub>	Timeout for bus inactivity (1)		Timer is reset and restarted, when bus changes from dominant to recessive or vice versa	0.6		1.2	s
t <sub>BIAS</sub>	Bus bias reaction time (1)	Measured from the start of a dominant-recessive-dominant sequence (each phase 6 $\mu$ s) until $V_{SYM} \ge 0.1$	nSTB = EN = 0 V, $R_L$ = 60 $\Omega$ , $C_{SPLIT}$ = 4.7 nF See Figure 6-9			200	μs
t <sub>CBF</sub>	Bus fault-detecti	on time	$45 \le R_{CM} \le 70 \Omega$ C <sub>L</sub> = open	2.5			μs
t <sub>WAKE_HT</sub>	Hold time for wh recognize LWU.	ich WAKE pin voltage should be sta	able after the rising or falling edge on WAKE pin to	5		50	μs
Mode Change	Characteristics						
t <sub>INH_SLP_STB</sub>	Time after WUP	or LWU event until INH asserted (1	)			100	μs
t <sub>MODE1</sub>		ne from leaving the Sleep mode to or Silent mode (1)	Time measured from VCC and VIO crossing UV thresholds to entering normal or silent mode.			20	μs
t <sub>MODE2</sub>		ne between normal, silent and nd from sleep to standby mode (1)	Mode change time between normal, silent and standby mode and from sleep to standby mode			10	μs
t <sub>GOTOSLEEP</sub>	Minimum hold tir	me for transition to sleep mode <sup>(1)</sup>	EN = H and nSTB = L	20		50	μs

(1) Specified by design and verified via bench characterization

<sup>(2)</sup> To minimize system level current consumption, the WAKE pin will automatically configure itself based on the applied voltage to either an internal pull-up or pull-down current source. A high-level input results in an internal pull-up and a low-level input results in an internal pull-down.



# **5.10 Switching Characteristics**

Over recommended operating conditions with  $T_J$  = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C,  $V_{SUP}$  = 12 V,  $V_{IO}$  = 3.3 V,  $V_{CC}$  = 5 V and  $R_L$  = 60  $\Omega$ 

201	= 12 V, V <sub>IO</sub> = 3.	RAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Chara				1201 001121110110				• • • • • • • • • • • • • • • • • • • •
	Propagation delay	time high TXD to						
t <sub>prop(TxD-</sub> busrec)	driver recessive				25	50	90	ns
t <sub>prop(TxD-</sub> busdom)	Propagation delay driver dominant	tin		$R_L = 60 \Omega, C_L = 100 pF, R_{CM} = open$	25	50	90	ns
t <sub>sk(p)</sub>	Pulse skew ( t <sub>pHR</sub> -	$t_{pLD} )$	driver recessive	See Figure 6-4		4		ns
t <sub>R</sub>	Differential output s	signal rise time				40		ns
t <sub>F</sub>	Differential output s	signal fall time				40		ns
t <sub>TXDDTO</sub>	Dominant timeout			TXD = 0 V, $R_L$ = 60 $\Omega$ , $C_L$ = open See Figure 6-7	1.2		3.8	ms
Receiver Ch	aracteristics							
t <sub>prop(busrec-</sub>	Propagation delay	time, bus recessive	input to high RXD		25	75	140	ns
t <sub>prop(busdom-</sub>	Propagation delay output	time, bus dominant i	nput to RXD low	C <sub>L(RXD)</sub> = 15 pF See Figure 6-5	20	75	130	ns
t <sub>R</sub>	Output signal rise ti	ime (RXD)		Soot igate o-o		4		ns
t <sub>F</sub>	Output signal fall tir			†		4		ns
t <sub>BUSDOM</sub>	Dominant time out	<u></u>		R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open See Figure 6-5			3.8	ms
CAN FD Cha	racteristics							
t <sub>ΔBIT(BUS)</sub> <sup>(1)</sup>	Transmitted recessive bit width variation on CAN bus output pins with t <sub>BIT(TXD)</sub> = 500 ns	Transmitted recessive bit width variation on CAN bus output pins with t <sub>BIT(TXD)</sub> = 500 ns		$R_L$ = 60 Ω, $C_{L1}$ = open, $C_{L2}$ = 100 pF, $C_{L(RXD)}$ = 15 pF $t_{\Delta Bit(BUS)}$ = $t_{BIT(BUS)}$ - $t_{BIT(TXD)}$ See Figure 6-6	-50		25	ns
t <sub>ΔΒΙΤ(BUS)</sub> <sup>(1)</sup>	Transmitted recessive bit width variation on CAN bus output pins with t <sub>BIT(TXD)</sub> = 200 ns	Transmitted recessive bit width variation on CAN bus output pins with t <sub>BIT(TXD)</sub> = 200 ns		$\begin{aligned} & R_{L} = 60 \ \Omega, \ C_{L1} = \text{open}, \ C_{L2} = 100 \ \text{pF}, \\ & C_{L(RXD)} = 15 \ \text{pF} \\ & t_{\Delta Bit(BUS)} = t_{BIT(BUS)} \cdot t_{BIT(TXD)} \\ & \text{See Figure 6-6} \end{aligned}$	-40		10	ns
t <sub>ΔΒΙΤ(BUS)</sub> <sup>(1)</sup>	Transmitted recessive bit width variation on CAN bus output pins with t <sub>BIT(TXD)</sub> = 125 ns	Transmitted recessive bit width variation on CAN bus output pins with t <sub>BIT(TXD)</sub> = 125 ns		$R_L$ = 60 Ω, $C_{L1}$ = open, $C_{L2}$ = 100 pF, $C_{L(RXD)}$ = 15 pF $t_{\Delta Bit(BUS)}$ = $t_{BIT(BUS)}$ - $t_{BIT(TXD)}$ See Figure 6-6	-45		10	ns
t <sub>ΔΒΙΤ(RXD)</sub> <sup>(1)</sup>	Received recessive bit width variation on RXD output pins with t <sub>BIT(TXD)</sub> = 500 ns	Received recessive bit width variation on RXD output pins with t <sub>BIT(TXD)</sub> = 500 ns		$R_L$ = 60 $\Omega$ , $C_{L1}$ = open, $C_{L2}$ = 100 pF, $C_{L(RXD)}$ = 15 pF $t_{\Delta Bit(RXD)}$ = $t_{BIT(RXD)}$ - $t_{BIT(TXD)}$ See Figure 6-6	-90		40	ns
t <sub>ΔΒΙΤ(RXD)</sub> <sup>(1)</sup>	Received recessive bit width variation on RXD output pins with $t_{BIT(TXD)} = 200 \text{ ns}$	Received recessive bit width variation on RXD output pins with t <sub>BIT(TXD)</sub> = 200 ns		$R_L$ = 60 Ω, $C_{L1}$ = open, $C_{L2}$ = 100 pF, $C_{L(RXD)}$ = 15 pF $t_{\Delta Bit(RXD)}$ = $t_{BIT(RXD)}$ - $t_{BIT(TXD)}$ See Figure 6-6	-70		20	ns
t <sub>ΔBIT(RXD)</sub> <sup>(1)</sup>	Received recessive bit width variation on RXD output pins with $t_{BIT(TXD)}$ =125 ns	Received recessive bit width variation on RXD output pins with $t_{BIT(TXD)} = 125 \text{ ns}$		$\begin{aligned} &R_{L} = 60 \ \Omega, \ C_{L1} = \text{open}, \ C_{L2} = 100 \ \text{pF}, \\ &C_{L(RXD)} = 15 \ \text{pF} \\ &t_{\Delta Bit(RXD)} = t_{BIT(RXD)} \cdot t_{BIT(TXD)} \\ &\text{See Figure 6-6} \end{aligned}$	-65		20	ns

# **5.10 Switching Characteristics (continued)**

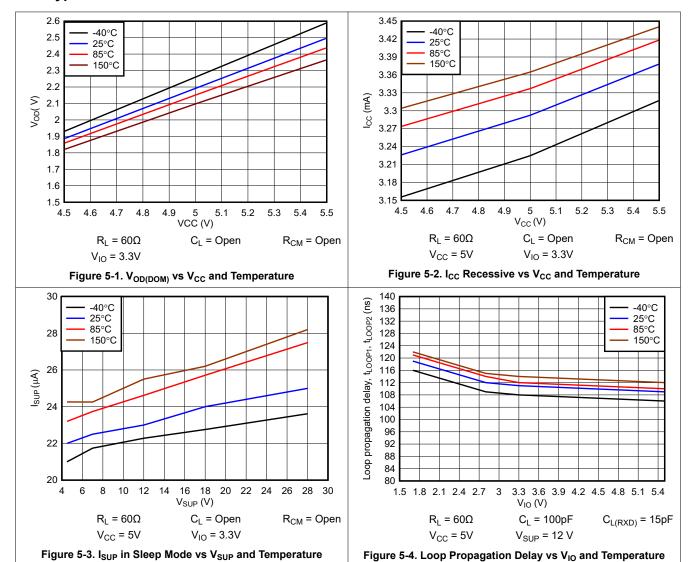
Over recommended operating conditions with  $T_J$  = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C,  $V_{SUP}$  = 12 V,  $V_{IO}$  = 3.3 V,  $V_{CC}$  = 5 V and  $R_L$  = 60  $\Omega$ 

	PARAMETER	TEST CONDITIONS	MIN	TYP N	IAX	UNIT
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	$\begin{array}{c} R_L = 60~\Omega,~C_{L1} = \text{open},~C_{L2} = 100~\text{p} \\ C_{L(RXD)} = 15~\text{pF} \\ \Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)} \\ \text{See Figure 6-6} \end{array}$	F, _50		20	ns
$t_{\Delta REC}$ (1) Receiver timing symmetry with $t_{BIT(TXD)} = 200 \text{ ns}$			F,45		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)} = 125 \text{ ns}^{(2)}$	R <sub>L</sub> = 60 $\Omega$ , C <sub>L1</sub> = open, C <sub>L2</sub> = 100 p C <sub>L(RXD)</sub> = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Figure 6-6	$R_L = 60 \Omega$ , $C_{L1} = \text{open}$ , $C_{L2} = 100 \text{ pF}$ , $C_{L(RXD)} = 15 \text{ pF}$ $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ $-25$		10	ns

- (1) The input signal on TXD shall have rise times and fall times (10% to 90%) of less than 10 ns
- (2) Specified by design and verified via bench characterization



## 5.11 Typical Characteristics





# **6 Parameter Measurement Information**

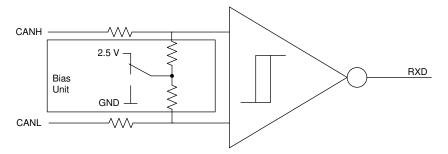


Figure 6-1. Common-Mode Bias Unit and Receiver

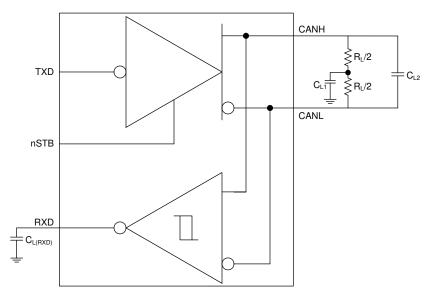


Figure 6-2. Test Circuit

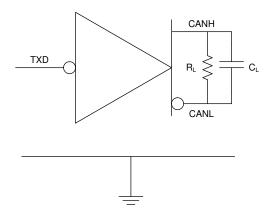


Figure 6-3. Supply Test Circuit



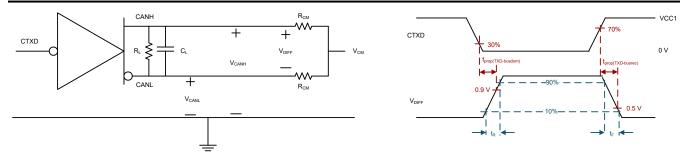


Figure 6-4. Driver Test Circuit and Measurement

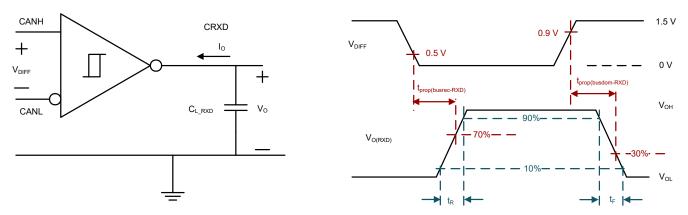


Figure 6-5. Receiver Test Circuit and Measurement

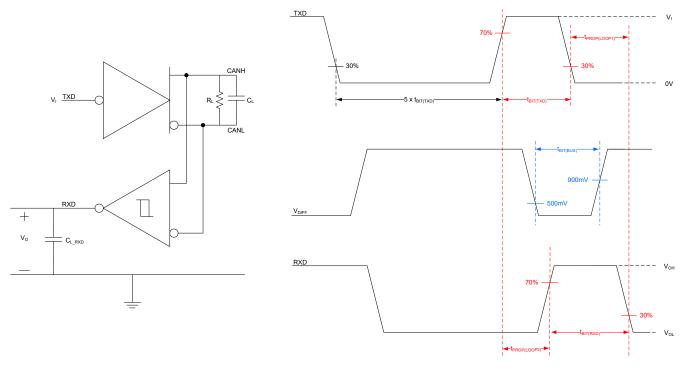


Figure 6-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

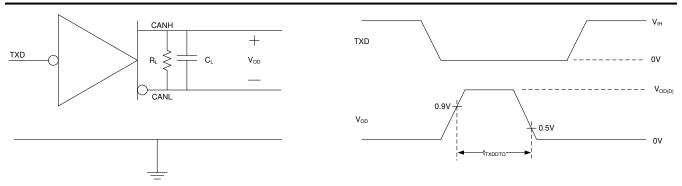


Figure 6-7. TXD Dominant Time Out Test Circuit and Measurement

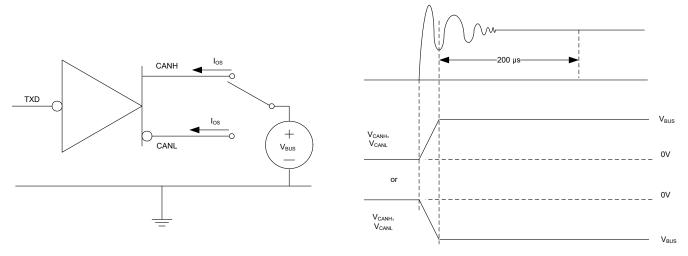


Figure 6-8. Driver Short-Circuit Current Test and Measurement

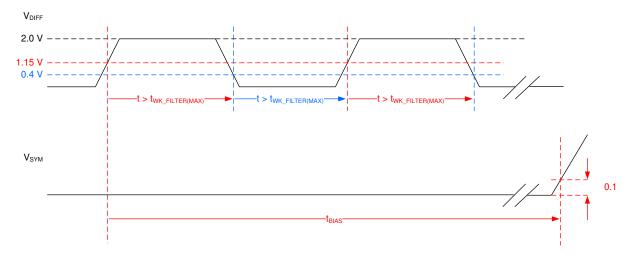


Figure 6-9. Bias Reaction Time Measurement



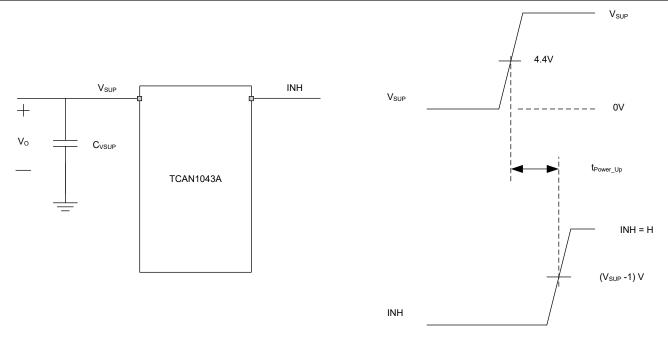


Figure 6-10. Power-Up Timing

# 7 Detailed Description

## 7.1 Overview

The transceiver has three separate supply inputs,  $V_{SUP}$ ,  $V_{CC}$ , and  $V_{IO}$ . By using  $V_{IO}$ , the TCAN1043N-Q1 can interface directly to a 1.8V, 2.5V, 3.3V, or 5V controller without the need for a level shifter. The TCAN1043N-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present in the system via the INH output pin. This enables a low-current sleep state in which power is gated to all system components except for the TCAN1043N-Q1, which remains in a low-power state while monitoring the CAN bus. When a wake-up pattern is detected on the bus or when a local wake up is requested via the WAKE input, the device initiates node start-up by driving INH high.

The TCAN1043N-Q1 includes many protection and diagnostic features including undervoltage detection, CAN bus fault detection, battery connection detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and bus fault protection up to ±58V.

## 7.2 Functional Block Diagram

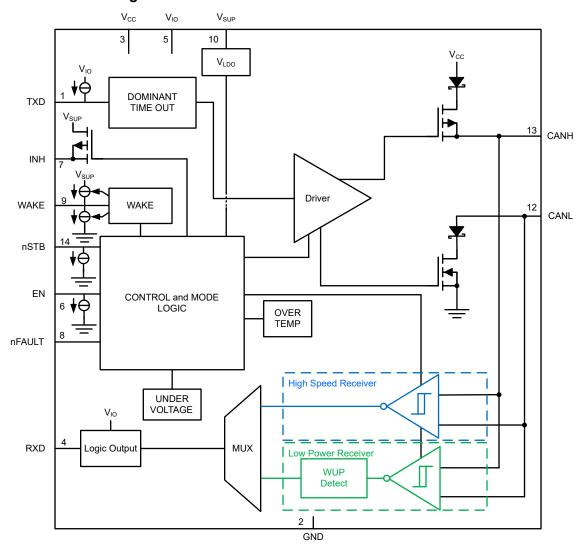


Figure 7-1. TCAN1043N-Q1 Functional Block Diagram

## 7.3 Feature Description

## 7.3.1 Supply Pins

The TCAN1043N-Q1 implements three independent supply inputs for regulating different portions of the device.

### 7.3.1.1 V<sub>SUP</sub> Pin

This pin is connected to the battery supply. The pin provides the supply to the internal regulators that support the digital core and the low power CAN receiver.

#### 7.3.1.2 V<sub>CC</sub> Pin

This pin provides the 5V supply voltage for the CAN transceiver.

#### 7.3.1.3 V<sub>IO</sub> Pin

This pin provides the digital I/O voltage to match the CAN FD controller I/O voltage. It supports I/O voltages from 1.7V to 5.5V providing a wide range of controller support.

## 7.3.2 Digital Inputs and Outputs

#### 7.3.2.1 TXD Pin

TXD is a logic-level input signal, referenced to  $V_{IO}$ , from a CAN FD controller to the TCAN1043N-Q1. TXD is biased to the V<sub>IO</sub> level to force a recessive input in case the pin floats.

#### 7.3.2.2 RXD Pin

RXD is a logic-level signal output, referenced to V<sub>IO</sub>, from the TCAN1043N-Q1 to a CAN FD controller. The RXD pin is driven to the  $V_{IO}$  level as logic-high outputs once a valid  $V_{IO}$  is present.

When a power-on or wake-up event takes place, the RXD pin is pulled low.

#### 7.3.2.3 nFAULT Pin

nFAULT is a logic-level output signal, referenced to V<sub>IO</sub>, from the TCAN1043N-Q1 to a CAN FD controller. The nFAULT output is driven to the V<sub>IO</sub> level as logic-high output.

The nFAULT output is used to transmit the TCAN1043N-Q1 status indicator flags to the CAN FD controller. Please see Table 7-1 for the specific fault scenarios that are indicated externally via the nFAULT pin.

#### 7.3.2.4 EN Pin

EN is a logic-level input signal, referenced to V<sub>IO</sub>, from a CAN FD controller to the TCAN1043N-Q1. The EN input pin is for mode selection in conjunction with the nSTB pin. EN is internally pulled low to prevent excessive system power and false wake-up events.

#### 7.3.2.5 nSTB Pin

nSTB is a logic-level input signal, referenced to V<sub>IO</sub>, from a CAN FD controller to the TCAN1043N-Q1. The nSTB input pin is for mode selection in conjunction with the EN pin. nSTB is internally pulled low to prevent excessive system power and false wake-up events.

#### 7.3.3 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

## 7.3.4 INH Pin

The INH pin is a high-voltage output. It can be used to control external regulators. These regulators are usually used to support the microprocessor and V<sub>IO</sub> pin. The INH function is on in all modes except for sleep mode. In sleep mode, the INH pin is turned off, going into a high-impedance state. This allows the node to be placed into the lowest power state while in sleep mode. A  $100k\Omega$  load can be added to the INH output for a fast transition time from the driven high state to the low state and to force the pin low when left floating.

This terminal should be considered a high-voltage logic terminal, not a power output. The INH pin should be used to drive the EN terminal of the system power management device, and is not used as a switch for the

power management supply itself. This terminal is not reverse-battery protected, and must not be connected outside the system module.

#### 7.3.5 WAKE Pin

The WAKE pin is a high-voltage reverse-blocked input used for the local wake-up (LWU) function. The WAKE pin is bi-directional edge-triggered and recognizes a local wake-up (LWU) on either a rising or falling edge of WAKE pin transition. The LWU function is explained further in the Local Wake-Up (LWU) via WAKE Input Terminal section.

#### 7.3.6 CAN Bus Pins

These are the CAN high and CAN low, CANH and CANL, differential bus pins. These pins are internally connected to the CAN transceiver and the low-voltage wake receiver.

#### 7.3.7 Faults

#### 7.3.7.1 Internal and External Fault Indicators

The following device status indicator flags are implemented to allow for the MCU to determine the status of the device and the system. In addition to faults, the nFAULT terminal also signals wake-up requests and a cold power-up sequence on the  $V_{SUP}$  battery terminal so the system can do any diagnostics or cold booting sequence necessary. The RXD terminal indicates wake-up request and the faults are multiplexed (ORed) to the nFAULT output.



#### Table 7-1. TCAN1043N-Q1 Transceiver Status Indicator

EVENT	FLAG NAME	CAUSE	INDICATORS(1)	FLAG IS CLEARED	COMMENT
Power-up	PWRON	Power up on $V_{SUP}$ and any return of $V_{SUP}$ after it has been below $UV_{SUP}$	nFAULT = low upon entering silent mode from standby or sleep mode	After a transition to normal mode	A cold start condition generates a local wake-up WAKERQ, WAKESR and a PWRON flag.
Wake-up Request	WAKERQ <sup>(2)</sup>		nFAULT = RXD = low after wake-up upon entering standby mode	After a transition to normal mode or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \ge t_{UV}$	Wake-up request may only be set from standby, go-to-sleep, or sleep mode. Resets timers for UV <sub>VCC</sub> or UV <sub>VIO</sub> .
Wake-up Source Recognition <sup>(3)</sup>	WAKESR	Wake-up event on CAN bus, state transition on WAKE pin, or initial power up	Available upon entering normal mode(4) nFAULT = low indicates a local wake-up event from the WAKE pin nFAULT = high indicates a remote wake-up event from the CAN bus	After four recessive-to-dominant edges on TXD in normal mode, leaving normal mode, or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \ge t_{UV}$	A cold start condition generates a local wake-up WAKERQ, WAKESR and a PWRON flag.
	UV <sub>CC</sub>	V <sub>CC</sub> < UV <sub>CC(F)</sub>	Not externally indicated	V <sub>CC</sub> > UV <sub>CC(R),</sub> or a wake-up request occurs	
Undervoltage	UV <sub>IO</sub>	V <sub>IO</sub> < UV <sub>IO(F)</sub>	Not externally indicated	V <sub>IO</sub> > UV <sub>IO(R),</sub> or a wake-up request occurs	
	UV <sub>SUP</sub>	V <sub>SUP</sub> < UV <sub>SUP(F)</sub>	Not externally indicated	V <sub>SUP</sub> > UV <sub>SUP(R)</sub>	A V <sub>SUP</sub> undervoltage event generates a cold start condition once V <sub>SUP</sub> > UV <sub>SUP(R)</sub>
CAN Bus Fault	CBF	See CAN Bus Fault	nFAULT = low in normal mode only <sup>(5)</sup>	Upon leaving normal mode, or if no CAN bus fault is detected for four consecutive dominant-to-recessive transitions of the TXD pin while in normal mode	CAN bus fault must persist for four consecutive dominant-to-recessive transitions
Local Faults	TXDDTO	TXD dominant time out, dominant (low) signal for t ≥ t <sub>TXDDTO</sub>	nFAULT = low upon entering silent mode from normal mode	RXD = low & TXD = high, TXD = high & a mode transition into normal, standby, go-to-sleep, or sleep	CAN driver remains disabled until the <i>TXDDTO</i> is cleared. CAN receiver remains active during the TXDDTO fault
	TXDRXD	TXD and RXD pins are shorted together for t ≥ t <sub>TXDDTO</sub>		modes	CAN driver remains disabled until the <i>TXDRXD</i> is cleared. CAN receiver remains active during the TXDRXD fault
	CANDOM	CAN bus dominant fault, when dominant bus signal received for t ≥ t <sub>BUSDOM</sub>		RXD = high, or a transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains enabled during CANDOM fault
	TSD	Thermal shutdown, T <sub>J</sub> ≥ T <sub>SDR</sub>		T <sub>J</sub> < T <sub>SDF</sub> and RXD = low & TXD = high, or transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains disabled until the <i>TSD</i> event is cleared

- (1) V<sub>IO</sub> and V<sub>SUP</sub> are present
- Transitions to go-to-sleep mode is blocked until WAKERQ flag is cleared
- (3) Wake-up source recognition reflects the first wake up source. If additional wake-up events occur the source still indicates the original wake-up source
- Indicator is only available in normal mode until the flag is cleared
- CAN Bus failure flag is indicated after four dominant-to-recessive edges on TXD

#### 7.3.7.1.1 Power-Up (PWRON Flag)

This is an internal and external flag that can be used to control the power-up sequence of the system. When a new battery connection to the transceiver is made the PWRON flag is set signifying a cold start condition. The TCAN1043N-Q1 treats any undervoltage conditions on the  $V_{SUP}$ ,  $V_{SUP}$  <  $UV_{SUP(F)}$ , as a cold start. Therefore, when the V<sub>SUP</sub> > UV<sub>SUP(R)</sub> condition is met the TCAN1043N-Q1 sets the PWRON flag which can be used by the system to enter a routine that is only called upon in cold start situations. The PWRON flag is indicated by nFAULT driven low after entering silent mode from either standby mode or sleep mode. This flag is cleared after a transition to normal mode.

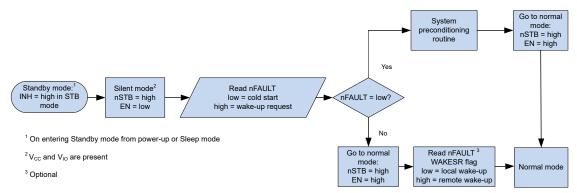


Figure 7-2. Distinguishing between PWRON and Wake Request by Entering Silent Mode

#### 7.3.7.1.2 Wake-Up Request (WAKERQ Flag)

This is an internal and external flag that can be set in standby, go-to-sleep, or sleep mode. This flag is set when either a valid local wake-up (LWU) request occurs, or a valid remote wake request occurs, or on power up on  $V_{SUP}$ . The setting of this flag clears the  $t_{UV}$  timer for the  $UV_{CC}$  or  $UV_{IO}$  fault detection. This flag is cleared upon entering normal mode or during an undervoltage event on  $V_{CC}$  or  $V_{IO}$ .

#### 7.3.7.1.3 Undervoltage Faults

The TCAN1043N-Q1 device implements undervoltage detection circuits on all supply terminals:  $V_{SUP}$ ,  $V_{CC}$ , and  $V_{IO}$ . The undervoltage flags are internal indicator flags and are not indicated on the nFAULT output pin.

## 7.3.7.1.3.1 Undervoltage on V<sub>SUP</sub>

 $UV_{SUP}$  is set when the voltage on  $V_{SUP}$  drops below the undervoltage detection voltage threshold,  $UV_{SUP}$ . The PWRON and WAKERQ flags are set once  $V_{SUP} > UV_{SUP(R)}$ .

## 7.3.7.1.3.2 Undervoltage on V<sub>CC</sub>

 $UV_{CC}$  is set when the voltage on  $V_{CC}$  drops below the undervoltage detection voltage threshold,  $UV_{CC}$ , for longer than the  $t_{UV}$  undervoltage filter time.

## 7.3.7.1.3.3 Undervoltage on V<sub>IO</sub>

 $UV_{IO}$  is set when the voltage on  $V_{IO}$  drops below the undervoltage detection voltage threshold,  $UV_{IO}$ , for longer than the  $t_{IIV}$  undervoltage filter time.

### 7.3.7.1.4 CAN Bus Fault (CBF Flag)

The TCAN1043N-Q1 device can detect the following six fault conditions and set the nFAULT pin low as an interrupt so that the controller can be notified and act if a CAN bus fault exists. These failures are detected while transmitting a dominant signal on the CAN bus. If one of these fault conditions persists for four consecutive dominant-to-recessive bit transitions, the nFAULT indicates a CAN bus failure flag in Normal mode by driving the nFAULT pin low. The CAN bus driver remains active. Table 7-2 shows what fault conditions can be detected by the TCAN1043N-Q1.

 FAULT
 Condition

 1
 CANH Shorted to V<sub>BAT</sub>

 2
 CANH Shorted to V<sub>CC</sub>

 3
 CANH Shorted to GND

 4
 CANL Shorted to V<sub>BAT</sub>

 5
 CANL Shorted to V<sub>CC</sub>

CANL Shorted to GND

Table 7-2. Bus Fault Pin State and Detection Table

6



Bus fault detection is a system level situation. If the fault is occurring at the ECU, the general communication of the bus may be compromised. Until a diagnostic determination can be made, the transceiver remains in CAN active mode during a CAN bus fault enabling the ECU to transmit data to the CAN bus and receive data from the CAN bus. For complete coverage of a node, a system level diagnostic step should be performed for each node and the information should be communicated back to a central point.

While in normal mode, if no CAN bus fault is detected for four consecutive dominant-to-recessive transitions on the TXD pin then the CBF flag is cleared and nFAULT is driven high. The bus fault failure circuitry is able to detect bus faults for a range of differential resistance loads (R<sub>CBF</sub>) and for any time greater than t<sub>CBF</sub>.

### 7.3.7.1.5 TXD Dominant State Timeout (TXDDTO Flag)

TXDDTO is an external flag that is set if the TXD pin is held dominant for t >  $t_{TXDDTO}$ . If a TXD DTO condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode. The TXDDTO flag is cleared on the next dominant-to-recessive transition on TXD or upon a transition into normal, standby, go-to-sleep, or sleep modes.

#### 7.3.7.1.6 TXD Shorted to RXD Fault (TXDRXD Flag)

TXDRXD is an external flag that is set if the transceiver detects that the TXD and RXD lines have been shorted together for  $t \ge t_{TXDDTO}$ . If a TXDRXD condition exists the nFAULT pin is driven low upon entering silent mode from normal mode and the CAN bus driver is disabled until the TXDRXD fault is cleared. The TXDRXD flag is cleared on the next dominant-to-recessive transition with TXD high and RXD low or upon a transition into normal, standby, go-to-sleep, or sleep modes.

## 7.3.7.1.7 CAN Bus Dominant Fault (CANDOM Flag)

CANDOM is an external flag that is set if the CAN bus is stuck dominant state for  $t > t_{BUSDOM}$ . If a CANDOM condition exists the nFAULT pin is driven low upon entering silent mode from normal mode. The CANDOM flag is cleared on the next dominant-to-recessive transition on RXD or upon a transition into normal, standby, go-to-sleep, or sleep modes.

#### 7.3.8 Local Faults

Local faults are detected in both normal mode and silent mode, but are only indicated via the nFAULT pin when the TCAN1043N-Q1 transitions from normal mode to silent mode. All other mode transitions clear the local fault flag indicators.

## 7.3.8.1 TXD Dominant Timeout (TXD DTO)

While the CAN driver is in active mode a TXD dominant state timeout circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the timeout period,  $t > t_{TXDDTO}$ . The TXD dominant state timeout circuit is triggered by a falling edge on the TXD pin. If no rising edge is seen before on TXD before  $t > t_{TXDDTO}$  than the CAN driver is disabled releasing the bus lines to the recessive level. This keeps the bus free for communication between other nodes on the network.

The CAN driver will be activated again on the next dominant-to-recessive transition on the TXD pin. During a *TXDDTO* fault the high-speed receiver remains active and the RXD output pin will mirror the CAN bus.

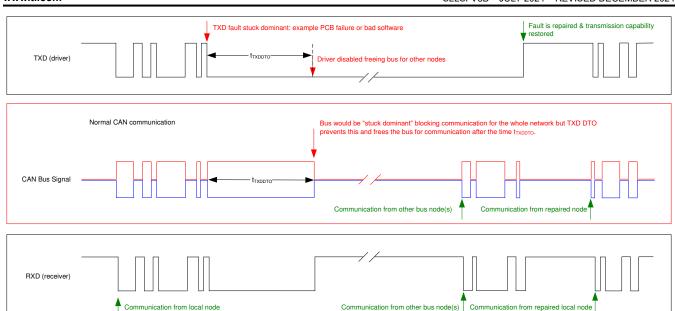


Figure 7-3. Timing Diagram for TXD DTO

The minimum dominant TXD time allowed by the dominant state timeout circuit limits the minimum possible transmitted data rate of the transceiver. The CAN protocol allows a maximum of eleven successive dominant bits to be transmitted in the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using the minimum transmitted in Equation 1.

Minimum Data Rate = 11 bits / 
$$t_{TXDDTO}$$
 = 11 bits / 1.2ms = 9.2kbps (1)

#### 7.3.8.2 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1043N-Q1 exceeds the thermal shutdown threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The CAN bus terminals are biased to recessive level during a TSD fault and the receiver to RXD path remains operational. The TSD fault condition is cleared when the junction temperature,  $T_J$ , of the device drops below the thermal shutdown release temperature,  $T_{SDF}$ , of the device. If the fault condition that caused the TSD fault is still present, the temperature may rise again and the device will enter thermal shutdown again. Prolonged operation with TSD fault conditions may affect device reliability. The TSD circuit includes hysteresis to avoid any oscillation of the driver output. During the fault the TSD fault condition is indicated to the CAN FD controller via the nFAULT terminal.

## 7.3.8.3 Undervoltage Lockout (UVLO)

The supply terminals,  $V_{SUP}$ ,  $V_{IO}$  and  $V_{CC}$ , are monitored for undervoltage events. If an undervoltage event occurs the TCAN1043N-Q1 enters a protected state where the bus pins present no load to the CAN bus. This protects the CAN bus and system from unwanted glitches and excessive current draw that could impact communication between other CAN nodes on the CAN bus.

If an undervoltage event occurs on  $V_{\text{SUP}}$  in any mode, the TCAN1043N-Q1 CAN transceiver enters the CAN off state.

If an undervoltage event occurs on  $V_{CC}$ , the TCAN1043N-Q1 remains in normal or silent mode but the CAN transceiver changes to the CAN autonomous active state. During a UV<sub>CC</sub> event, RXD remains high as long as  $V_{IO}$  is present and the wake-up circuitry is inactive. See Figure 7-9. If the undervoltage event persists longer than  $t_{UV}$ , the TCAN1043N-Q1 transitions to sleep mode.

If an undervoltage event occurs on the  $V_{IO}$ , the TCAN1043N-Q1 transitions to standby mode. If the undervoltage event persists longer than  $t_{UV}$ , the TCAN1043N-Q1 transitions to sleep mode.

Once an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically needs 200µs to transition to normal operation.

### 7.3.8.4 Unpowered Devices

The device is designed to be a passive or no load to the CAN bus if the device is unpowered. The CANH and CANL pins have low leakage currents when the device is unpowered, thus, presenting no load to the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The logic terminals also have low leakage currents when the device is unpowered, so the terminals do not load down other circuits which may remain powered.

#### 7.3.8.5 Floating Terminals

The TCAN1043N-Q1 has internal pull-ups and pull-downs on critical pins to make sure a known operating behavior if the pins are left floating. See Table 7-3 for the pin fail-safe biasing protection description.

Table 7-3. Pin Fail-safe Biasing

PIN	FAIL-SAFE PROTECTION	VALUE	COMMENT
TXD	Recessive level		Weak pull-up to V <sub>IO</sub>
EN	Low-power mode	60kΩ	Weak pull-down to GND
nSTB	Low-power mode		Weak pull-down to GND

This internal bias should not be relied upon by design but rather a fail-safe option. Special care needs to be taken when the transceiver is used with a CAN FD controller that has open-drain outputs. The TCAN1043N-Q1 implements a weak internal pull-up resistor on the TXD pin. The bit timing requirements for CAN FD data rates require special consideration and the pull-up strength should be considered carefully when using open-drain outputs. An adequate external pull-up resistor must be used to make sure the TXD output of the CAN FD controller maintains proper bit timing input to the CAN device.

#### 7.3.8.6 CAN Bus Short-Circuit Current Limiting

The TCAN1043N-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. The features include CAN driver current limiting in the dominant and recessive states, and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in a system fault.

During CAN communication, the bus switches between the dominant and recessive states. Thus, the shortcircuit current may be viewed either as the current during each bus state or as an average current. The average short-circuit current can be used when considering system power for the termination resistors and common-mode choke. The percentage of time that the driver can be dominant is limited by the TXD dominant state timeout and the CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe spacing. These make sure there is a minimum recessive time on the bus even if the data field contains a high percentage of dominant bits.

The short-circuit current of the bus depends on the ratio of recessive to dominant bits and the respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%$$
Transmit × [( $\%$ REC\_Bits ×  $I_{OS(SS)}$  REC) + ( $\%$ DOM\_Bits ×  $I_{OS(SS)}$  DOM)] + [ $\%$ Receive ×  $I_{OS(SS)}$  REC] (2)

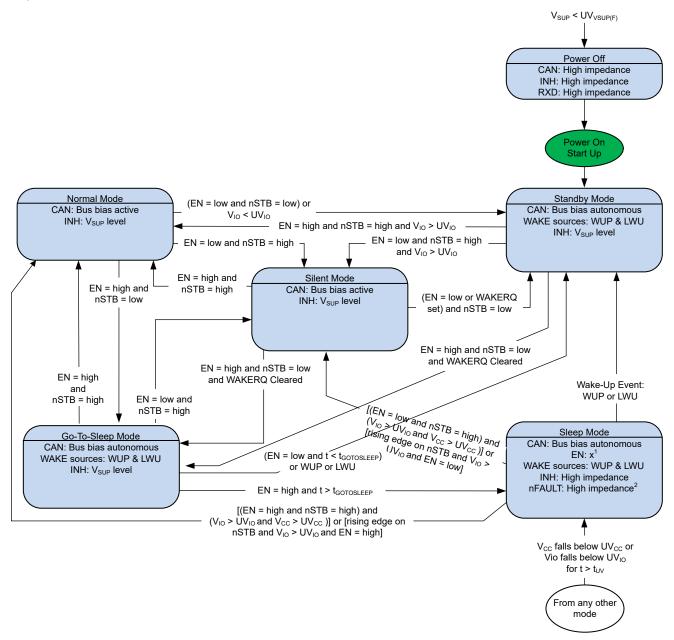
#### Where:

- I<sub>OS(AVG)</sub> is the average short-circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM Bits is the percentage of dominant bits in the transmitted CAN messages
- I<sub>OS(SS)</sub> REC is the recessive steady state short-circuit current
- I<sub>OS(SS)</sub> DOM is the dominant steady state short-circuit current

The short-circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components.

### 7.4 Device Functional Modes

The TCAN1043N-Q1 has six operating modes: normal, standby, silent, go-to-sleep, sleep, and off mode. Operating mode selection is controlled using the nSTB pin and EN pin in conjunction with supply conditions, temperature conditions, and wake events.



- 1. The enable pin can be in a logical high or low state while in sleep mode, but since the pin has an internal pull-down, the lowest possible power consumption occurs when the pin is left either floating or pulled low externally.
- 2. The nFAULT pin is in high impedance mode if  $V_{IO} < UV_{IO}$ . The nFAULT pin is in logic high, if  $V_{IO} > UV_{IO}$ .

Figure 7-4. TCAN1043N-Q1 State Machine



#### Table 7-4. TCAN1043N-Q1 Mode Overview

MODE	V <sub>CC</sub> and V <sub>IO</sub>	V <sub>SUP</sub>	EN	nSTB	WAKERQ FLAG	DRIVER	RECEIVER	RXD	INH
Normal	> UV <sub>CC</sub> and > UV <sub>IO</sub>	> UV <sub>SUP</sub>	High	High	Х	Enabled	Enabled	Mirrors bus state	On
Silent	> UV <sub>CC</sub> and > UV <sub>IO</sub>	> UV <sub>SUP</sub>	Low	High	Х	Disabled	Enabled	Mirrors bus state	On
	> UV <sub>CC</sub> and> UV <sub>IO</sub>	> UV <sub>SUP</sub>	High	Low	Set	Disabled	Low power bus monitor enabled	Low signals wake-up	On
Standby	> UV <sub>CC</sub> and > UV <sub>IO</sub>	> UV <sub>SUP</sub>	Low	Low	Х	Disabled	Low power bus monitor enabled	Low signals wake-up	On
	> UV <sub>CC</sub> and < UV <sub>IO</sub>	> UV <sub>SUP</sub>	Low	Low	Х	Disabled	Low power bus monitor enabled	High impedance	On
Go-to-sleep <sup>(1)</sup>	> UV <sub>CC</sub> and > UV <sub>IO</sub>	> UV <sub>SUP</sub>	High	Low	Cleared	Disabled	Low power bus monitor enabled	High or high impedance (no V <sub>IO</sub> )	On <sup>(2)</sup>
Sleep <sup>(3)</sup>	> UV <sub>CC</sub> and> UV <sub>IO</sub>	> UV <sub>SUP</sub>	High	Low	Cleared	Disabled	Low power bus monitor enabled	High or high impedance (no V <sub>IO</sub> )	High Impedance
	< UV <sub>CC</sub> or <uv<sub>IO</uv<sub>	> UV <sub>SUP</sub>	Х	х	Х	Disabled	Low power bus monitor enabled	High or high impedance (no V <sub>IO</sub> )	High impedance
Protected	Х	< UV <sub>SUP</sub>	х	х	Х	Disabled	Disabled	High impedance	High impedance

- Go-to-sleep: Transitional mode for EN = H, nSTB = L until  $t_{GOTOSLEEP}$  timer has expired.
- The INH pin transitions to high impedance after the  $t_{\mbox{\scriptsize GOTOSLEEP}}$  timer has expired.
- Mode change from go-to-sleep mode to sleep mode once  $t_{\hbox{\scriptsize GOTOSLEEP}}$  timer has expired. (3)

## 7.4.1 Operating Mode Description

#### 7.4.1.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

Entering normal mode clears both the WAKERQ and the PWRON flags.

#### 7.4.1.2 Silent Mode

Silent mode is commonly referred to as listen only and receive only mode. In this mode, the CAN driver is disabled but the receiver is fully operational and CAN communication is unidirectional into the device. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD terminal.

In silent mode, PWRON and Local Failure flags are indicated on the nFAULT pin.

#### 7.4.1.3 Standby Mode

Standby mode is a low-power mode where the driver and receiver are disabled, reducing current consumption. However, this is not the lowest power mode of the device since the INH terminal is on, allowing the rest of the system to resume normal operation.

During standby mode, a wake-up request (WAKERQ) is indicated by the RXD terminal being low. The wake-up source is identified via the nFAULT pin after the device is returned to normal mode.

### 7.4.1.4 Go-To-Sleep Mode

Go-to-sleep mode is the transitional mode of the device from any state to sleep. In this state the driver and receiver are disabled, reducing the current consumption. The INH pin is active to supply an enable to the V<sub>IO</sub> controller which allows the rest of the system to operate normally. If the device is held in this state for t ≥ t<sub>GOTOSLEEP</sub> the device transitions to sleep mode and the INH turns off transitioning to the high impedance state.

If any wake-up events persist, the TCAN1043N-Q1 remains in standby mode until the device is switched into normal mode to clear the pending wake-up events.

#### 7.4.1.5 Sleep Mode

Sleep mode is the lowest power mode of the TCAN1043N-Q1. In sleep mode, the CAN transmitter and the main receiver are switched off and the transceiver cannot send or receive data. The low power receiver is able to monitor the bus for any activity that validates the wake-up pattern (WUP) requirements, and the WAKE monitoring circuit monitors for state changes on the WAKE terminal for a local wake-up (LWU) event. ISUP

current is reduced to the minimum level when the CAN transceiver is in CAN autonomous inactive state. The INH pin is switched off in sleep mode causing any system power supplies controlled by INH to be switched off thus reducing system power consumption.

### Sleep mode is exited:

- If a valid wake-up pattern (WUP) is received via the CAN bus pins
- On a local WAKE (LWU) event
- nSTB is high and VCC > UV<sub>CC</sub> and VIO > UV<sub>IO</sub> (the device enters Normal or Silent mode depending upon the logic level on the EN pin.

#### 7.4.1.5.1 Remote Wake Request via Wake-Up Pattern (WUP)

The TCAN1043N-Q1 implements a low-power wake receiver in the standby and sleep mode that uses the multiple filtered dominant wake-up pattern (WUP) defined in the ISO11898-2:2024 standard.

The wake-up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered dominant bus time. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive; other bus traffic will not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant, and other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant, the bus monitor recognizes the WUP, and drives the RXD terminal low. If a valid  $V_{IO}$  is present, the controller is signaled for a wake-up request. If a valid  $V_{IO}$  is not present when the wake-up pattern is received, the transceiver drives the RXD output pin low once  $V_{IO} > UV_{IOR}$ .

#### The WUP consists of:

- A filtered dominant bus of at least t<sub>WK(FILTER)</sub> followed by
- A filtered recessive bus time of at least t<sub>WK(FILTER)</sub> followed by
- A second filtered dominant bus time of at least t<sub>WK(FILTER)</sub>

For a dominant or recessive to be considered *filtered*, the bus must be in that state for more than  $t_{WK(FILTER)}$  time. Due to variability in the  $t_{WK(FILTER)}$ , the following scenarios are applicable. Bus state times less than the  $t_{WK(FILTER)}$  minimum are never detected as part of a WUP, and no wake request is generated. Bus state times between  $t_{WK(FILTER)}$  minimum and  $t_{WK(FILTER)}$  maximum may be detected as part of a WUP and a wake request may be generated. Bus state times more than  $t_{WK(FILTER)}$  maximum is always detected as part of a WUP, and a wake request is always generated. See Figure 7-5 for the timing diagram of the WUP.

The pattern and  $t_{WK(FILTER)}$  time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

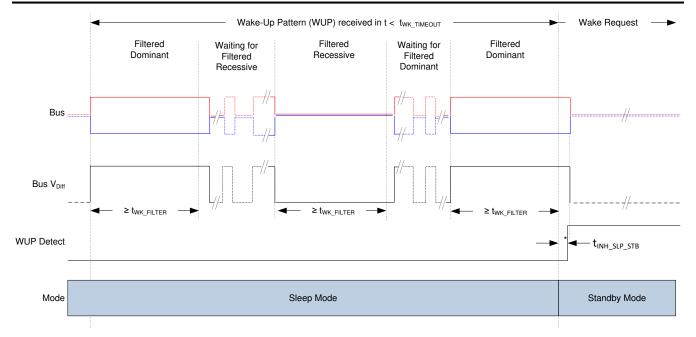
ISO11898-2:2024 has two sets of times for a short and long wake-up filter times. The  $t_{WK(FILTER)}$  timing for the TCAN1043N-Q1 has been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back to back bit times at 1Mbps triggers the filter in either bus state.

For an additional layer of robustness and to prevent false wake-ups, the transceiver implements the  $t_{WK(TIMEOUT)}$  timer. For a remote wake-up event to successfully occur, the entire wake-up pattern must be received within the timeout value. If the full wake-up pattern is not received before the  $t_{WK(TIMEOUT)}$  expires then the internal logic is reset and the transceiver remains in sleep mode without waking up. The full pattern must then be transmitted again within the  $t_{WK(TIMEOUT)}$  window. See Figure 7-5.

A recessive bus of at least  $t_{WK(FILTER)}$  must separate the next WUP pattern if the CAN bus is dominant when the  $t_{WK(TIMEOUT)}$  expires.

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<sup>\*</sup>The RXD pin is only driven once  $V_{IO}$  is present.

Figure 7-5. Wake-Up Pattern (WUP)

#### 7.4.1.5.2 Local Wake-Up (LWU) via WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage reverse-battery protected input which can be used for local wake-up (LWU) requests via a voltage transition. A LWU event is triggered on either a low-to-high or high-to-low transition since the terminal has bi-directional input thresholds. The WAKE pin could be used with a switch to  $V_{SUP}$  or to ground. Unused terminals should be pulled to  $V_{SUP}$  or ground to avoid unwanted parasitic wake-up events.

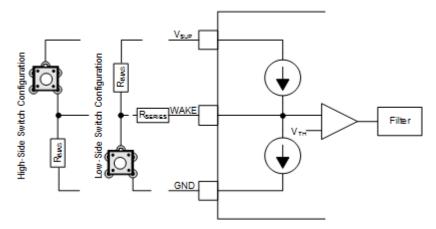


Figure 7-6. WAKE Circuit Example

Figure 7-6 shows two possible configurations for the WAKE pin, a low-side and high-side switch configuration. The objective of the series resistor, R<sub>SERIES</sub>, is to protect the WAKE input of the device from over current conditions that may occur in the event of a ground shift or ground loss. The minimum value of R<sub>SERIES</sub> can be calculated using the maximum supply voltage, V<sub>SUPMAX</sub>, and the maximum allowable current of the WAKE pin, I<sub>IO(WAKE)</sub>. R<sub>SERIES</sub> is calculated using:

$$R_{SERIES} = V_{SUPMAX} / I_{IO(WAKE)}$$
(3)

With absolute maximum voltage,  $V_{SUPMAX}$ , of 45V and maximum allowable  $I_{IO(WAKE)}$  of 3mA, the minimum required  $R_{SERIES}$  value is 15k $\Omega$ .

The  $R_{BIAS}$  resistor is used to set the static voltage level of the WAKE input when the switch is released. When the switch is in use in a high-side switch configuration, the  $R_{BIAS}$  resistor in combination with the  $R_{SERIES}$  resistor sets the WAKE pin voltage above the  $V_{IH}$  threshold. The maximum value of  $R_{BIAS}$  can be calculated using the maximum supply voltage,  $V_{SUPMAX}$ , the maximum WAKE threshold voltage  $V_{IH}$ , the maximum WAKE input current  $I_{IH}$  and the series resistor value  $R_{SERIES}$ .  $R_{BIAS}$  is calculated using:

$$R_{BIAS} < ((V_{SUPMAX} - V_{IH}) / I_{IH}) - R_{SERIES}$$

$$\tag{4}$$

With  $V_{SUPMAX}$  of 45V,  $V_{IH}$  of 44V at  $I_{IH}$  of  $3\mu A$ , the  $R_{BIAS}$  resistor value must be less than  $330k\Omega$ . The recommendations is to use  $R_{Series}$  less than  $50k\Omega$  to provide better margin for the WAKE pin voltage to rise above  $V_{IH}$  when the switch is released.

The LWU circuitry is active in sleep mode.

The WAKE circuitry is switched off in normal mode.

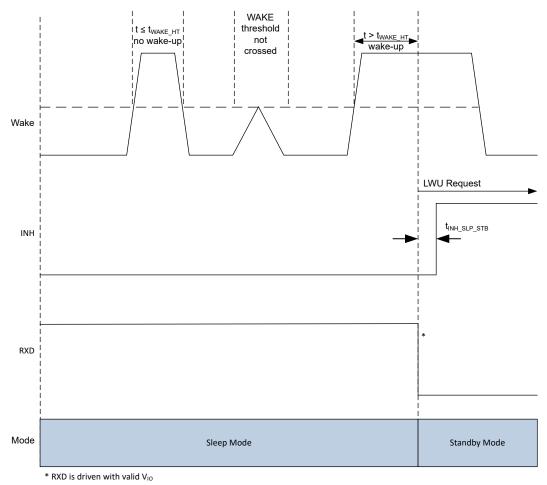


Figure 7-7. LWU Request Rising Edge



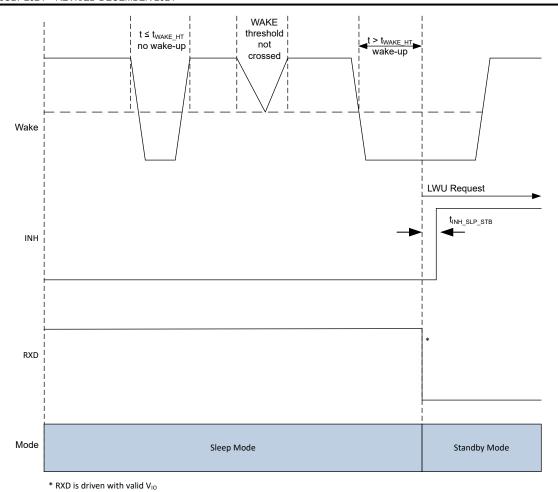


Figure 7-8. LWU Request Falling Edge

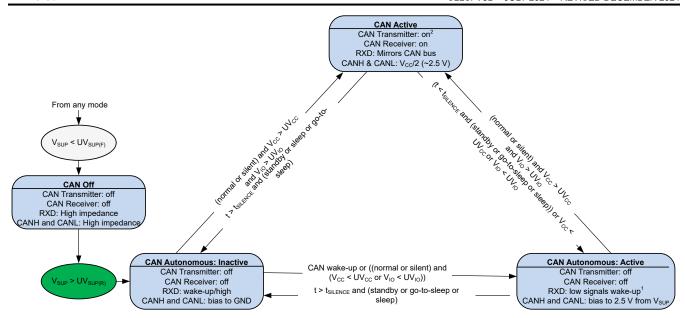
## 7.4.2 CAN Transceiver

## 7.4.2.1 CAN Transceiver Operation

The TCAN1043N-Q1 supports the ISO 11898-2:2024 CAN physical layer standard autonomous bus biasing scheme. Autonomous bus biasing enables the transceiver to switch between CAN active, CAN autonomous active, and CAN autonomous inactive which helps to reduce RF emissions.

## 7.4.2.1.1 CAN Transceiver Modes

The TCAN1043N-Q1 CAN transceiver has four modes of operation; CAN off, CAN autonomous active, CAN autonomous inactive and CAN active.



- 1. Wake-up is inactive in normal or silent mode.
- 2. CAN transmitter is off in silent mode.

Figure 7-9. TCAN1043N-Q1 CAN Transceiver State Machine

#### 7.4.2.1.1.1 CAN Off Mode

In CAN off mode the CAN transceiver is switched off and the CAN bus lines are truly floating. In this mode the device presents no load to the CAN bus while preventing reverse currents from flowing into the device if the battery or ground connection is lost.

The CAN off state is entered if:

V<sub>SUP</sub> < UV<sub>SUPF</sub>

The CAN transceiver switches between the CAN off state and CAN autonomous inactive mode if:

V<sub>SUP</sub> > UV<sub>SUPR</sub>

#### 7.4.2.1.1.2 CAN Autonomous: Inactive and Active

When the CAN transceiver is in standby, go-to-sleep or sleep mode, the bias circuit can be in either the CAN autonomous inactive or CAN autonomous active state. In the autonomous inactive state, the CAN pins are biased to GND. When a remote wake-up (WUP) event occurs, the CAN bus is biased to 2.5V and the CAN transceiver enters the CAN autonomous active state. If the controller does not transition the transceiver into normal mode before the t<sub>SILENCE</sub> timer expires, the CAN transceiver enters the CAN autonomous inactive state.

The CAN transceiver switches to the CAN autonomous mode if any of the following conditions are met:

- · The operating mode changes from CAN off mode to CAN autonomous inactive
- The operating mode changes from normal or silent mode to standby, go-to-sleep, or sleep mode:
  - If the bus was inactive for t < t<sub>SILENCE</sub> before the mode change, the transceiver enters autonomous active
  - If the bus was inactive for t > t<sub>SILENCE</sub> before the mode change, the transceiver enters autonomous inactive state
- V<sub>CC</sub> < UV<sub>CC(F)</sub>
- V<sub>IO</sub> < UV<sub>IO(F)</sub>

The CAN transceiver switches from the CAN autonomous inactive mode to the CAN autonomous active mode if:

- A remote wake-up event occurs
- The transceiver transitions to normal or silent mode and V<sub>CC</sub> < UV<sub>CC(F)</sub> or V<sub>IO</sub> < UV<sub>IO(F)</sub>

The CAN transceiver switches from the CAN autonomous active mode to the CAN autonomous inactive mode if:

The transceiver is in standby, go-to-sleep, or sleep mode and t > t<sub>SILENCE</sub>

#### 7.4.2.1.1.3 CAN Active

When the transceiver is in normal or silent mode, the CAN transceiver is in active mode. In normal mode, the CAN driver and receiver are fully operational and CAN communication is bi-directional. In silent mode, the CAN driver is off but the CAN receiver is fully operational. The CAN bias voltage in CAN active mode is derived from  $V_{\rm CC}$  and is held at  $V_{\rm CC}/2$ 

The CAN transceiver switches from the CAN autonomous inactive or CAN autonomous active modes to the CAN active mode if:

The transceiver transitions to normal mode and V<sub>CC</sub> > UV<sub>CC(R)</sub>, V<sub>IO</sub> > UV<sub>IO(R)</sub>

The CAN transceiver switches from the CAN active mode to the CAN autonomous inactive mode if:

The transceiver switches to standby, go-to-sleep, or sleep modes and t > t<sub>SILENCE</sub>

The CAN transceiver switches from the CAN active mode to the CAN autonomous active mode if:

- The transceiver switches to standby, go-to-sleep, or sleep modes and t < t<sub>SILENCE</sub>
- V<sub>CC</sub> < UV<sub>CC(F)</sub>
- V<sub>IO</sub> < UV<sub>IO(F)</sub>

## 7.4.2.1.2 Driver and Receiver Function Tables

**Table 7-5. Driver Function Table** 

DEVICE MODE	TXD INPUTS(1)	BUS OL	JTPUTS	DRIVEN BUS STATE(2)				
DEVICE WODE	TAD INFO13(7)	CANH	CANL	DRIVER BOS STATE				
Normal	Low	High	Low	Dominant				
Nomai	High or Open	High impedance	High impedance	V <sub>CC</sub> /2				
Silent	x	High impedance	High impedance	V <sub>CC</sub> /2				
Standby	x	High impedance	High impedance	Autonomous biasing				
Sleep	х	High impedance	High impedance	Autonomous biasing				

- (1) x = irrelevant
- (2) For bus states and typical bus voltages see Figure 7-10.

Table 7-6. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS V <sub>ID</sub> = V <sub>CANH</sub> - V <sub>CANL</sub>	BUS STATE	RXD TERMINAL		
	V <sub>ID</sub> ≥ 0.9 V	Dominant	Low		
Normal / Silent	0.5 V < V <sub>ID</sub> < 0.9 V	Indeterminate	Indeterminate		
Normal / Silent	V <sub>ID</sub> ≤ 0.5 V	Recessive	High		
	Open (V <sub>ID</sub> ≈ 0 V)	Open	High		
	V <sub>ID</sub> ≥ 1.15 V	Dominant			
Standby	0.4 V < V <sub>ID</sub> < 1.15 V	Indeterminate	High		
Stariuby	V <sub>ID</sub> ≤ 0.4	Recessive	Low if wake-up event persists		
	Open (V <sub>ID</sub> ≈ 0 V)	Open			
	V <sub>ID</sub> ≥ 1.15 V	Dominant			
Sleep / Go-to-	0.4 V < V <sub>ID</sub> < 1.15 V	Indeterminate	High Tri-state if V <sub>IO</sub> or V <sub>SUP</sub> are not		
sleep <sup>(1)</sup>	V <sub>ID</sub> ≤ 0.4 V	Recessive	present		
	Open (V <sub>ID</sub> ≈ 0 V)	Open			

(1) Low power wake-up receiver is active

#### 7.4.2.1.3 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 7-10.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to one half of the CAN transceiver supply voltage via the high resistance internal input resistors ( $R_{IN}$ ) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration when the differential voltage of the CAN bus is greater than the differential voltage of a single CAN driver. The TCAN1043N-Q1 CAN transceiver implements low-power standby modes which enable a third bus state where, if the CAN bus is inactive for t > t<sub>SILENCE</sub>. The bus pins are biased to ground via the high-resistance internal resistors of the receiver.

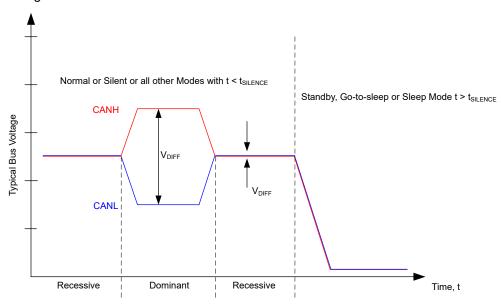


Figure 7-10. Bus States

# 8 Application Information Disclaimer

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TCAN1043N-Q1 transceiver is typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. These types of applications usually also include power management technology that allows for power to be gated to the application via an enable (EN) or inhibit (INH) pin. A single 5V regulator can be used to drive both  $V_{CC}$  and  $V_{IO}$ , or independent 5V and 3.3V regulators can be used to drive V<sub>CC</sub> and V<sub>IO</sub> separately as shown in Figure 8-1. The bus termination is shown for illustrative purposes.

## 8.1.1 Typical Application

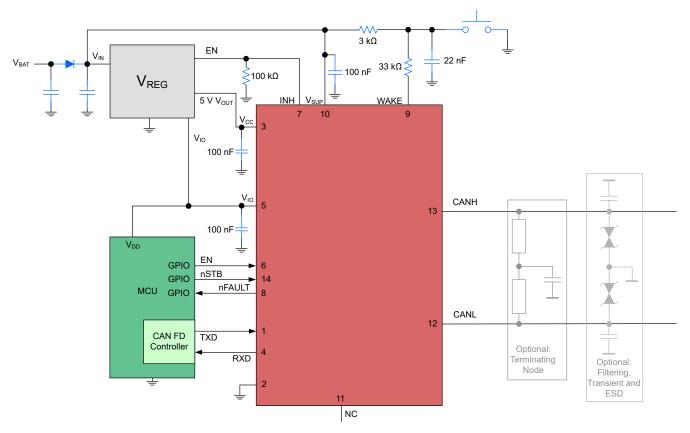


Figure 8-1. Typical Application

#### 8.1.2 Design Requirements

#### 8.1.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1043N-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2:2024 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification the differential output driver is specified with a bus load that can range from  $50\Omega$  to  $65\Omega$  where the differential output must be greater than 1.5V. The TCAN1043N-Q1 is specified to meet the 1.5V requirement down to  $50\Omega$  and is specified to meet 1.4V differential output at  $45\Omega$  bus load. The differential input resistance,  $R_{ID}$ , of the TCAN1043N-Q1 is a minimum of  $50k\Omega$ . If 100 TCAN1043N-Q1 transceivers are in parallel on a bus, this is equivalent to a  $500\Omega$  differential load in parallel with the nominal  $60\Omega$  bus termination which gives a total bus load of approximately  $54\Omega$ . Therefore, the TCAN1043N-Q1 theoretically supports over 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths allowing for these system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for a robust network operation.

## 8.1.3 Detailed Design Procedure

#### 8.1.3.1 CAN Termination

Termination may be a single  $120\Omega$  resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

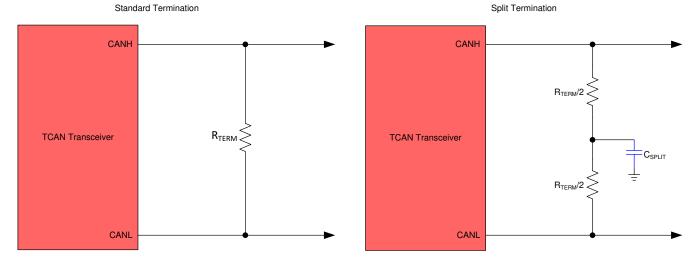


Figure 8-2. CAN Bus Termination Concepts

### 8.1.4 Application Curves

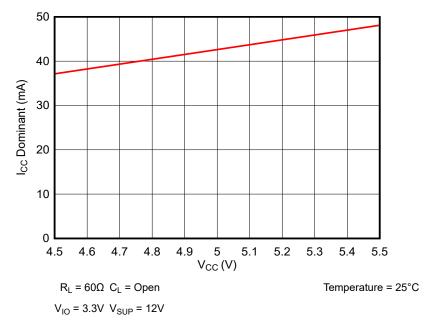


Figure 8-3. I<sub>CC</sub> Dominant over I<sub>CC</sub> Supply Voltage

## 8.2 Power Supply Recommendations

The TCAN1043N-Q1 is designed to operate off of three supply rails;  $V_{SUP}$ ,  $V_{CC}$ , and  $V_{IO}$ .  $V_{SUP}$  is a high-voltage supply pin designed to connect to the  $V_{BAT}$  rail,  $V_{CC}$  is a low-voltage supply pin with an input voltage range from 4.5V to 5.5V that supports the CAN transceiver and  $V_{IO}$  is a low-voltage supply pin with an input voltage range from 1.7V to 5.5V that provides the I/O voltage to match the system controller. For a reliable operation, a 100nF decoupling capacitor should be placed as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the output of switched-mode power supplies, and also helps to compensate for the resistance and inductance of the PCB power planes.

#### 8.3 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

### 8.3.1 Layout Guidelines

The layout example provides information on components around the device. Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. Transient voltage suppression (TVS) device can be added for extra protection, shown as D1. The production solution can be either a bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C6 and C7. A series common-mode choke (CMC) is placed on the CANH and CANL lines between the device and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance. Note that high-frequency currents follow the path of least impedance and not the path of least resistance. Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1 on V<sub>CC</sub>, C2 on V<sub>IO</sub>, and C3 and C4 on the V<sub>SUP</sub> supply.
- V<sub>IO</sub> pin of the transceiver is connected to the microcontroller IO supply voltage 'µC V'.

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- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R3 and R4, with the center or split tap of the termination connected to ground via capacitor C5. Split termination provides common-mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus thus also removing the termination.
- INH, pin 7, can have a 100kΩ resistor (R1) to ground.
- WAKE, pin 9, can recognize either a rising or a falling edge of a wake signal and is usually connected to an external switch. It should be configured as shown with C8 which is a 22nF capacitor to GND where R5 is  $33k\Omega$  and R6 is  $3k\Omega$ .
- INH\_MASK, pin 11, can be left floating or connected to GND when INH\_MASK function is not used. Do not
  connect to V<sub>IO</sub>.

### 8.3.2 Layout Example

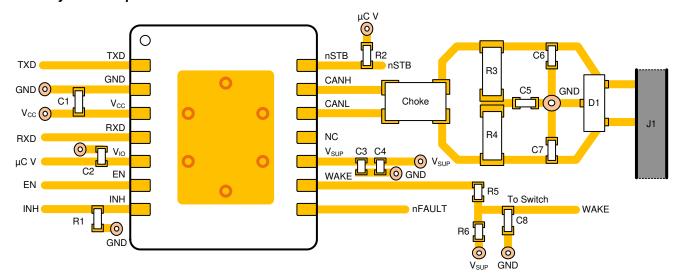


Figure 8-4. Example Layout

# 9 Device and Documentation Support

## 9.1 Documentation Support

# 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

# Changes from Revision A (November 2024) to Revision B (December 2024)

**Page** 

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TCAN1043N-Q1

14-Oct-2025 www.ti.com

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
PTCAN1043NDRQ1	Active	Preproduction	SOIC (D)   14	3000   LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN1043NDRQ1.A	Active	Preproduction	SOIC (D)   14	3000   LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN1043NDYYRQ1	Active	Preproduction	SOT-23-THIN (DYY)   14	3000   LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN1043NDYYRQ1.A	Active	Preproduction	SOT-23-THIN (DYY)   14	3000   LARGE T&R	-	Call TI	Call TI	-40 to 150	
TCAN1043NDMTRQ1	Active	Production	VSON (DMT)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1043N
TCAN1043NDMTRQ1.A	Active	Production	VSON (DMT)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1043N
TCAN1043NDRQ1	Active	Production	SOIC (D)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TCAN1043N
TCAN1043NDYYRQ1	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TCAN1043N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# PACKAGE OPTION ADDENDUM

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# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1043NDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043NDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1043NDYYRQ1	SOT-23- THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1043NDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1043NDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
TCAN1043NDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

PLASTIC SMALL OUTLINE



## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- 5. Reference JEDEC Registration MO-345, Variation AB



PLASTIC SMALL OUTLINE



- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



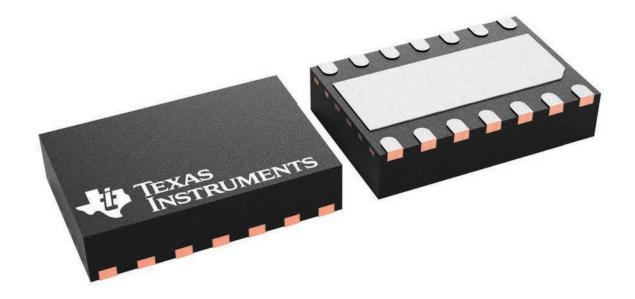
- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

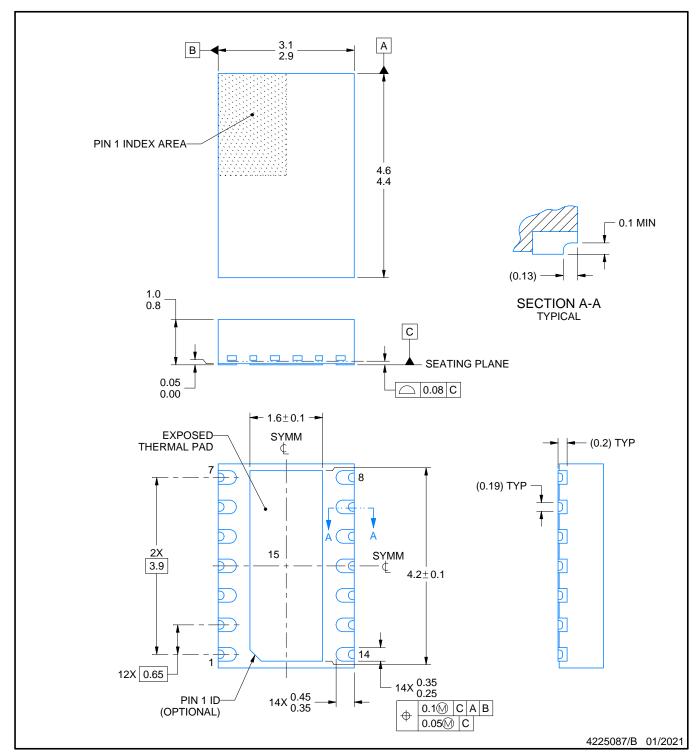
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC SMALL OUTLINE - NO LEAD



## NOTES:

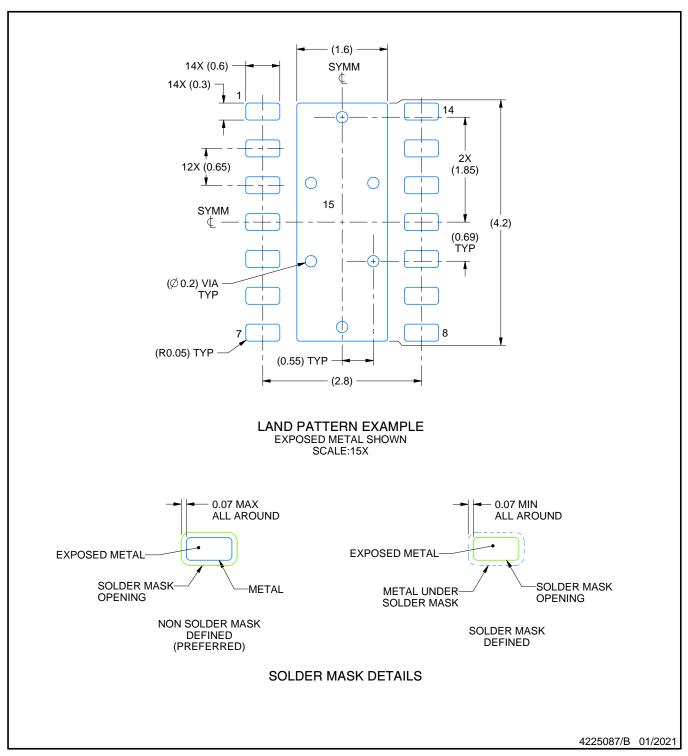
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



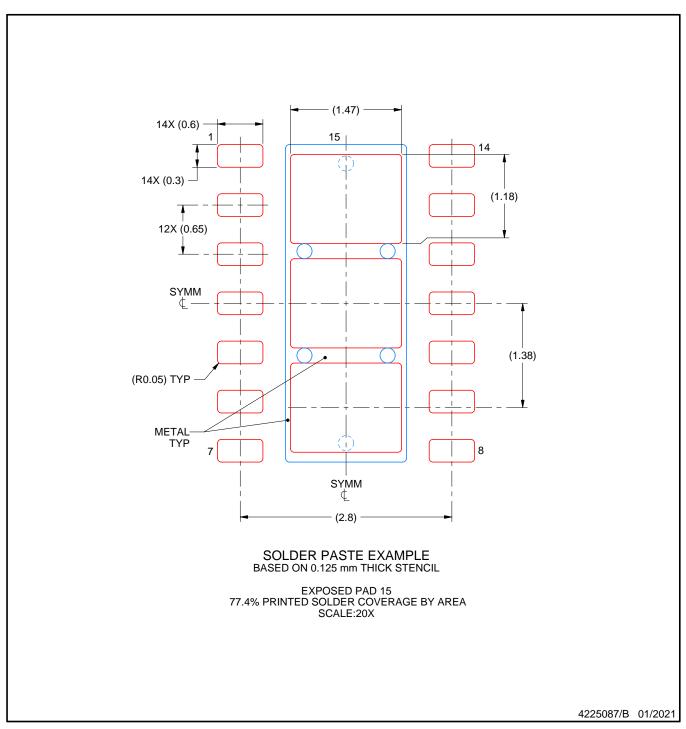
PLASTIC SMALL OUTLINE - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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