TAS5830 65W Stereo, Digital Input, High Efficiency Closed-Loop Class-D Amplifier with Class-H Algorithm

1 Features

- Supports multiple output configurations
  - 2 × 80W, BTL Mode(4Ω, 26V, THD+N=10%)
  - 2 × 65W, BTL Mode(4Ω, 26V, THD+N=1%)
  - 2 × 74W, BTL Mode(6Ω, 30V, THD+N=10%)
  - 2 × 63W, BTL Mode(6Ω, 30V, THD+N=1%)
  - 1 × 151W, PBTL Mode(3Ω, 30V, THD+N=10%)
  - 1 × 131W, PBTL Mode(3Ω, 30V, THD+N=1%)
- Flexible audio I/O:
  - Supports 32, 44.1, 48, 88.2, 96, 192kHz sample rates
  - I^2S, LJ, RJ, 4- 16 channels TDM input
  - SDOUT for audio monitoring, sub-channel, or echo cancellation
  - Supports 3-wire digital audio interface (no MCLK required)
- High-efficiency Class-D modulation
  - > 90% power efficiency, 70mΩ R_{DS}on
- Excellent audio performance:
  - THD+N ≤ 0.03% at 1 W, 1kHz, PVDD = 12V
  - SNR ≥ 110dB (A-weighted), ICN ≤ 40μVrms
- Flexible processing features
  - 3-Band advanced DRC + 2 EQs + AGL + 2 EQs
  - 15 BQs per channel, level meter
  - 96kHz, 192kHz processor sampling
  - Mixer, volume, dynamic EQ, output crossbar
  - PVDD sensing and Class-H algorithm audio signal tracking
  - Rattle suppression, Frequency limiter
- Flexible power supply configurations
  - PVDD: 4.5V to 30V
  - DVDD and I/O: 1.8V or 3.3V
- Excellent integrated self-protection:
  - Over-current error (OCE)
  - Cycle-by-cycle current limit supports 4 selectable OC levels
  - Over-temperature warning (OTW)
  - Over-temperature error (OTE)
  - Under and over-voltage lock-out (UVLO/OVLO)
  - PVDD voltage drop detection
- Easy system integration
  - I^2C Software Control (TAS5830 supports both Fast and Fast Plus mode) or Hardware Mode
  - Fewer passives required compared to open-loop devices

2 Applications

- Battery-powered speaker
- Wireless bluetooth speakers
- Soundbars and subwoofers
- Smart speaker

3 Description

The TAS5830 is a stereo high-performance, closed-loop Class-D with integrated audio processor and up to 192kHz audio support.

After startup with Software Control Mode, TAS5830 not only implements classic BQs, 3-Band DRC, AGL, but also proprietary audio envelope tracking Class-H control algorithm. The Class-H algorithm detects the required audio power demand and provides a PWM format control signal to the DC-DC converter via the GPIO pin. The TAS5830 supports a delay buffer up to 5ms in BTL mode or 10ms in PBTL mode, Class-H control significantly helps to increase the system efficiency.

When setting the device into Hardware control mode, TAS5830 supports selecting switching frequency, analog gain, BTL/PBTL mode and cycle by cycle current limit threshold through pin configuration. This mode is designed to eliminate end system software driver integration efforts.

The TAS5830 also provides the DSP features Rattle suppression and Frequency limiter. Rattle suppression reduces the gain of the signal at frequencies that cause rattle through interaction with the speaker enclosure, improving sound quality. The frequency limiter process senses the input level, limits the gain of EQ dynamically and helps SPL without phase change.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TAS5830	TSSOP (32) DAD	11.00mm × 6.20mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

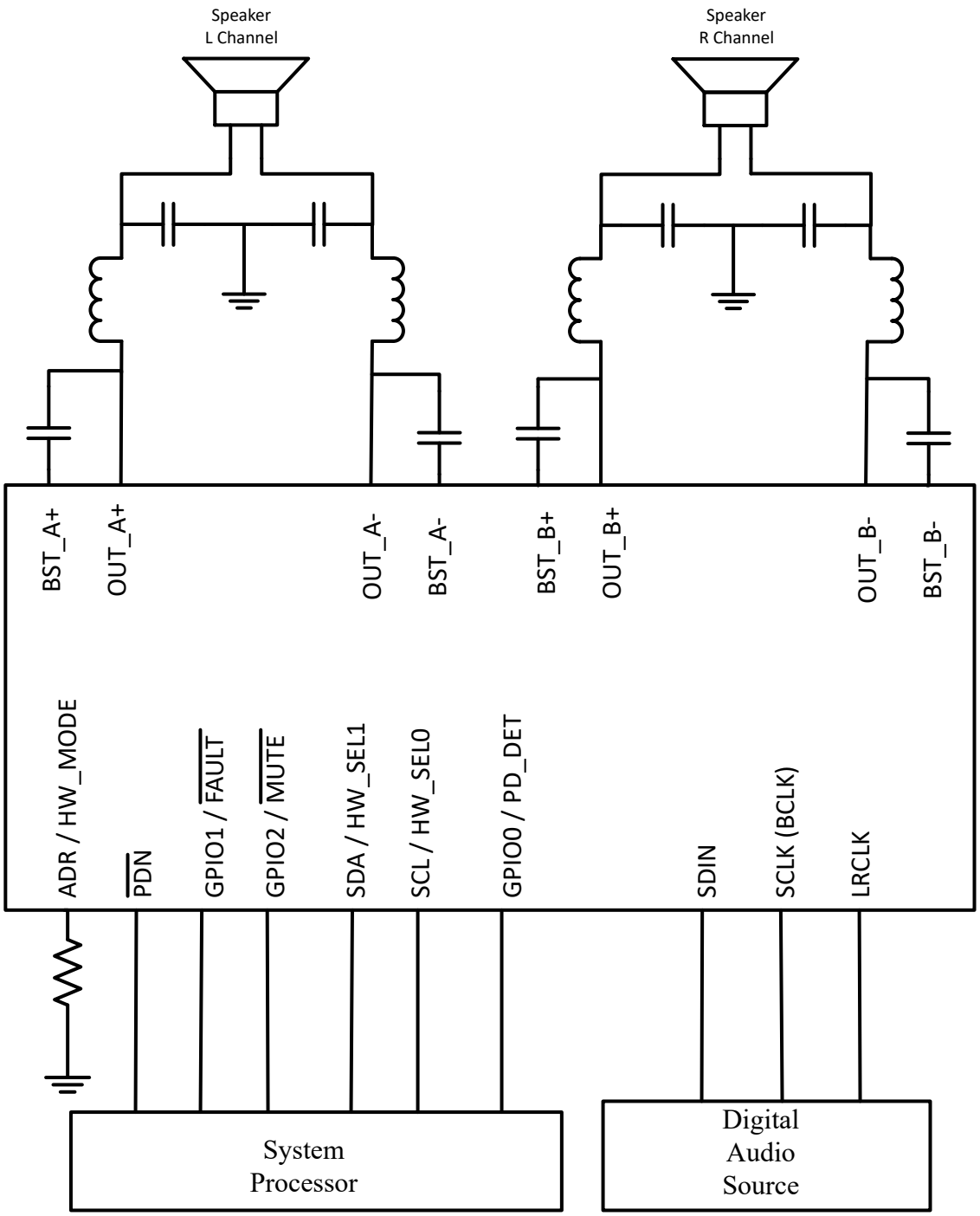


Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....7
5.1 Absolute Maximum Ratings....7
5.2 ESD Ratings....7
5.3 Recommended Operating Conditions....7
5.4 Thermal Information....7
5.5 Electrical Characteristics....8
5.6 Timing Requirements....12
5.7 Typical Characteristics....13
6 Detailed Description....27
6.1 Overview....27
6.2 Functional Block Diagram....28
6.3 Feature Description....29
6.4 Device Functional Modes....33
7 Register Maps....46
7.1 reg_map Registers....46
8 Application and Implementation....95
8.1 Typical Applications....96
8.2 Power Supply Recommendations....97
8.3 Layout....99
9 Device and Documentation Support....105
9.1 Device Support....105
9.2 Receiving Notification of Documentation Updates....105
9.3 Support Resources....105
9.4 Trademarks....106
9.5 Electrostatic Discharge Caution....106
9.6 Glossary....106
10 Revision History....106

4 Pin Configuration and Functions

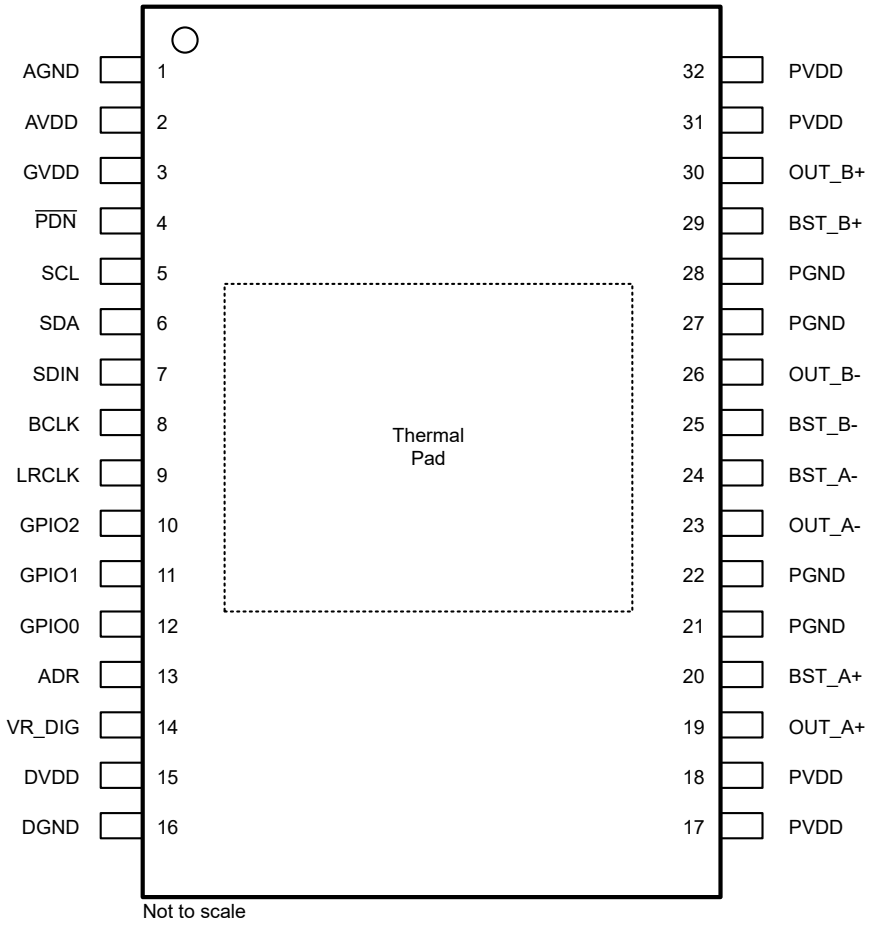


Figure 4-1. DAD (TSSOP) Package, 32-Pin PadUp, Software Mode, Top View

Table 4-1. Pin Functions - Software Mode

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog ground.
AVDD	2	P	Internally regulated 5V analog supply voltage. This pin must not be used to drive external devices.
GVDD	3	P	Gate drive internal regulator output. This pin must not be used to drive external devices.
$\overline{PDN}$	4	DI	Power down, active-low. $\overline{PDN}$ place the amplifier in Shutdown, turn off all internal regulators.
SCL	5	DI	I^2C serial control clock input.
SDA	6	DI/O	I^2C serial control data interface input/output.
SDIN	7	DI	Data line to the serial data port.
BCLK	8	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
LRCLK	9	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
GPIO2	10	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x62h). Can be configured to be open drain output or push-pull output.
GPIO1	11	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x61h). Can be configured to be open drain output or push-pull output.
GPIO0	12	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x63h). Can be configured to be open drain output or push-pull output.
ADR	13	AI	A table of resistor value (Pull down to GND) decides the device I2C address. See Section 6.4.7.3.
VR_DIG	14	P	Internally regulated 1.5V digital supply voltage. This pin must not be used to drive external devices.
DVDD	15	P	3.3V or 1.8V digital power supply.
DGND	16	G	Digital ground.
PVDD	17	P	PVDD voltage input.
	18	P	
	31	P	
	32	P	
PGND	21	G	Ground reference for power device circuitry. Connect this pin to system ground.
	22	G	
	27	G	
	28	G	
OUT_A+	19	O	Positive pin for differential speaker amplifier output A.
BST_A+	20	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+.
OUT_A-	23	O	Negative pin for differential speaker amplifier output A.
BST_A-	24	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-.
BST_B-	25	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-.
OUT_B-	26	O	Negative pin for differential speaker amplifier output B.
BST_B+	29	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+.
OUT_B+	30	O	Positive pin for differential speaker amplifier output B.
PowerPAD™		P	Ground, connect to grounded heat sink for best system performance.

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), PO = Positive output, NO = Negative output, P = Power, G = Ground (0V)

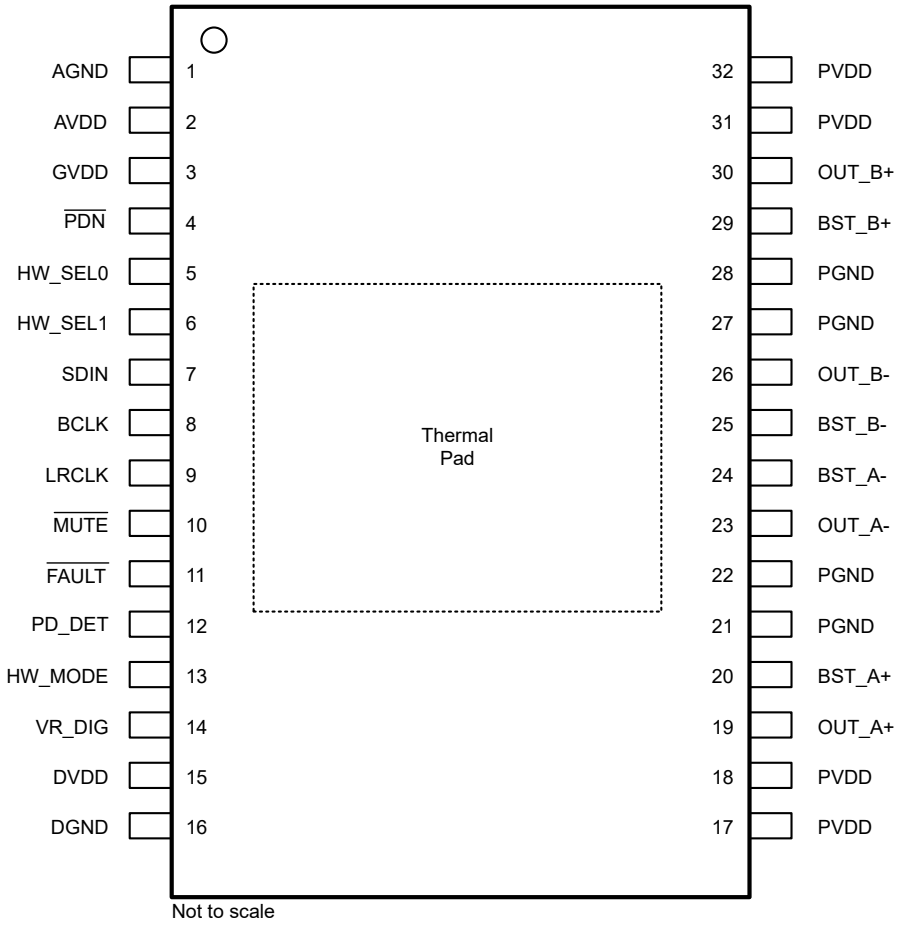


Figure 4-2. DAD (TSSOP) Package, 32-Pin PadUp, Hardware Mode, Top View

Table 4-2. Pin Functions - Hardware Mode

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog ground.
AVDD	2	P	Internally regulated 5V analog supply voltage. This pin must not be used to drive external devices.
GVDD	3	P	Gate drive internal regulator output. This pin must not be used to drive external devices.
PDN	4	DI	Power down, active-low. PDN place the amplifier in Shutdown, turn off all internal regulators.
HW_SEL0	5	DI	Analog gain and BTL/PBTL mode selection in Hardware Mode . Pull up to DVDD or Pull down to ground with different resistor. See Section 6.4.7.2.
HW_SEL1	6	DI	PWM Switching Frequency and Spread Spectrum Enable/Disable selection in Hardware Mode. Pull up to DVDD or Pull down to ground with different resistor. See Section 6.4.7.2.
SDIN	7	DI	Data line to the serial data port.
BCLK	8	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
LRCLK	9	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
MUTE	10	DI	Speaker amplifier Mute. Which must be pulled low (connect to DGND) to MUTE the device and pulled high (connected to DVDD) to exit MUTE state. In Mute state, device output keep in Hi-Z state.
FAULT	11	DO	Fault terminal,which is pulled LOW when an internal fault occurs.
PD_DET	12	DO	PVDD Drop detection, which is pulled LOW when the PVDD drop below 8V.
HW_MODE	13	AI	Connect to DVDD directly to ensure device enter into Hardware Control Mode.
VR_DIG	14	P	Internally regulated 1.5V digital supply voltage. This pin must not be used to drive external devices.
DVDD	15	P	3.3V or 1.8V digital power supply.
DGND	16	G	Digital ground.

Table 4-2. Pin Functions - Hardware Mode (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
PVDD	17	P	PVDD voltage input.
	18	P	
	31	P	
	32	P	
PGND	21	G	Ground reference for power device circuitry. Connect this pin to system ground.
	22	G	
	27	G	
	28	G	
OUT_A+	19	O	Positive pin for differential speaker amplifier output A.
BST_A+	20	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+.
OUT_A-	23	O	Negative pin for differential speaker amplifier output A.
BST_A-	24	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-.
BST_B-	25	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-.
OUT_B-	26	O	Negative pin for differential speaker amplifier output B.
BST_B+	29	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+.
OUT_B+	30	O	Positive pin for differential speaker amplifier output B.
PowerPAD™		P	Ground, connect to grounded heat sink for best system performance.

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), PO = Positive output, NO = Negative output, P = Power, G = Ground (0V)

5 Specifications

5.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	35	V
$V_{I(DigIn)}$	DVDD referenced digital inputs(2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK\_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
T_A	Ambient operating temperature	–40	85	°C
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SDIN, SDOUT, SCL, SDA, $\overline{\text{PDN}}$

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002.(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	PVDD	4.5		30	V
		DVDD	1.62		3.63	V
R_{SPK}	Minimum Speaker Load	4.5V-30V Operating PVDD Range, BTL Mode	3.2			Ω
		4.5V-30V Operating PVDD Range, PBTL Mode	1.6			Ω
$V_{IH(DigIn)}$	Input logic high for DVDD referenced digital inputs		0.9 × V_{DVDD}		DVDD	V
$V_{IL(DigIn)}$	Input logic low for DVDD referenced digital inputs				0.1 × V_{DVDD}	V
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1			µH

5.4 Thermal Information

THERMAL METRIC(1)		TAS5830 - TSSOP32 (DAD) - 32 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
$R_{\theta JA(top)}$	Junction-to-ambient thermal resistance	60.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = V_{DVDD}$			10	uA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)}$ = 0 V			–10	uA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	I_{OH} = 4 mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	I_{OH} = –4 mA			20%	V_{DVDD}
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode		400	1000	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required LRCLK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		192	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
AMPLIFIER OPERATING MODE AND DC PRAMETERS						
t_{off}	Turn-off Time	Play to Shutdown, HiZ, Sleep, or Deep Sleep. Excluding volume ramp.		4.35		ms
t_{wake}	Wake up time	Deep sleep to Play. Excluding volume ramp.		2.4		ms
t_{wake}	Wake up time	Sleep to Play. Excluding volume ramp.		2.3		ms
t_{wake}	Wake up time	Hi-Z to Play. Excluding volume ramp.		70		µs
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V, Play mode, General Audio Process flow with full DSP running		24		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V, Sleep mode		1		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V, Deep Sleep mode		1		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 0.8 V, DVDD = 3.3 V, Shutdown mode		18		uA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 24 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, 1SPW Modulation, Play Mode		35		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 24 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Output Hiz Mode		11		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 24 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Sleep Mode		7.5		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 24 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Deep Sleep Mode		10		uA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 24 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Shutdown Mode		10		uA

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD Measured at 0 dB input(1FS)	14.9		30.4	dBV
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain = 30.4dBV		0.5		dB
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Software Mode		384		kHz
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Software Mode		480		kHz
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Software Mode		576		kHz
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Software Mode		768		kHz
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Hardware Mode		480		kHz
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Hardware Mode		768		kHz
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization. V_{PVDD} = 24V, $I_{(OUT)}$ = 500mA, T_J=25℃		70		mΩ
Efficiency(BTL)	The efficiency of low power playing(Power stage efficiency)	PVDD = 24V, LC filter = 10 µH + 0.68 µF, F_{SW} = 384 kHz, 1SPW Modulation, Load = 4Ω, playing 1W output power on each channel		53		%
Efficiency(PBTL)	The efficiency of larger power playing(Power stage efficiency)	PVDD = 24V, LC filter = 10 µH + 0.68 µF, F_{SW} = 384 kHz, 1SPW Modulation, Load = 3Ω, playing 120W output power		92		%
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold (Speaker current)	Speaker Output Current (Post LC filter), Speaker current, LC Filter=10uH+0.68uF, BTL Mode	7.5	8	8.5	A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold			4	4.25	V
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold		30.5	32		V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		3.2		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		640		ms
OTE_{THRES}	Over temperature error threshold			179		℃
$OTE_{Hystersis}$	Over temperature error hysteresis			11		℃
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit0		106		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit1		130		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit2		143		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit3		156		°C

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMACNE (STEREO BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 30.4dBV analog gain, V_{PVDD} range: 12V~30V	–5		5	mV
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 KHz)	V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, Load = 4Ω		0.015		%
		V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, Load = 8Ω		0.015		%
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, R_{SPK} = 4Ω, f = 1kHz, THD+N = 10%		80		W
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, R_{SPK} = 4Ω, f = 1kHz, THD+N = 1%		65		W
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, R_{SPK} = 8Ω, f = 1kHz, THD+N = 10%		41		W
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, R_{SPK} = 8 Ω, f = 1kHz, THD+N = 1%		33		W
$ICN_{(SPK)}$	Idle channel noise(Aweighted, AES17)	V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, Load = 4Ω, Fsw = 576kHz, BD Modulation		40		µVrms
		V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, Load = 4Ω, Fsw = 384kHz, 1SPW Modulation		37		µVrms
		V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, Load = 8Ω, Fsw = 576kHz, BD Modulation		42		µVrms
		V_{PVDD} = 26V, LC Filter = 10uH + 0.68uF, Load = 8Ω, Fsw = 384kHz, 1SPW Modulation		40		µVrms
DR	Dynamic range	A-Weighted, -60 dBFS method. V_{PVDD} = 24V, Load = 6Ω Analog Gain = 30.4dBV		111		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD} = 24V, Load = 6Ω		111		dB
		A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD} = 18V, Load = 4Ω		108		dB
PSRR	Power supply rejection ratio	Injected Noise = 1kHz, 1Vrms, V_{PVDD} = 26V, Input audio signal = digital zero		73		dB
$X\text{-}talk_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1kHz, based on Inductor (DFEG7030D-4R7) from Murata		100		dB

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE (MONO PBTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 30.4dBV Analog gain, V_{PVDD} = 12V-30V range, 1SPW mode	–5		5	mV
$P_{O(SPK)}$	Output Power	V_{PVDD} = 29V, R_{SPK} = 3Ω, f = 1kHz, THD+N = 1%		123		W
		V_{PVDD} = 29V, R_{SPK} = 3Ω, f = 1kHz, THD+N = 10%		148		W
		V_{PVDD} = 24V, R_{SPK} = 2Ω, f = 1kHz, THD+N = 1%		119		W
		V_{PVDD} = 24V, R_{SPK} = 2Ω, f = 1kHz, THD+N = 10%		141		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 KHz)	V_{PVDD} = 24V, LC-filter = 10uH + 0.68uF, R_{SPK} = 2Ω		0.05		%
		V_{PVDD} = 29V, LC-filter = 10uH + 0.68uF, R_{SPK} = 3Ω		0.07		%
DR	Dynamic range	A-Weighted, -60 dBFS method, V_{PVDD} = 29V, R_{SPK} = 3Ω.		109		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD} = 29V, R_{SPK} = 3Ω		109		dB
		A-Weighted,referenced to 1% THD+N Output Level, V_{PVDD} = 24V, R_{SPK} = 2Ω		108		dB
PSRR	Power supply rejection ratio	Injected Noise = 1kHz, 1Vrms, V_{PVDD} = 18V, input audio signal = digital zero		70		dB

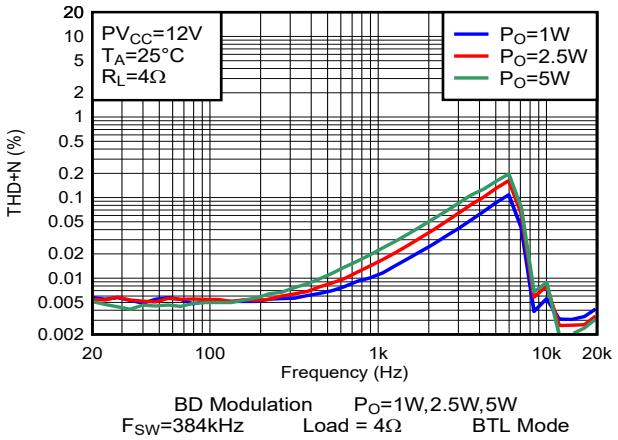
5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing - Target Mode					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCLK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I^2C Bus Timing – Fast Plus					
f_{SCL}	SCL clock frequency			1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs
t_{LOW}	Low period of the SCL clock	0.5			µs
t_{HI}	High period of the SCL clock	0.26			µs
t_{RS-SU}	Setup time for (repeated) START condition	0.26			µs
t_{S-HD}	Hold time for (repeated) START condition	0.26			µs
t_{D-SU}	Data setup time	50			ns
t_{D-HD}	Data hold time	0			ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		120	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		120	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		120	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		120	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		120	ns
t_{P-SU}	Setup time for STOP condition	0.26			µs
C_b	Capacitive load for each bus line			400	pf
I^2C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated)START condition	600			ns
t_{RS-HD}	Hold time for (repeated)START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_b	Capacitive load for each bus line			400	pf

5.7 Typical Characteristics

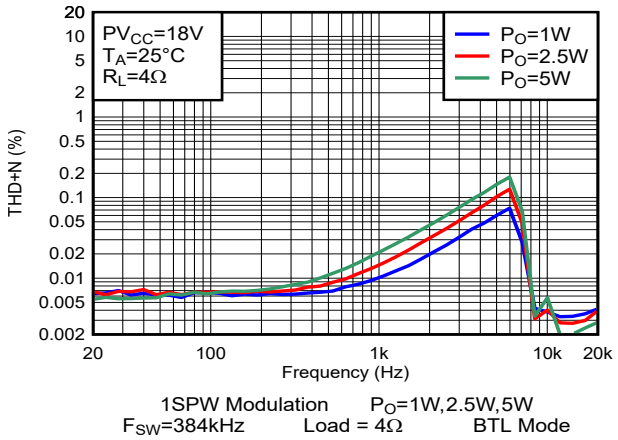
5.7.1 Bridge Tied Load (BTL) Configuration Curves with BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Amplifier Loop Bandwidth, LC filter with 10µH / 0.68µF, unless otherwise noted.



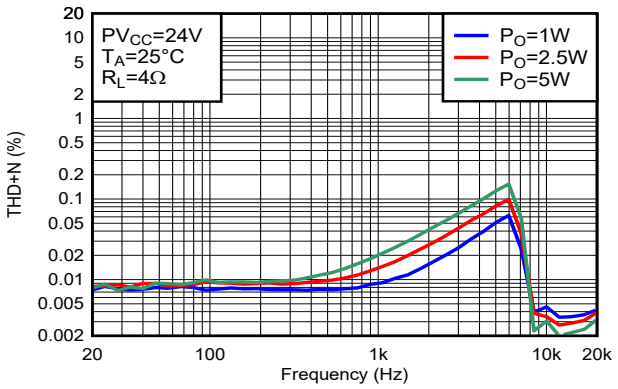
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-1. THD+N vs Frequency-BTL



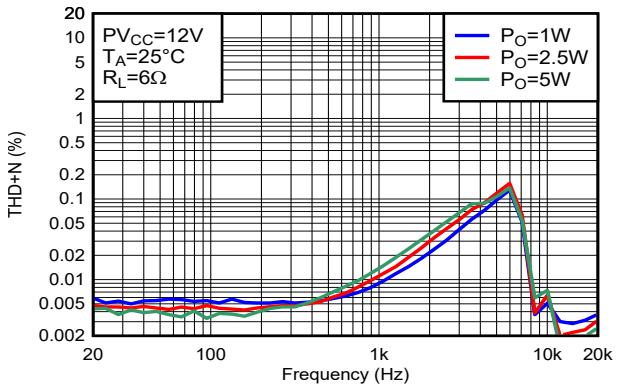
1SPW Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-2. THD+N vs Frequency-BTL



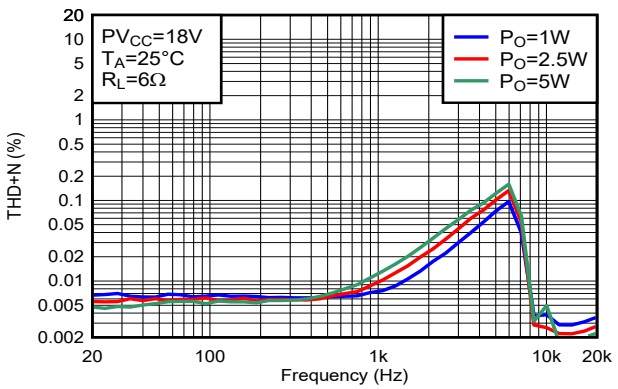
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-3. THD+N vs Frequency-BTL



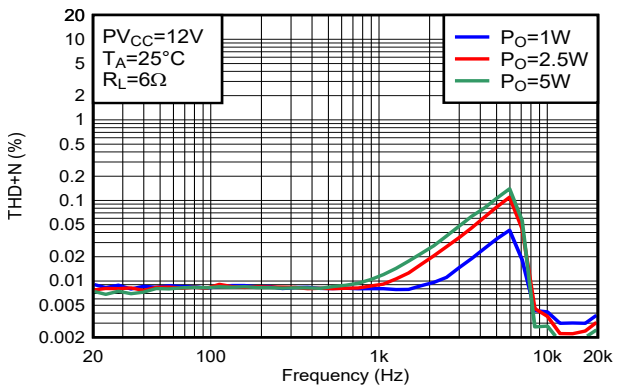
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-4. THD+N vs Frequency-BTL



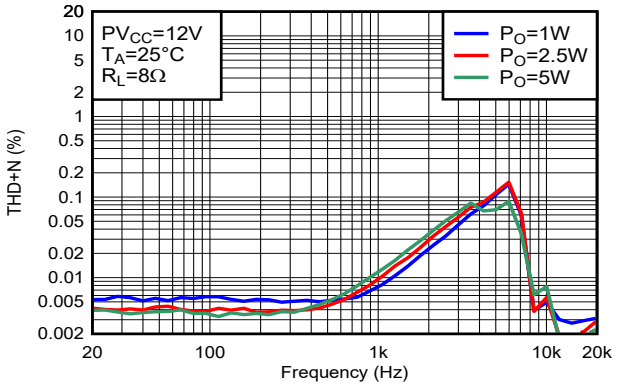
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-5. THD+N vs Frequency-BTL



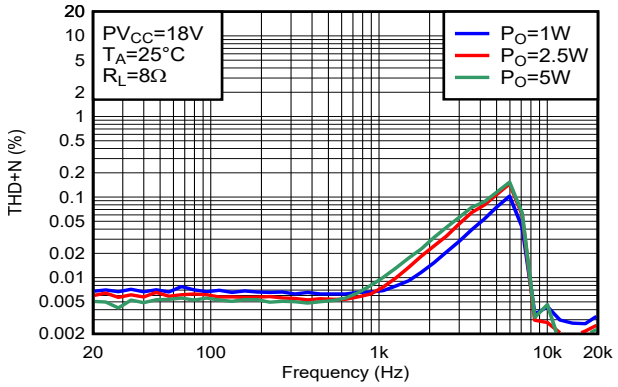
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-6. THD+N vs Frequency-BTL



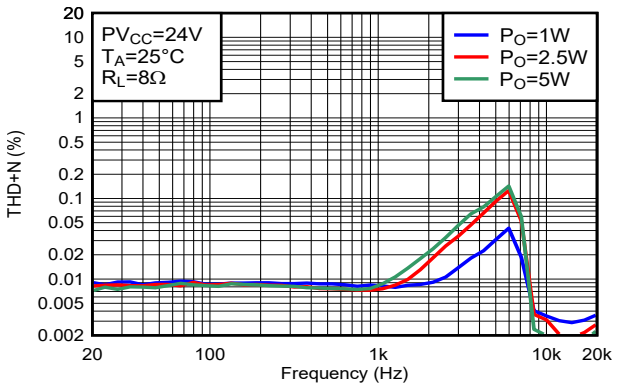
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 4Ω BTL Mode

Figure 5-7. THD+N vs Frequency-BTL



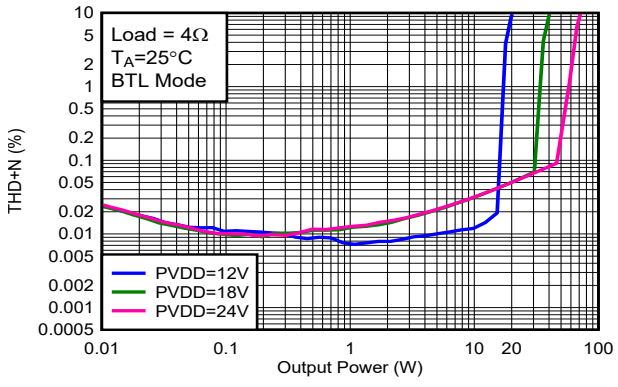
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 4Ω BTL Mode

Figure 5-8. THD+N vs Frequency-BTL



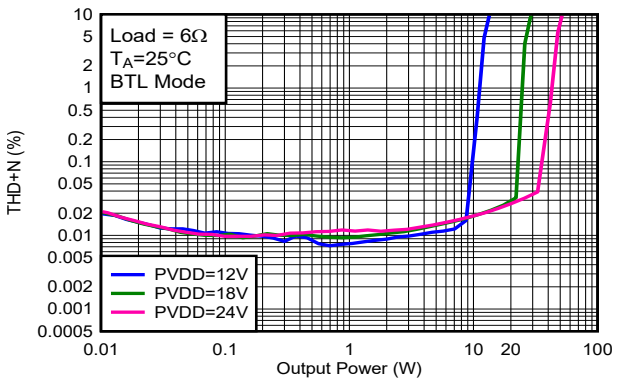
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 4Ω BTL Mode

Figure 5-9. THD+N vs Frequency-BTL



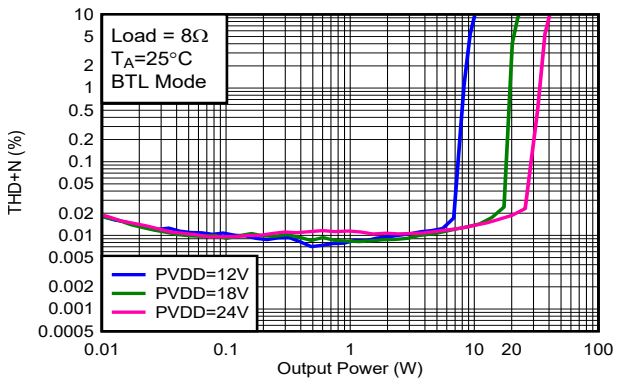
BD Modulation
FSW=384kHz PVDD = 12V, 18V, 24V BTL Mode

Figure 5-10. THD+N vs Output Power-BTL



BD Modulation
FSW=384kHz PVDD = 12V, 18V, 24V BTL Mode

Figure 5-11. THD+N vs Output Power-BTL



BD Modulation
FSW=384kHz PVDD = 12V, 18V, 24V BTL Mode

Figure 5-12. THD+N vs Output Power-BTL

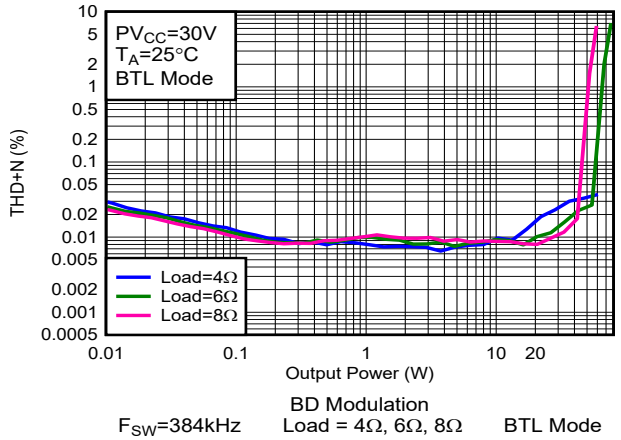


Figure 5-13. THD+N vs Power-BTL

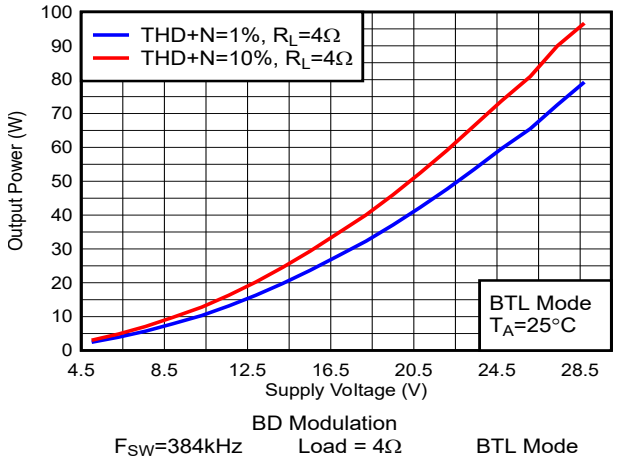


Figure 5-14. Output Power vs Supply Voltage

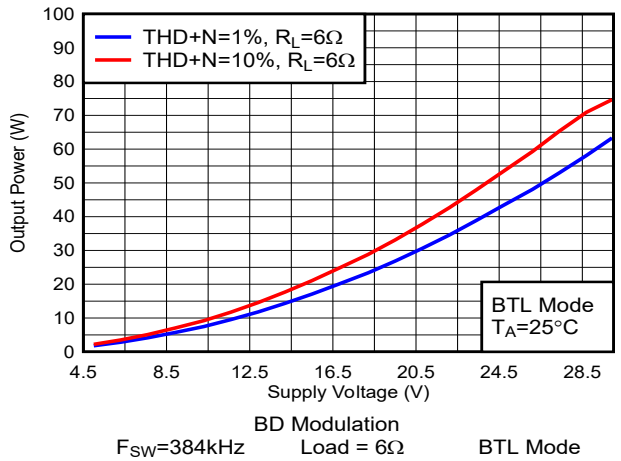


Figure 5-15. Output Power vs Supply Voltage

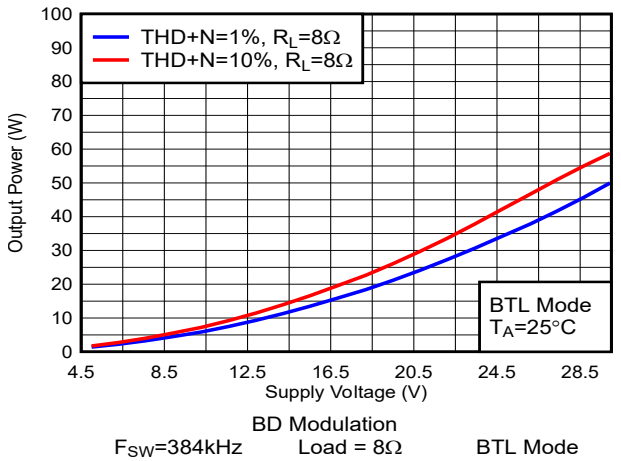


Figure 5-16. Output Power vs Supply Voltage

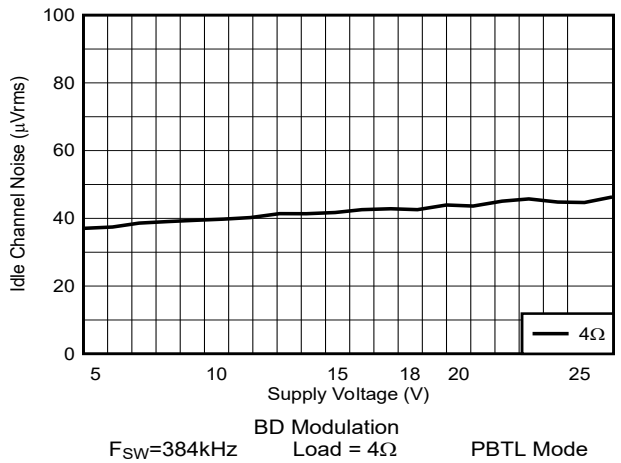


Figure 5-17. Idle Channel Noise vs Supply Voltage

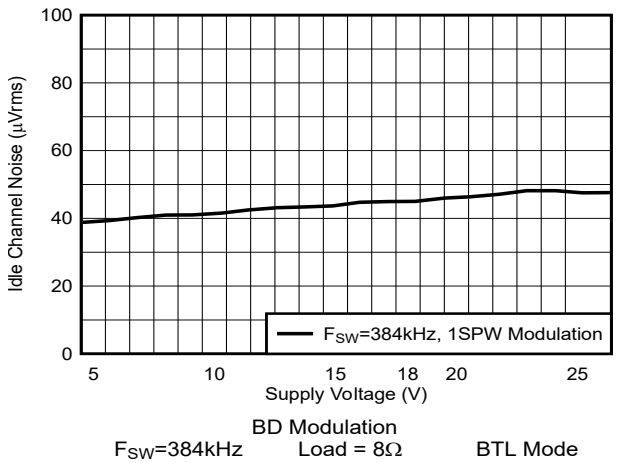
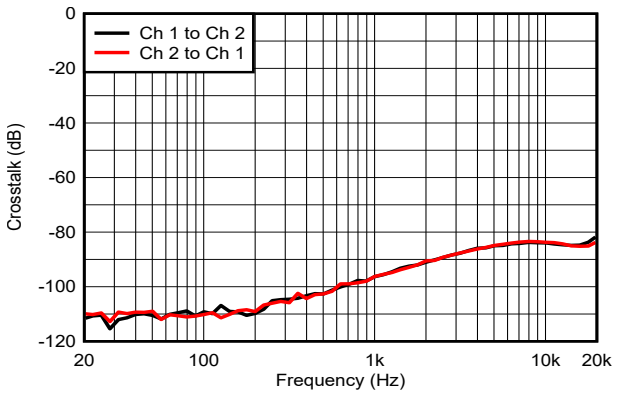
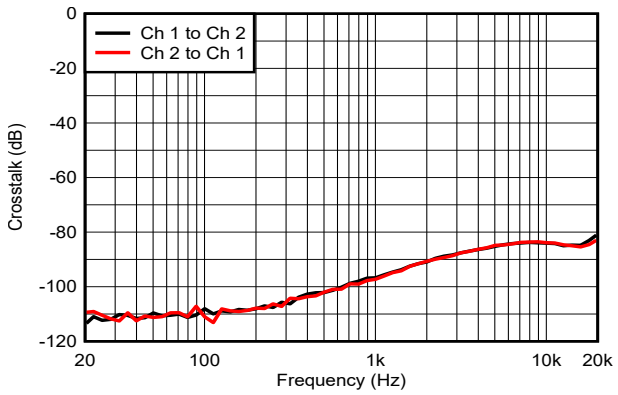


Figure 5-18. Idle Channel Noise vs Supply Voltage



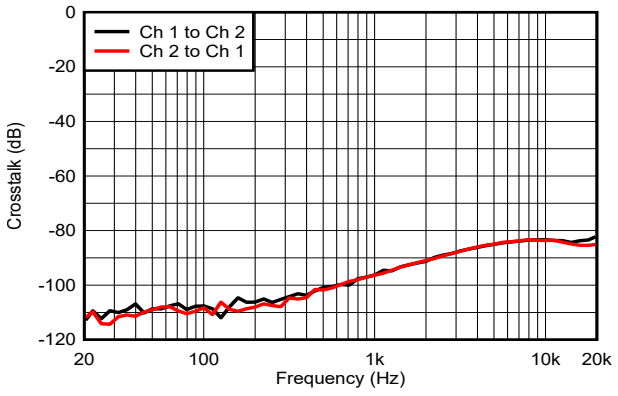
PVDD=12V
F_{SW}=384kHz
BD Modulation
Load = 4Ω
P_o=1W
BTL Mode

Figure 5-19. Crosstalk



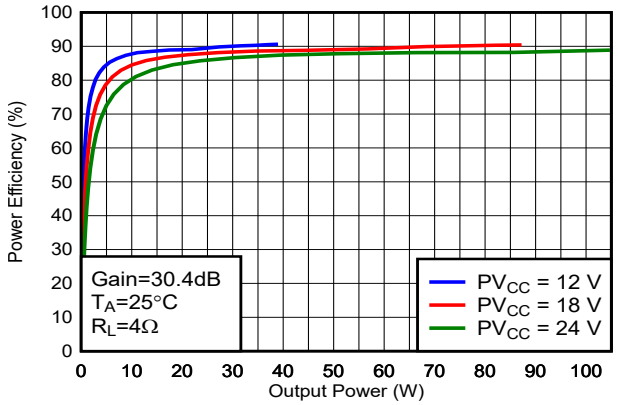
PVDD=18V
F_{SW}=384kHz
BD Modulation
Load = 4Ω
P_o=1W
BTL Mode

Figure 5-20. Crosstalk



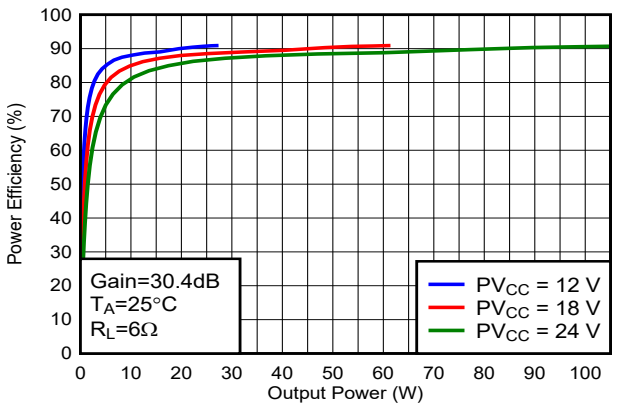
PVDD=24V
F_{SW}=384kHz
BD Modulation
Load = 4Ω
P_o=1W
BTL Mode

Figure 5-21. Crosstalk



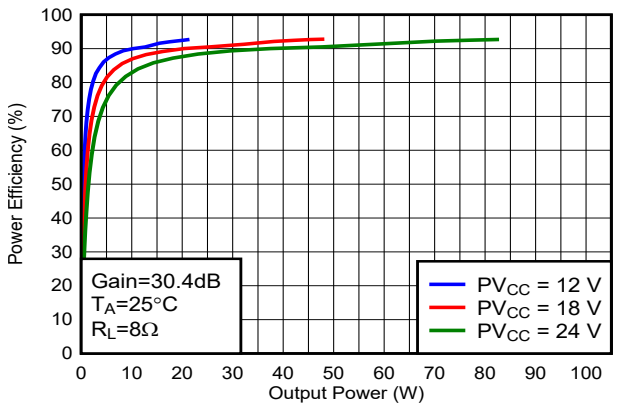
BD Modulation
F_{SW}=384kHz
Load = 4Ω
BTL Mode

Figure 5-22. Efficiency vs Output Power



BD Modulation
F_{SW}=384kHz
Load = 6Ω
BTL Mode

Figure 5-23. Efficiency vs Output Power



BD Modulation
F_{SW}=384kHz
Load = 8Ω
BTL Mode

Figure 5-24. Efficiency vs Output Power

5.7.2 Bridge Tied Load (BTL) Configuration Curves with 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Loop Bandwidth, the LC filter used was 10µH / 0.68µF, unless otherwise noted.

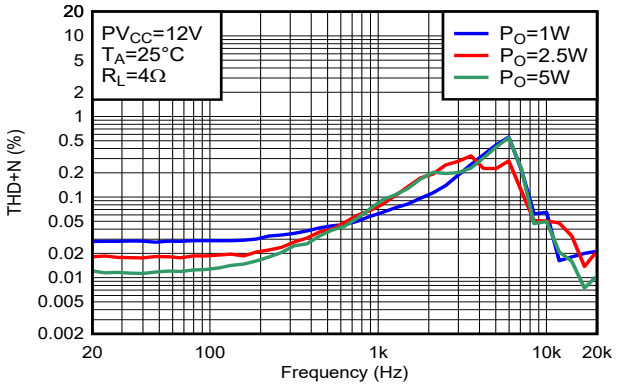


Figure 5-25. THD+N vs Frequency-BTL

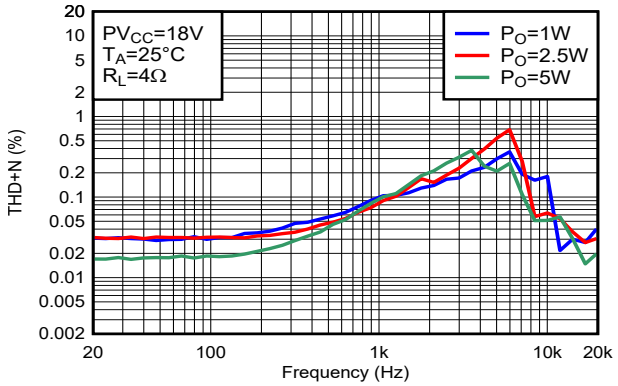


Figure 5-26. THD+N vs Frequency-BTL

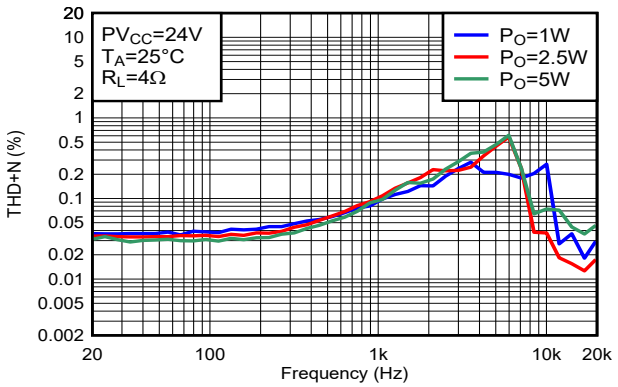


Figure 5-27. THD+N vs Frequency-BTL

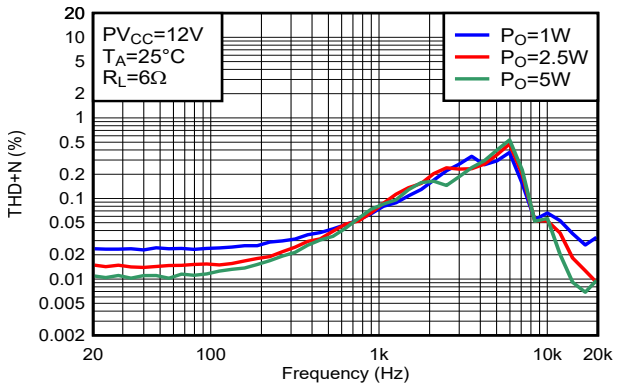


Figure 5-28. THD+N vs Frequency-BTL

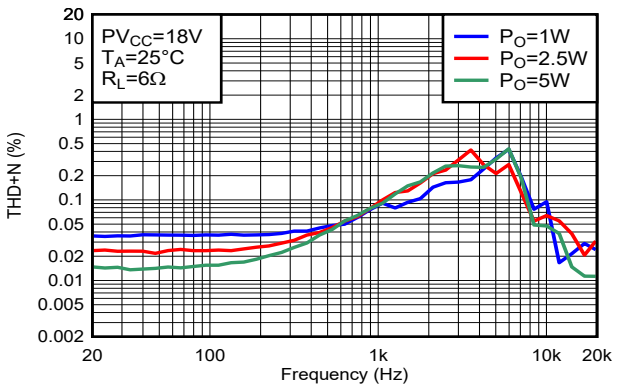


Figure 5-29. THD+N vs Frequency-BTL

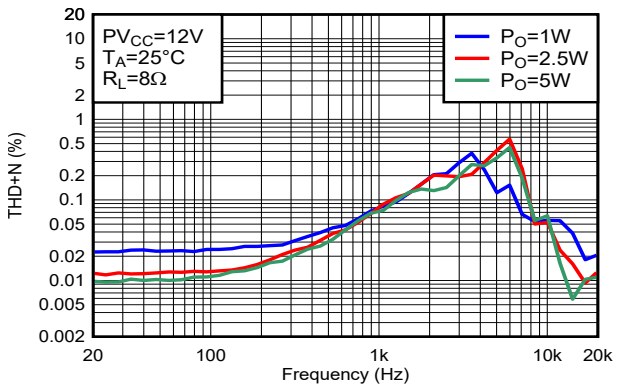


Figure 5-30. THD+N vs Frequency-BTL

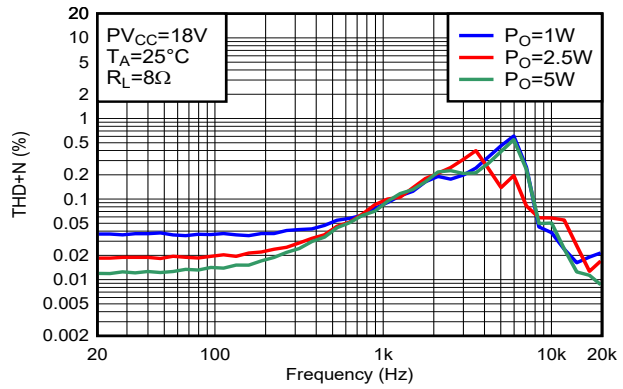


Figure 5-31. THD+N vs Frequency-BTL

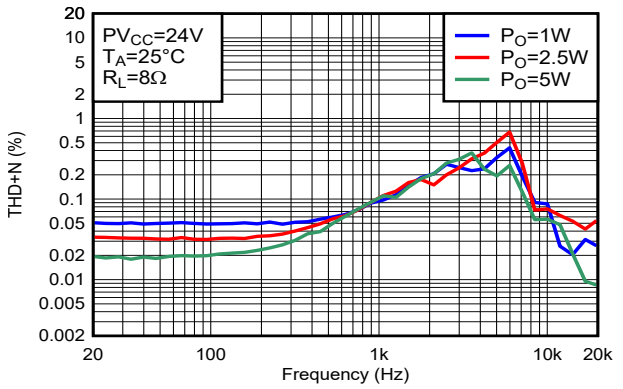


Figure 5-32. THD+N vs Frequency-BTL

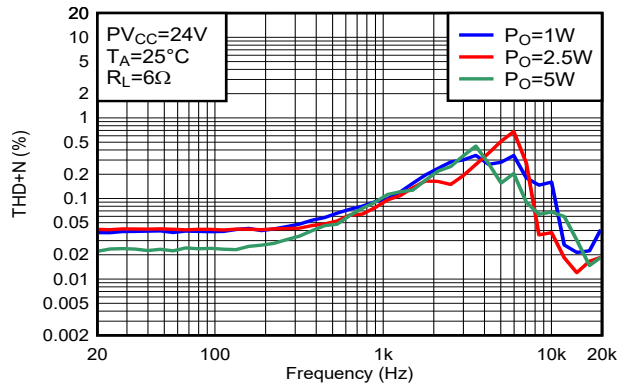


Figure 5-33. THD+N vs Frequency-BTL

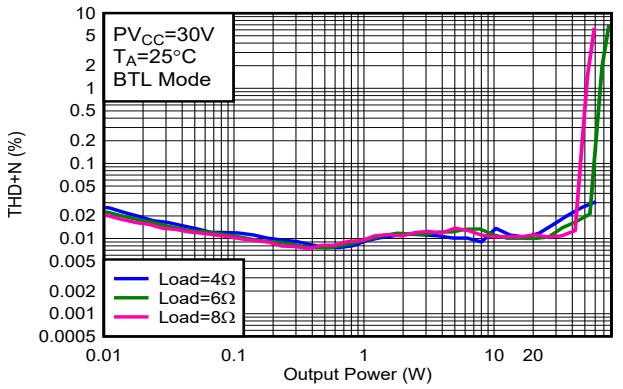


Figure 5-34. THD+N vs Power-BTL

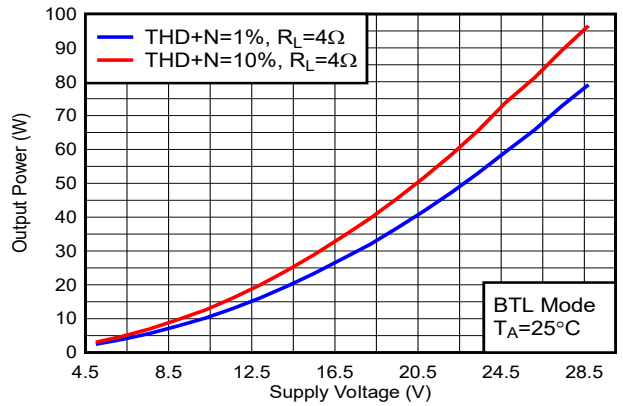


Figure 5-35. Output Power vs Supply Voltage

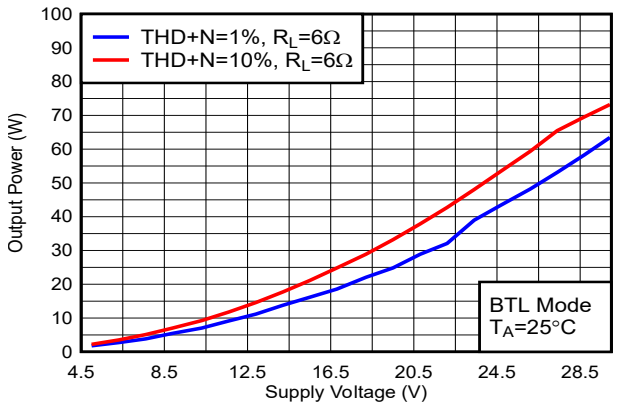
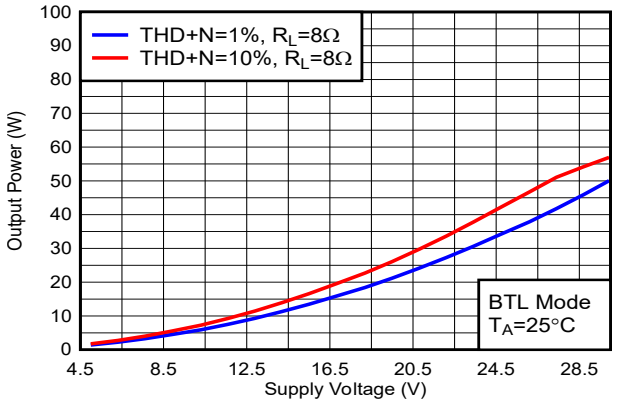
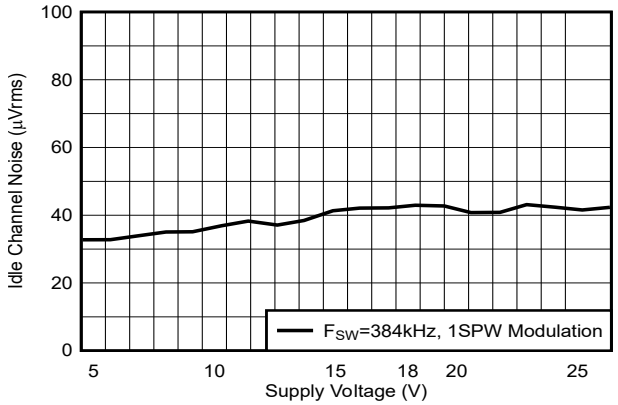


Figure 5-36. Output Power vs Supply Voltage



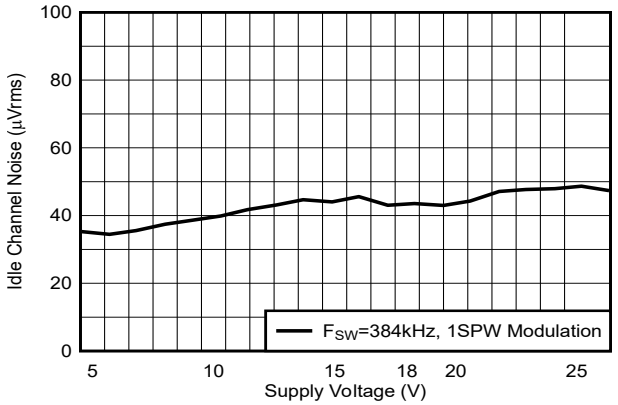
1SPW Modulation
F_{SW}=384kHz Load = 8Ω BTL Mode

Figure 5-37. Output Power vs Supply Voltage



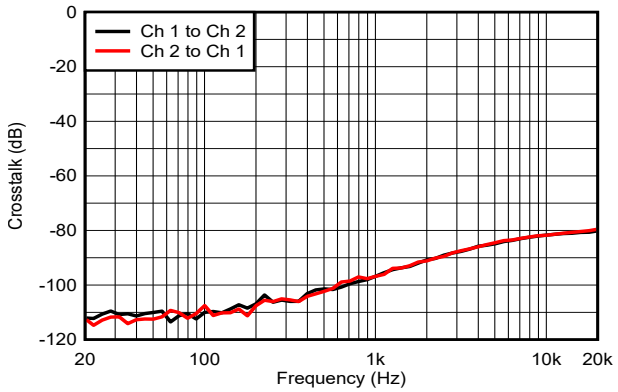
1SPW Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-38. Idle Channel Noise vs Supply Voltage



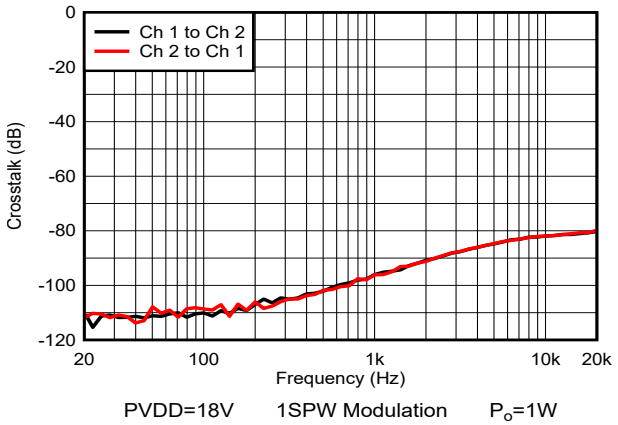
1SPW Modulation
F_{SW}=384kHz Load = 8Ω BTL Mode

Figure 5-39. Idle Channel Noise vs Supply Voltage



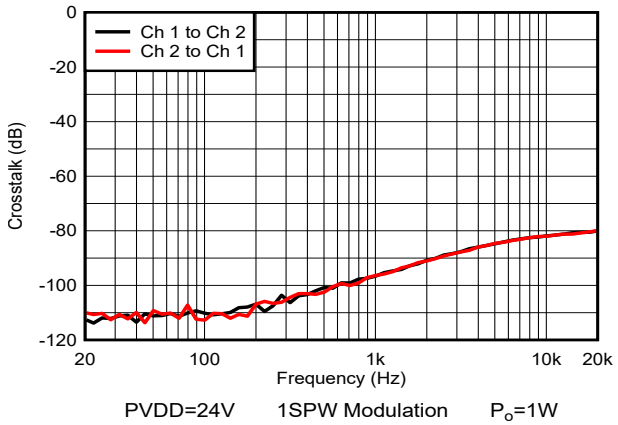
PVDD=12V 1SPW Modulation P_o=1W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-40. Crosstalk



PVDD=18V 1SPW Modulation P_o=1W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-41. Crosstalk



PVDD=24V 1SPW Modulation P_o=1W
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-42. Crosstalk

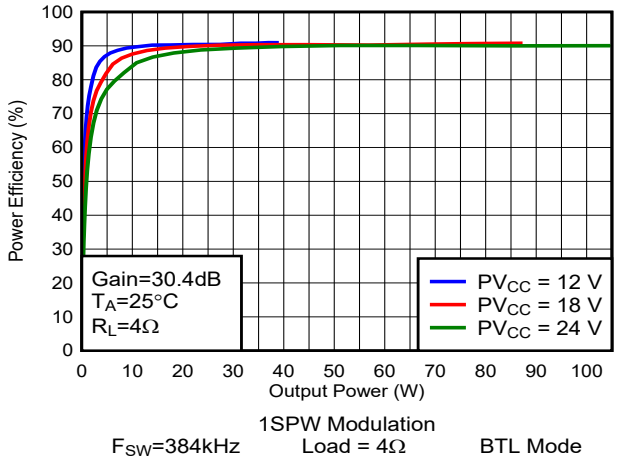


Figure 5-43. Efficiency vs Output Power

5.7.3 Parallel Bridge Tied Load (PBTL) Configuration With BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Amplifier Loop Bandwidth, LC filter with 10µH / 0.68µF (Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see details in Section 8.1.2) , unless otherwise noted.

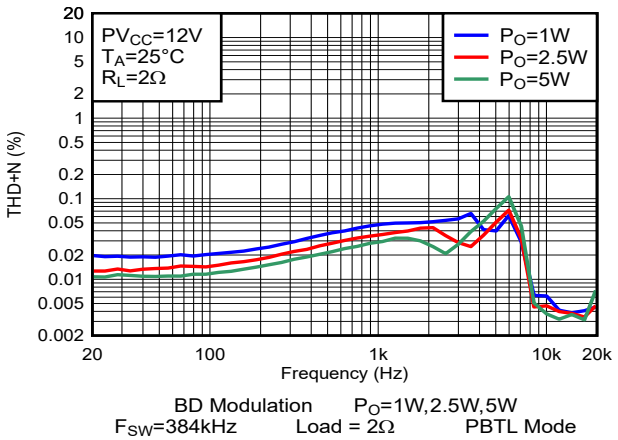


Figure 5-44. THD+N vs Frequency-PBTL

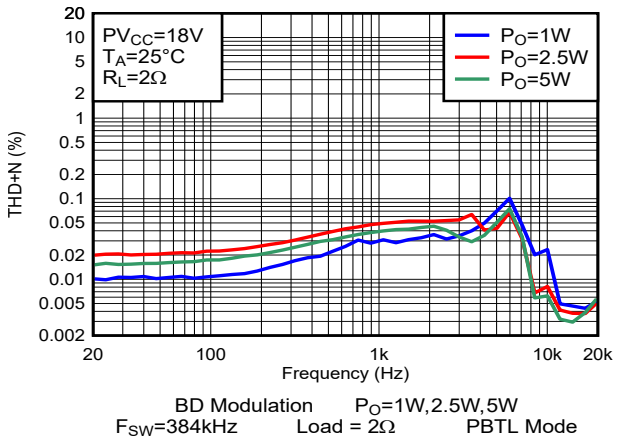


Figure 5-45. THD+N vs Frequency-PBTL

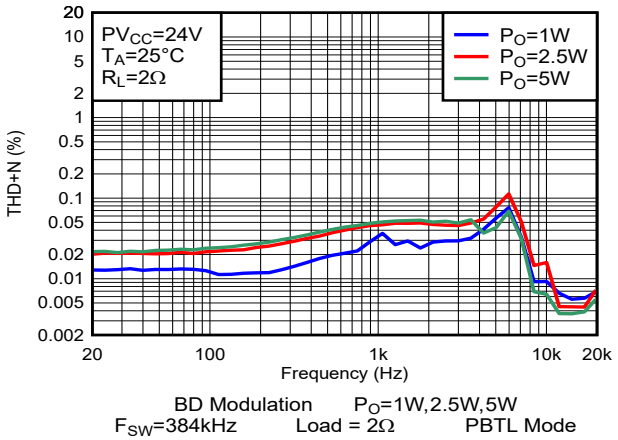


Figure 5-46. THD+N vs Frequency-PBTL

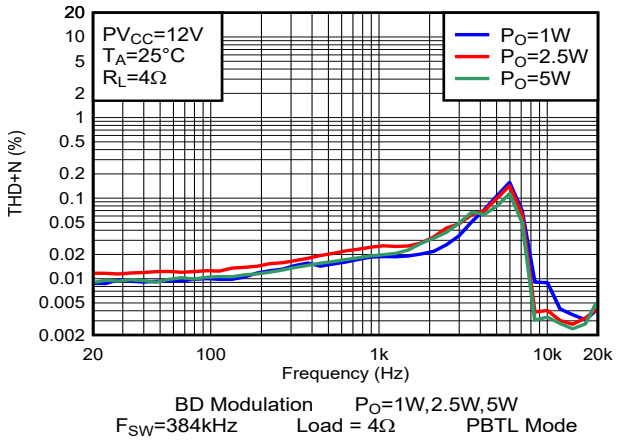


Figure 5-47. THD+N vs Frequency-PBTL

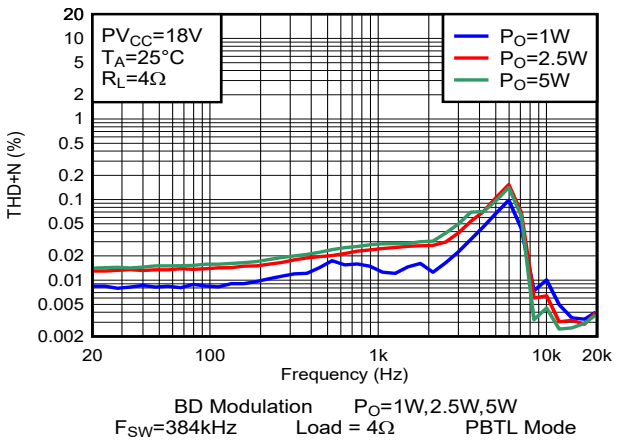


Figure 5-48. THD+N vs Frequency-PBTL

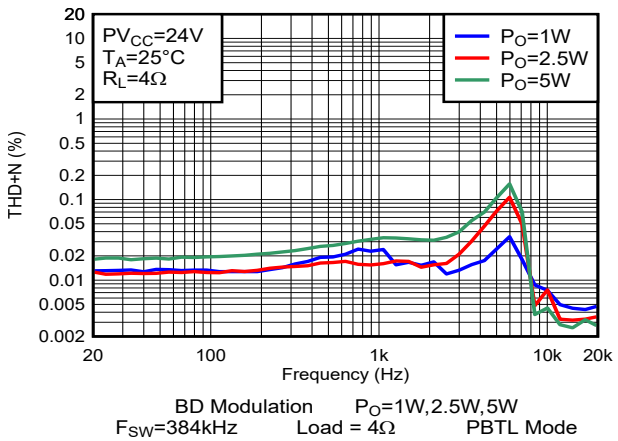


Figure 5-49. THD+N vs Frequency-PBTL

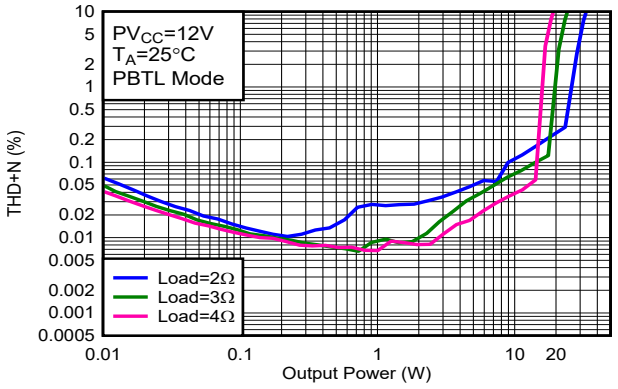


Figure 5-50. THD+N vs Output Power-PBTL

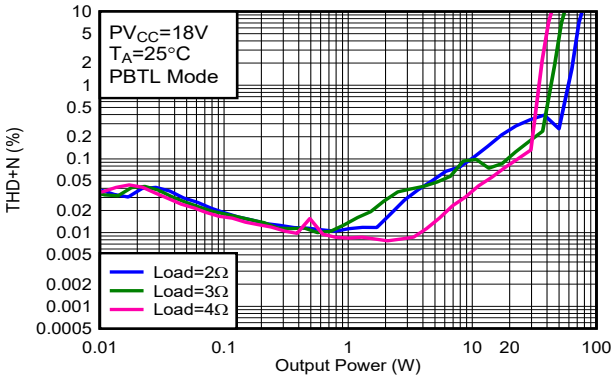


Figure 5-51. THD+N vs Output Power-PBTL

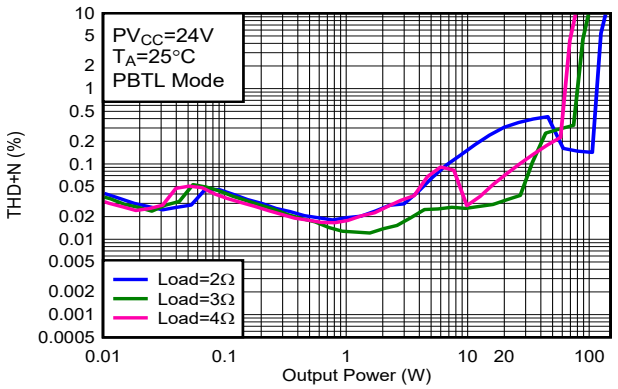


Figure 5-52. THD+N vs Output Power-PBTL

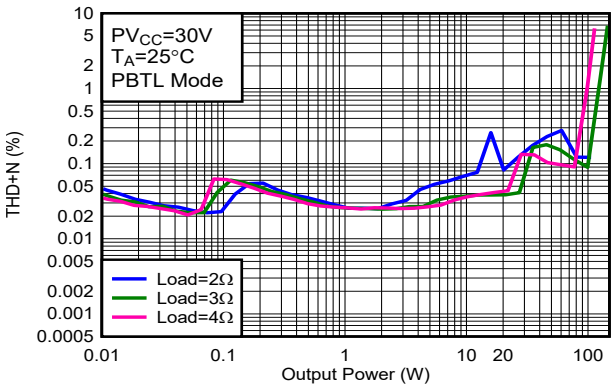
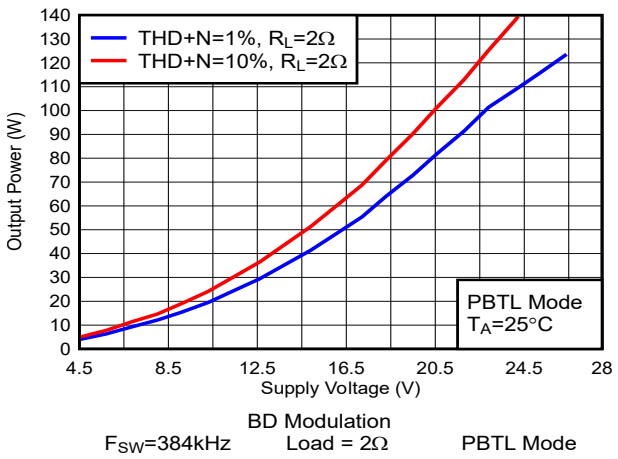


Figure 5-53. THD+N vs Power-PBTL



Dashed lines represent thermally limited region.

Figure 5-54. Output Power vs Supply Voltage

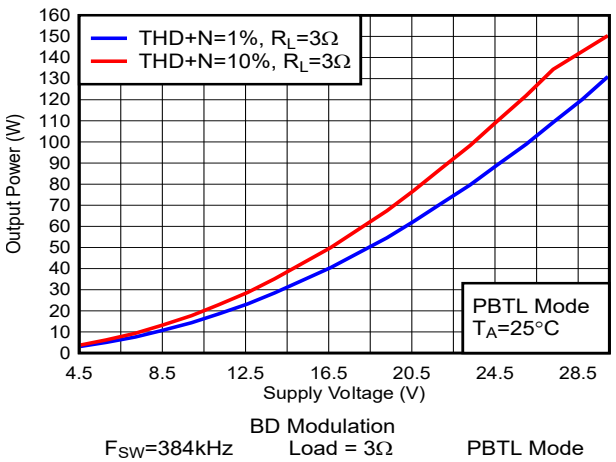


Figure 5-55. Output Power vs Supply Voltage

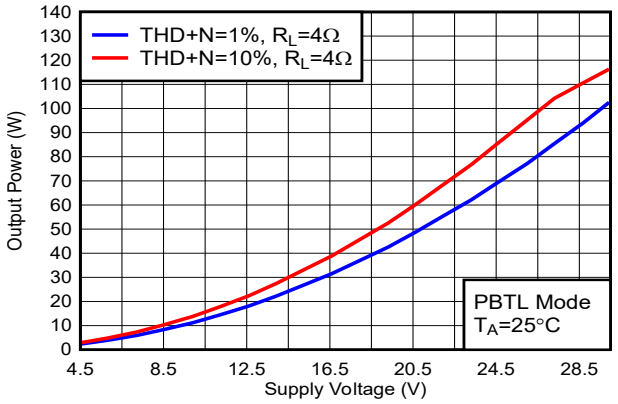


Figure 5-56. Output Power vs Supply Voltage

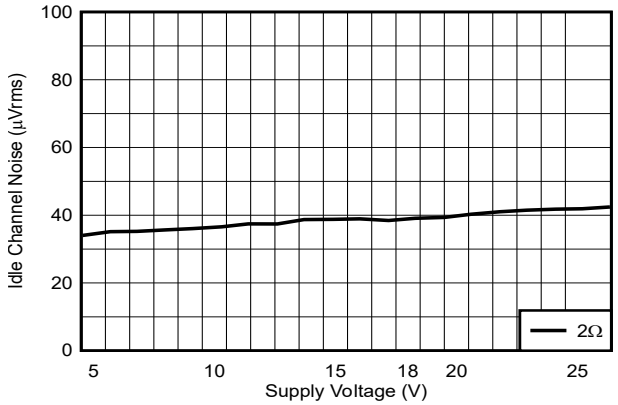


Figure 5-57. Idle Channel Noise vs Supply Voltage

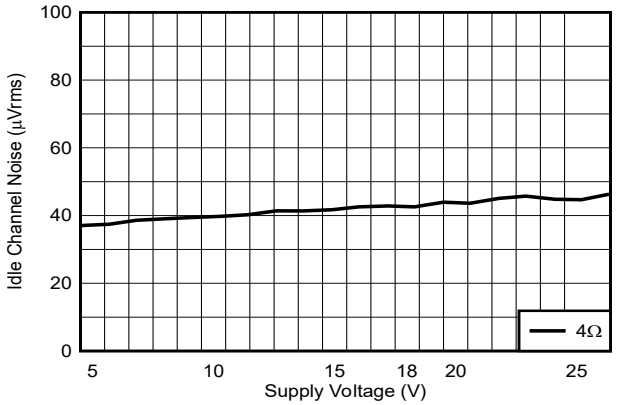


Figure 5-58. Idle Channel Noise vs Supply Voltage

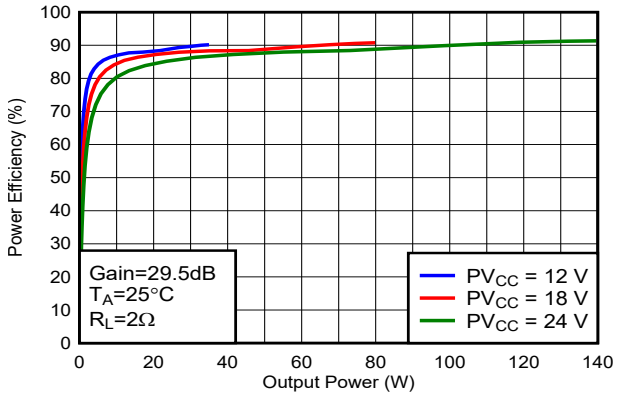


Figure 5-59. Efficiency vs Output Power

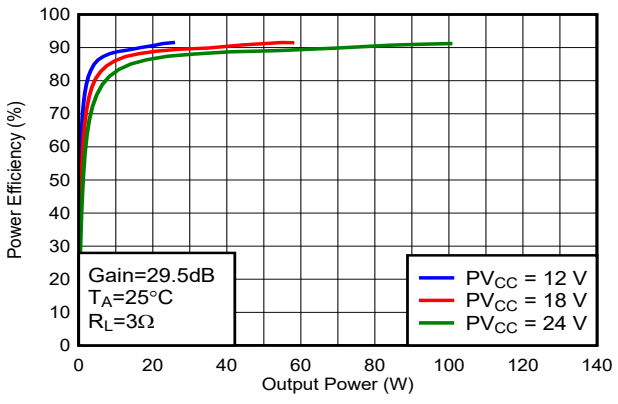


Figure 5-60. Efficiency vs Output Power

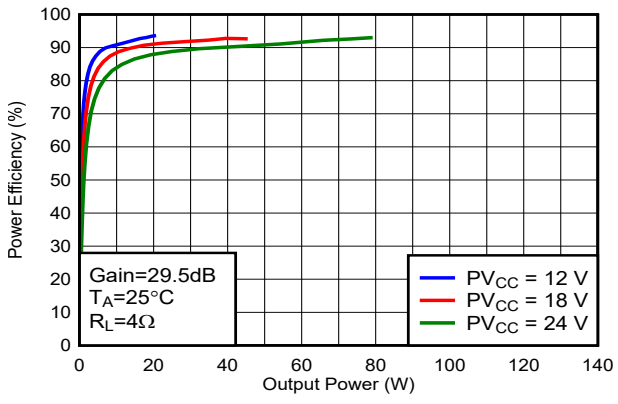


Figure 5-61. Efficiency vs Output Power

5.7.4 Parallel Bridge Tied Load (PBTL) Configuration With 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Amplifier Loop Bandwidth, the LC filter used was 10µH / 0.68µF (Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see connect method in Section 8.1.2) , unless otherwise noted.

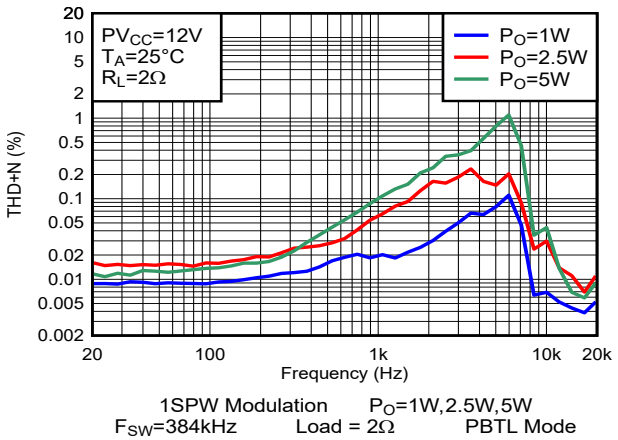


Figure 5-62. THD+N vs Frequency-PBTL

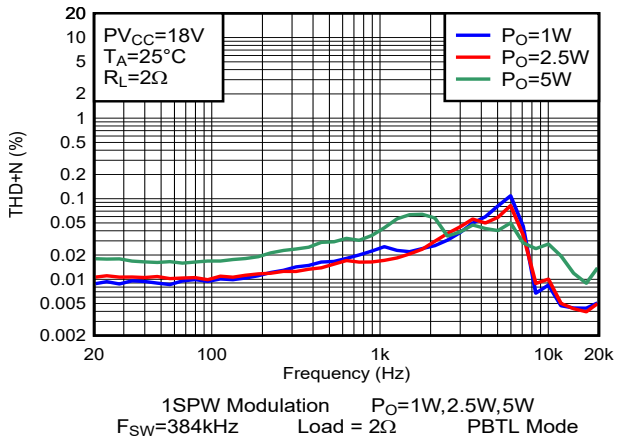


Figure 5-63. THD+N vs Frequency-PBTL

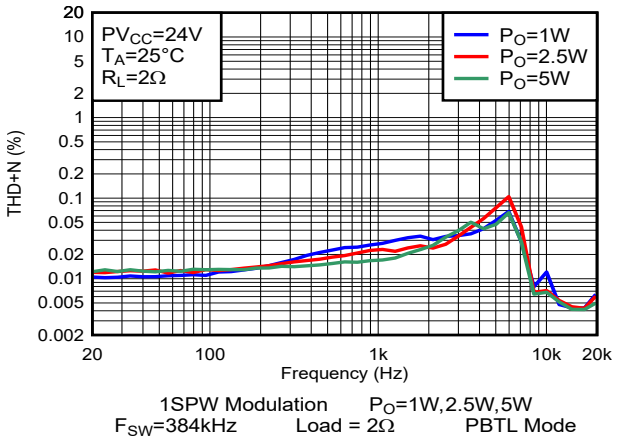


Figure 5-64. THD+N vs Frequency-PBTL

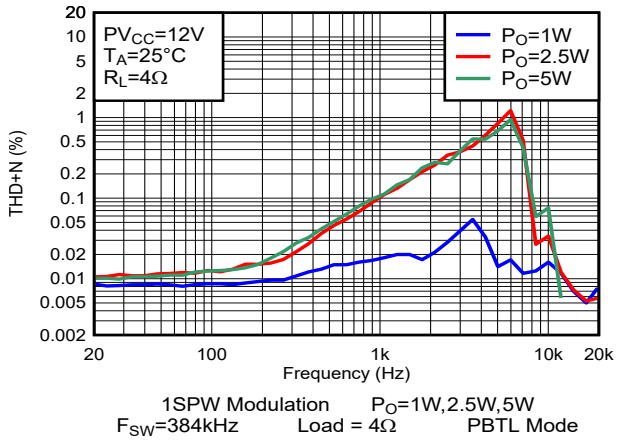


Figure 5-65. THD+N vs Frequency-PBTL

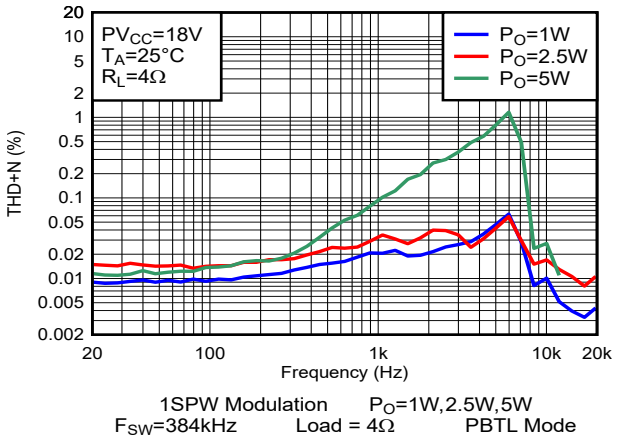


Figure 5-66. THD+N vs Frequency-PBTL

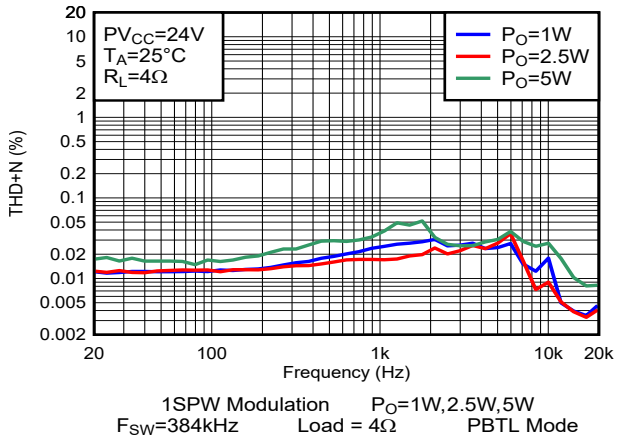


Figure 5-67. THD+N vs Frequency-PBTL

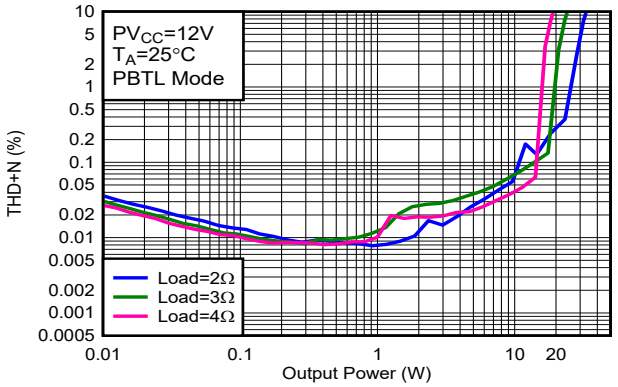


Figure 5-68. THD+N vs Output Power-PBTL

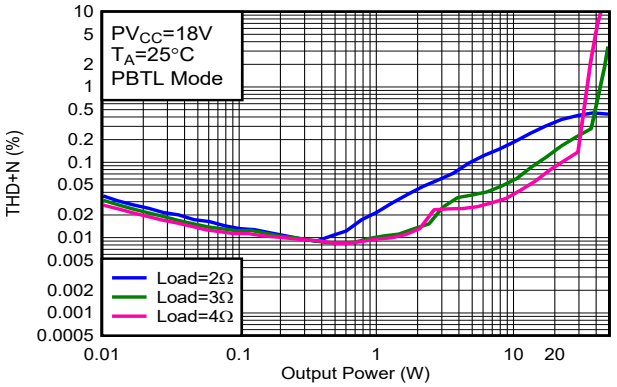


Figure 5-69. THD+N vs Output Power-PBTL

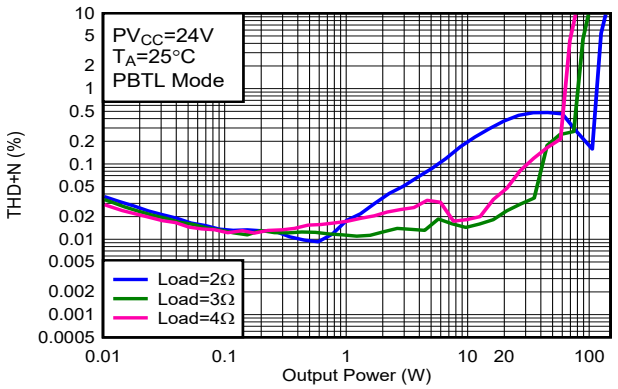


Figure 5-70. THD+N vs Output Power-PBTL

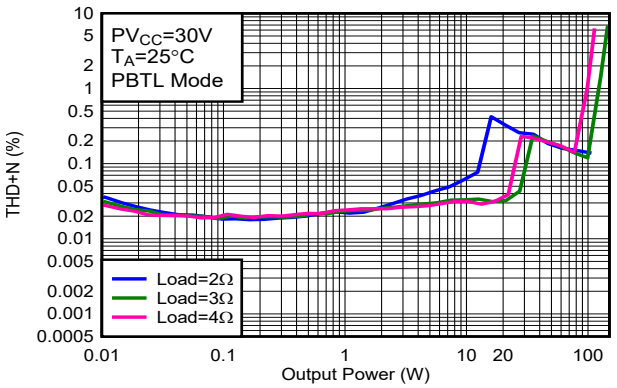


Figure 5-71. THD+N vs Power-BTL

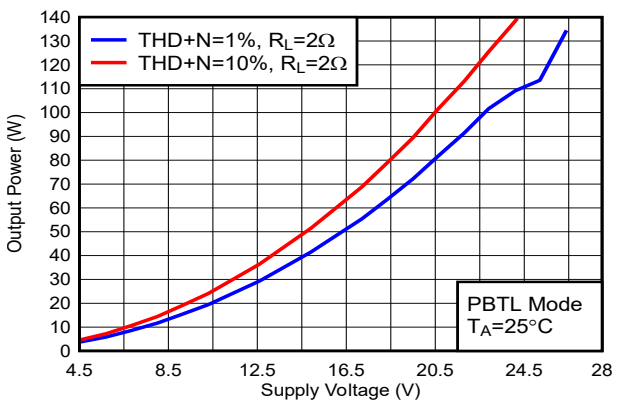


Figure 5-72. Output Power vs Supply Voltage

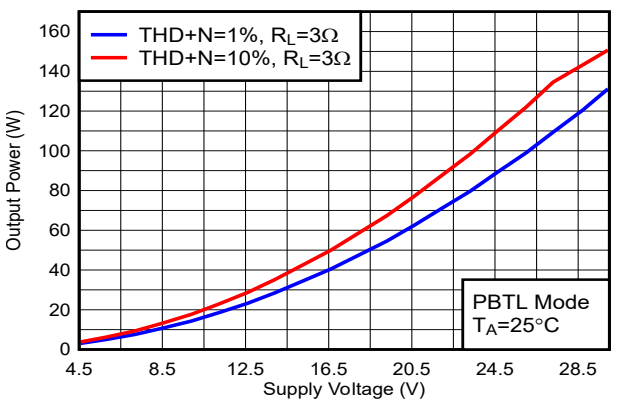
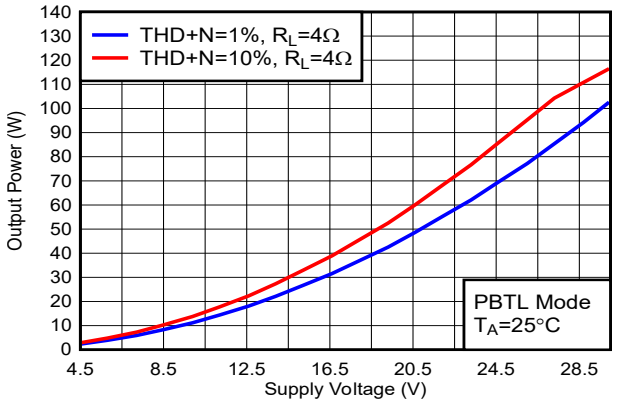
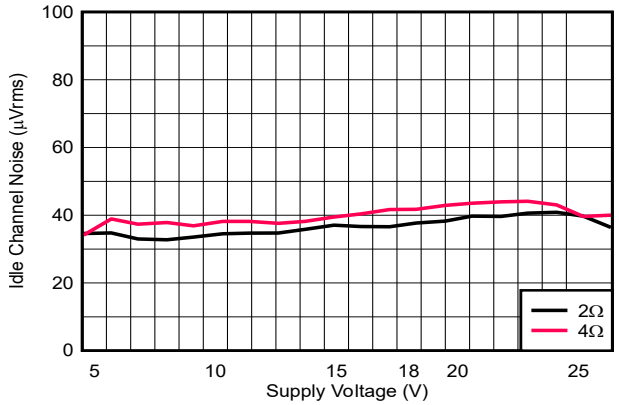


Figure 5-73. Output Power vs Supply Voltage



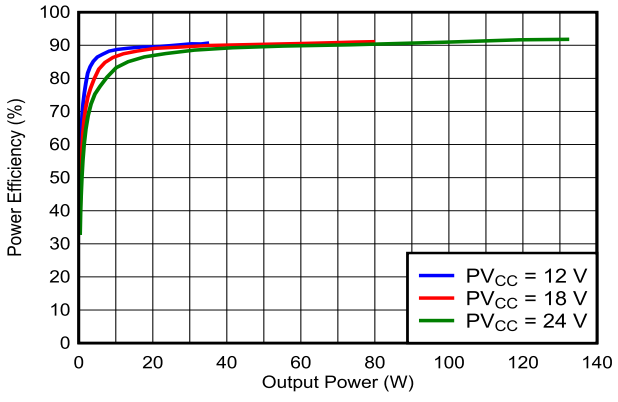
1SPW Modulation
F_{SW}=384kHz Load = 4Ω PBTL Mode

Figure 5-74. Output Power vs Supply Voltage



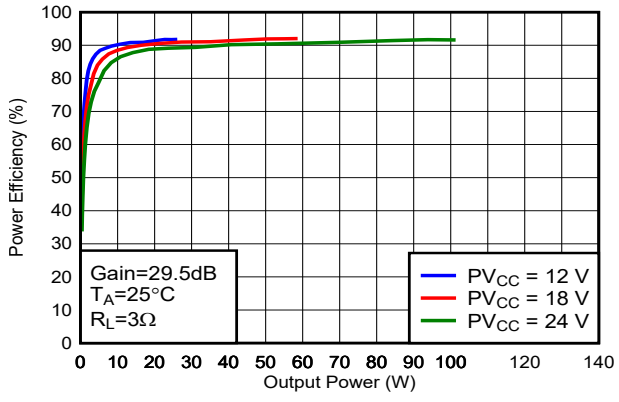
1SPW Modulation
F_{SW}=384kHz Load = 2Ω, 4Ω PBTL Mode

Figure 5-75. Idle Channel Noise vs Supply Voltage



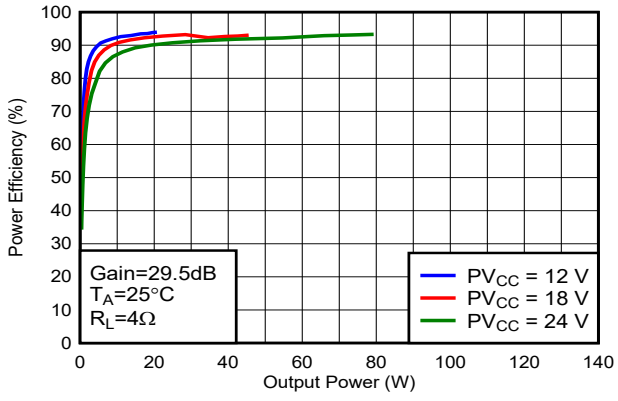
1SPW Modulation
F_{SW}=384kHz Load = 2Ω PBTL Mode

Figure 5-76. Efficiency vs Output Power



1SPW Modulation
F_{SW}=384kHz Load = 3Ω PBTL Mode

Figure 5-77. Efficiency vs Output Power



1SPW Modulation
F_{SW}=384kHz Load = 4Ω PBTL Mode

Figure 5-78. Efficiency vs Output Power

6 Detailed Description

6.1 Overview

The TAS5830 device combines 4 main building blocks into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

- A stereo digital to PWM modulator, then PWM modulator to power stage.
- An Audio DSP subsystem.
- A flexible closed-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low-voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. Two internal LDOs convert PVDD to 5V for GVDD and AVDD, one internal LDO converts DVDD to 1.5V for VR_DIG.

6.2 Functional Block Diagram

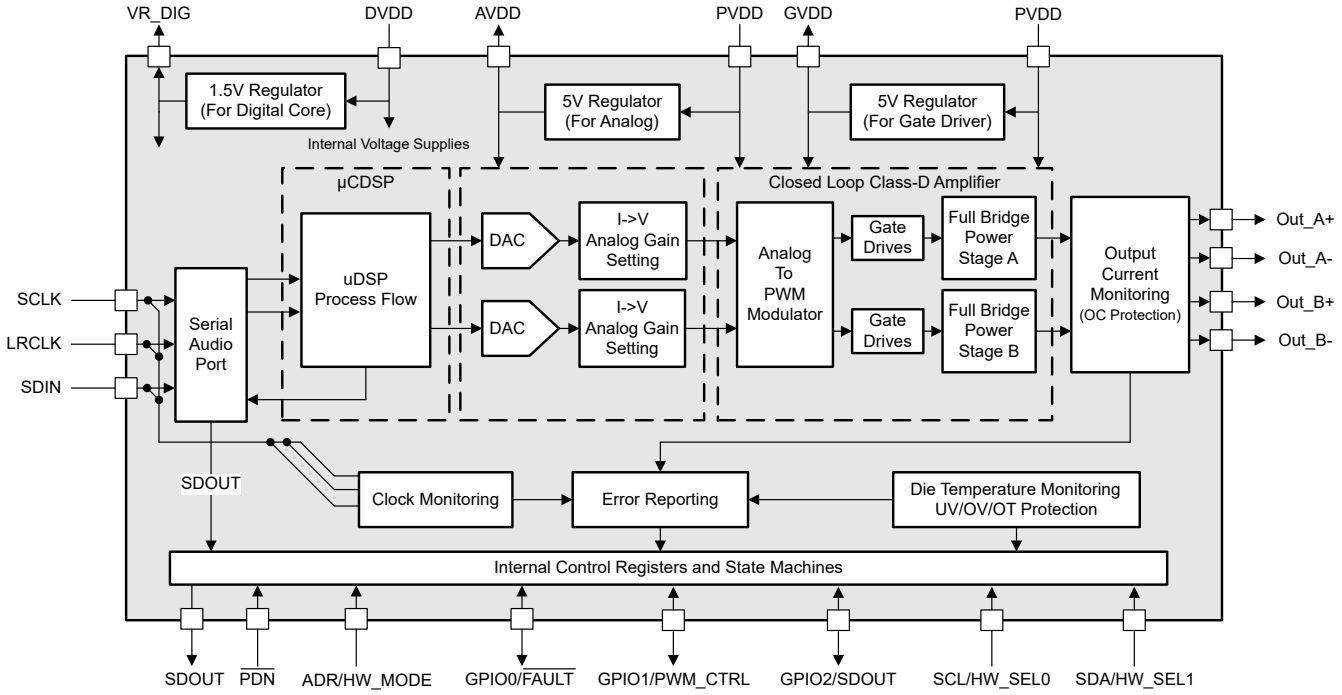


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Power Supplies

For system design, TAS5830 needs a 3.3V or 1.8V supply in addition to the (typical) 12V or 24V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (GVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

6.3.2 Device Clocking

The TAS5830 devices have flexible systems for clocking. Internally, the device requires several clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

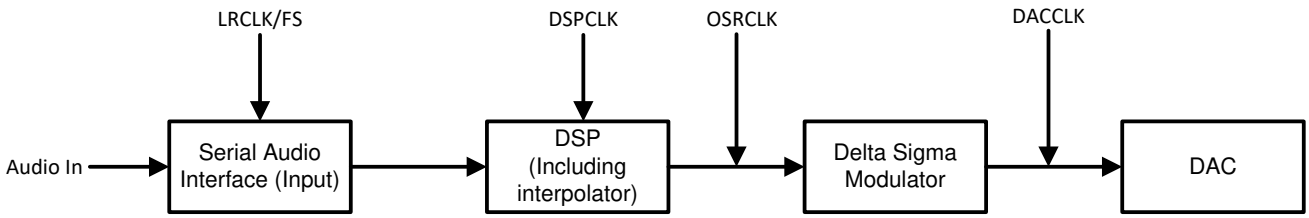


Figure 6-2. Audio Flow with Respective Clocks

Figure 6-2 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left/Right Word Clock or Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher-rate clocks required by the DSP and the DAC clock.

The TAS5830 device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32kHz, 44.1kHz – 48kHz, 88.2kHz – 96kHz, and 176.4kHz – 192kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

If the input LRCLK/SCLK stopped during music playing, the TAS5830 DSP switches to sleep state and waits for the clock recovery (Class D output switches to Hi-Z automatically), once LRCLK/SCLK recovered, TAS5830 auto recovers to the play mode. There is no need to reload the DSP code.

6.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK , and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio

interface. Serial data is clocked into the TAS5830 device with SCLK. The LRCLK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Table 6-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	32 to 192	64, 32
TDM	32, 24, 20, 16	32	128
		44.1, 48	128, 256, 512
		96	128, 256
		192	128

When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

6.3.4 Clock Halt Auto-recovery

Certain host processors halt the I^2S clock when there is no audio playing. When the clock is halted, the device puts all channels into the Hi-Z state and issues a latched clock error in Register GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h] - D[2]. After audio clocks recovery, the device automatically returns to the previous state.

6.3.5 Sample Rate on the Fly Change

TAS5830 supports an on-the-fly change of the LRCLK(FS) rate. When changing LRCLK(FS) from 48kHz to 96kHz, the host processor seeds to put LRCLK(FS)/SCLK to a halt state for at least 100us before changing to the new sample rate.

6.3.6 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[5:4]). If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[3:2]) should set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in Figure 6-3 through Figure 6-7. The word length are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[1:0]). The offsets of data are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[7]) and Register (SAP_CTRL2 Register (Offset = 34h) [Reset = 00h] -D[7:0]). Default setting is I2S and 24 bit word length.

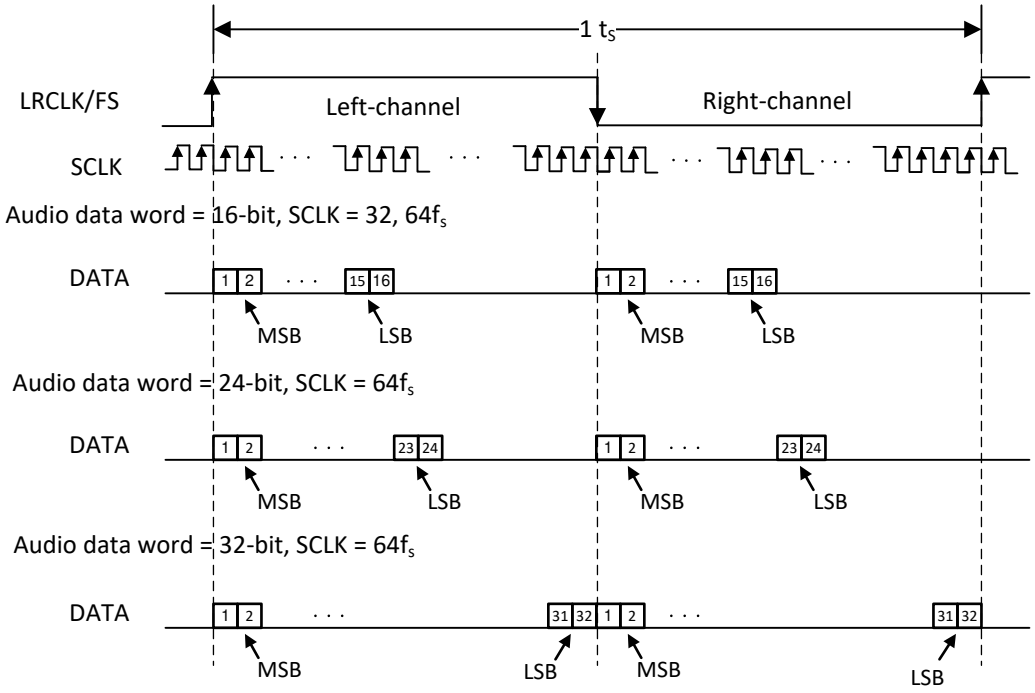
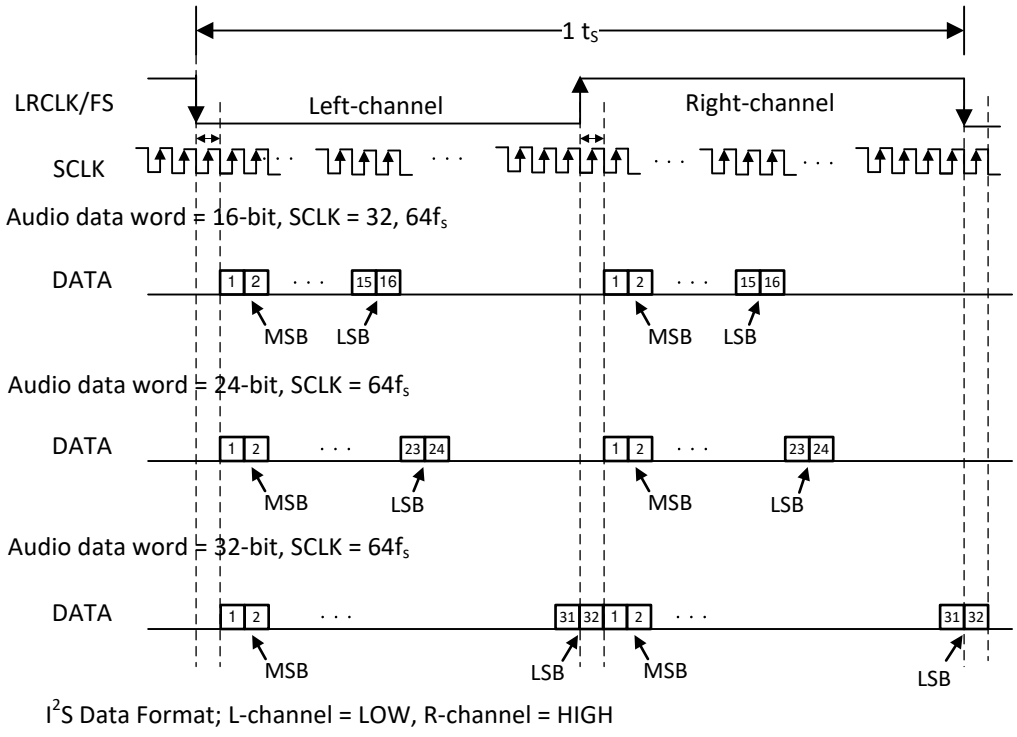
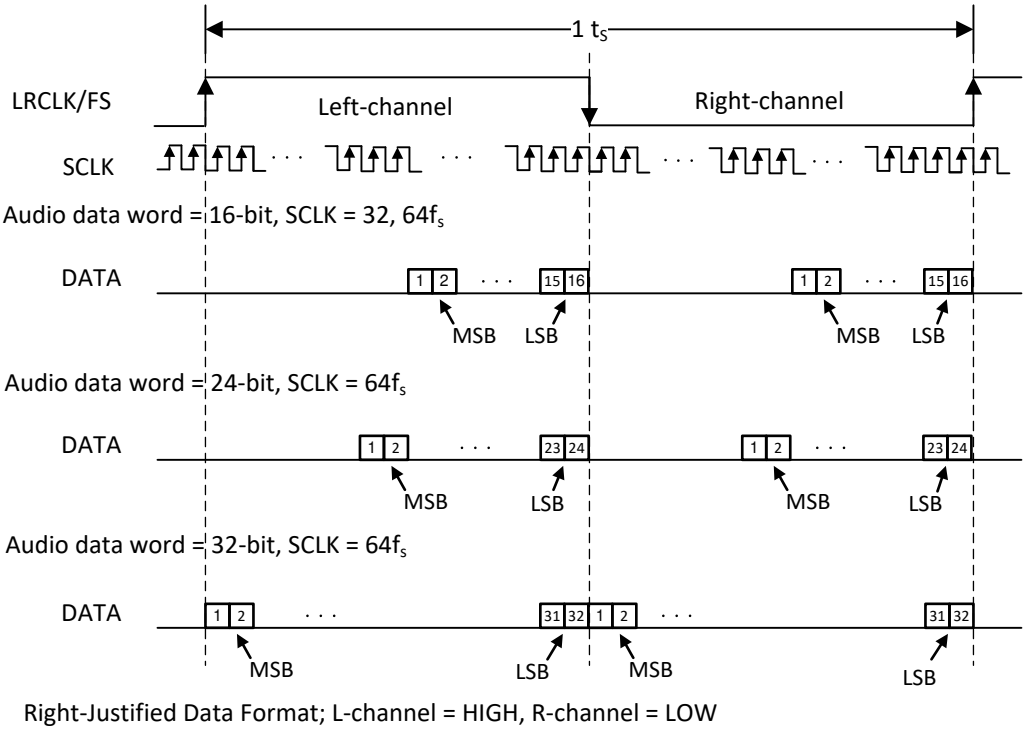


Figure 6-3. Left Justified Audio Data Format



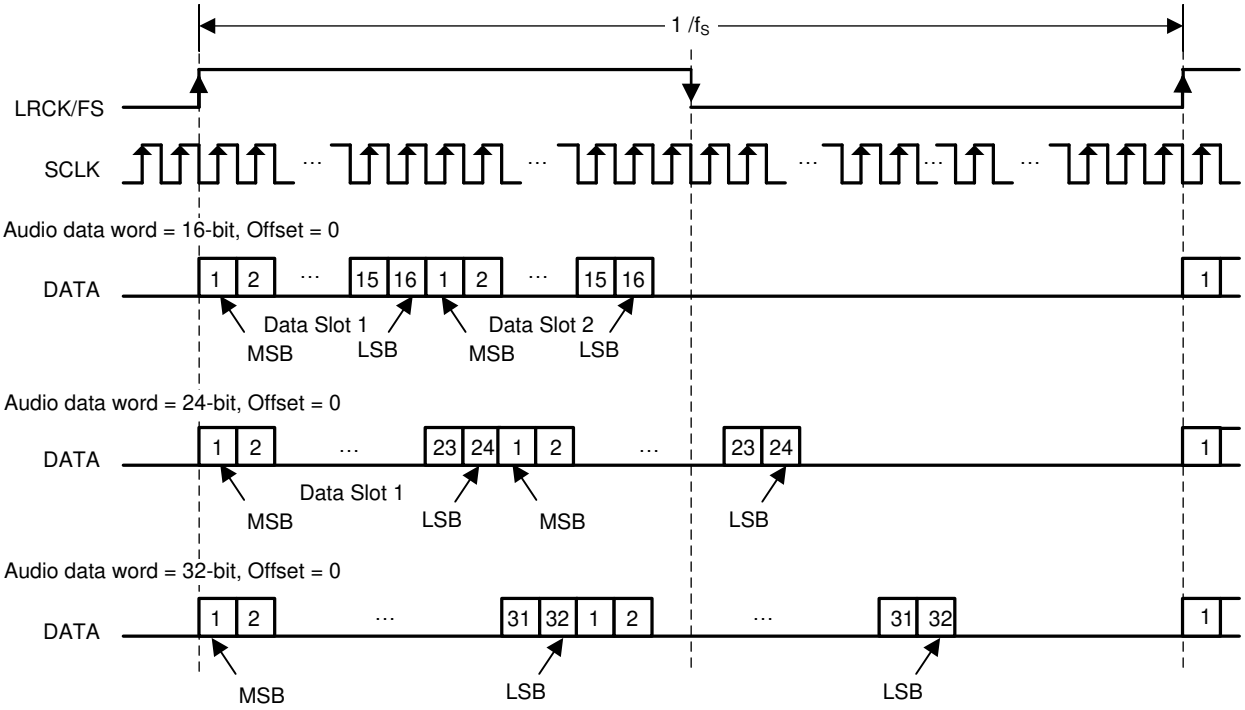
I²S Data Format; L-channel = LOW, R-channel = HIGH

Figure 6-4. I²S Audio Data Format



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

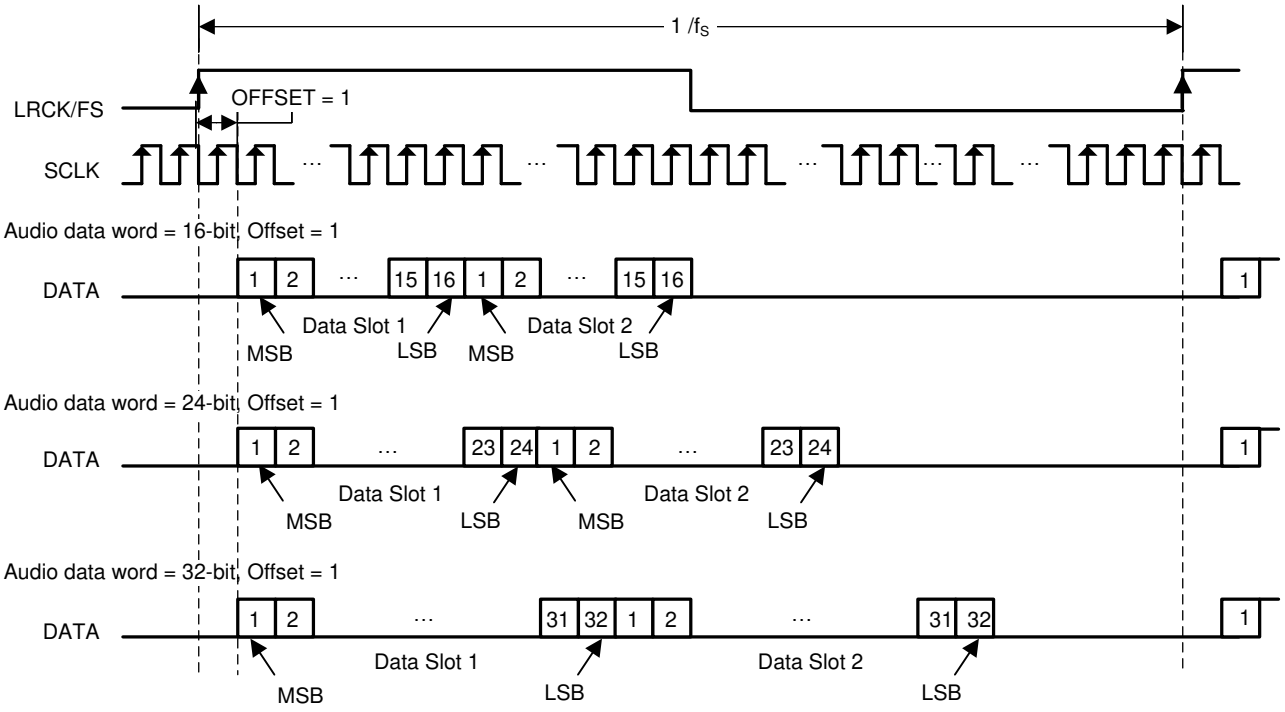
Figure 6-5. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 6-6. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 6-7. TDM 2 Audio Data Format

6.4 Device Functional Modes

6.4.1 Software Control

The TAS5830 device is configured via an I^2C communication port.

The I2C Communication Protocol is detailed in the I^2C Communication Port section. The I^2C timing requirements are described in theSection 5.6.

6.4.2 Speaker Amplifier Operating Modes

The TAS5830 device can be configured as two different amplifier configurations through Register DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] -D[2]:

- BTL Mode
- PBTL Mode

6.4.2.1 BTL Mode

In BTL mode, the TAS5830 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on the differential output pair shown as OUT_A+ and OUT_A-, and the amplified right signal is presented on the differential output pair shown as OUT_B+ and OUT_B-.

6.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe an operation in which the two outputs of the device are placed in parallel with one another to increase the power-sourcing capabilities of the device. On the output side of the TAS5830 device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter

PBTL. On the input side of the TAS5830 device, the input signal to the PBTL amplifier is the left frame of I2S or TDM data.

6.4.3 Low EMI Modes

TAS5830 employs several modes to minimize EMI while playing audio, and these modes can be used based on different applications.

6.4.3.1 Spread Spectrum

Spread spectrum modulation is a PWM modulation technique that reduces the peaks seen in EMI measurements by varying the output PWM frequency, resulting in a wider spectrum but lower level. The TAS5830 supports Spread Spectrum both of triangle and random mode.

The user needs to configure register RAMP_SS_CTRL0 Register (Offset = 6Bh) [Reset = 00h] to Enable triangle mode and enable spread spectrum, select spread spectrum frequency and range with RAMP_SS_CTRL1 Register (Offset = 6Ch) [Reset = 00h] . For 768kHz F_{SW} which is configured by DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] , the spread spectrum frequency and range are described in Table 6-2.

Table 6-2. Triangle Mode Spread Spectrum Frequency and Range Selection

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example: Central Switching Frequency is 768kHz, Triangle Frequency is 48kHz.

Register 0x02 = 0x41 // 768kHz Fsw, BTL Mode, 1SPW mode.

Register 0x6b = 0x03 // Enable Spread Spectrum

Register 0x6c = 0x03 // SS_CTRL[3:0]=0011, Triangle Frequency = 48kHz, Spread Spectrum Range should be 10% (729 kHz~807 kHz)

6.4.3.2 Channel to Channel Phase Shift

This device supports channel-to-channel 180-degree PWM phase shift to minimize the EMI. Bit 0 of ANA_CTRL Register (Offset = 53h) [Reset = 00h] can be used to disable or enable the phase shift.

6.4.3.3 Multi-Devices PWM Phase Synchronization

TAS5830 supports up to 4 phases of selection for the multi-device application system. For example, when a system integrates 4 TAS5830 devices, the user can select phase 0/1/2/3 for each device by registering RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] , which means there is a 45-degree phase shift between each device to minimize the EMI.

There are two methods for Multi-Device PWM phase synchronization. Phase Synchronization With I^2S Clock In Startup Phase or Phase Synchronization With GPIO.

6.4.3.3.1 Phase Synchronization With I^2S Clock In Startup Phase

1. Step 1, Halt I^2S clock.
2. Step 2, Configure each device phase selection and enable the phase synchronization. For example: Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x03 for device 0; Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x07 for device 1; Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x0B for device 2; Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x0F for device 3.
3. Step 3, Configure each device into HIZ mode.
4. Step 4, Provide I^2S to each device. Phase synchronization for all 4 devices is automatically done by internal sequence.
5. Step 5, Initialize the DSP code (This step can be skipped if only need to do the Phase Synchronization).
6. Step 6, Device to Device PWM phase shift should be fixed with 45 degrees.

6.4.3.3.2 Phase Synchronization With GPIO

1. Step 1, Connect the GPIOx pin of each device to the SOC GPIO pin on PCB.
2. Step 2, Configure each device GPIOx as phase sync input usage by registers GPIO_CTRL Register (Offset = 60h) [Reset = 00h] and GPIO_INPUT_SEL Register (Offset = 64h) [Reset = 00h] .
3. Step 3, Select a different phase for each device and enable phase synchronization by register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] .
4. Step 4, Configure each device into PLAY mode by register DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] and monitoring the POWER_STATE Register (Offset = 68h) [Reset = 00h] until device changes to HIZ state.
5. Step 5, Give a 0 to 1 toggle on SOC GPIO. Then all 4 devices enter into PLAY mode, and the device-to-device PWM phase shift should be fixed at 45 degrees.
6. Step 6, Phase Synchronization has been finished. Configure the GPIOx pin to another function based on the application.

6.4.4 Thermal Foldback

The Thermal Foldback (TFB), is designed to protect TAS5830 from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. The TFB allows the TAS5830 to play as loud as possible without triggering unexpected thermal shutdown. TAS5830 has four over-temperature warning (OTW) thresholds, each threshold is indicated in I2C register 0x73 bits 0, 1, 2, and 3. An internal Automatic Gain Limiter (AGL) gradually reduces the digital gain when the OTW value increases in temperature from level 1 (lowest OTW temperature) to level 4 (highest OTW temperature). The gain attenuation applied is proportional to OTW level, with lower OTW levels resulting in lower attenuation and higher OTW levels resulting in higher attenuation. When die temperature decreases and the OTW level reduces, the digital signal gain gradually increases until the temperature falls below the OTW level and digital gain is restored to the original level. Both the attenuation gain and adjustable rate are programmable. The TFB gain regulation speed (attack rate and release rate) settings are the same as a regular AGL, which is also configurable with TAS5830 App in PurePath™ Console3.

6.4.5 Device State Control

Other than Shutdown Mode, TAS5830 has other 4 states for different power dissipation: Deep Sleep, Sleep, HiZ, and Play mode. The power levels for each mode are listed in Electrical Characteristics.

- Writing register 0x03 [1:0]=00 places the device in Deep Sleep Mode. In this mode, I^2C is active. This mode can be used to extend the battery lifetime in some portable speaker applications. Once the host processor stops playing audio, TAS5830 can be set to Deep Sleep Mode to minimize power dissipation until host processor starts playing audio again. The device can return back to Play Mode by setting Register 0x03 [1:0] to 11. Compared with Shutdown Mode (Pull $\overline{PDN}$ Low), Deep Sleep Mode keeps the DSP and I2C active.
- Writing register 0x03 [1:0]=01 places the device in Sleep Mode. In this mode, the I^2C block, Digital core, DSP Memory, and 5V Analog LDO are active.
- Writing register 0x03 [1:0]=10 places the device in HiZ Mode. In this mode, the driver outputs are set to the HiZ state, and all other blocks are operating normally.
- Writing register 0x03 [1:0]=11 places the device in Play Mode enabling the output path.

6.4.6 Device Modulation

TAS5830 has 3 modulation schemes: BD modulation, 1SPW modulation, and Hybrid modulation. Select modulation schemes for TAS5830 with Register DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] D[1:0]-DAMP_MOD.

6.4.6.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

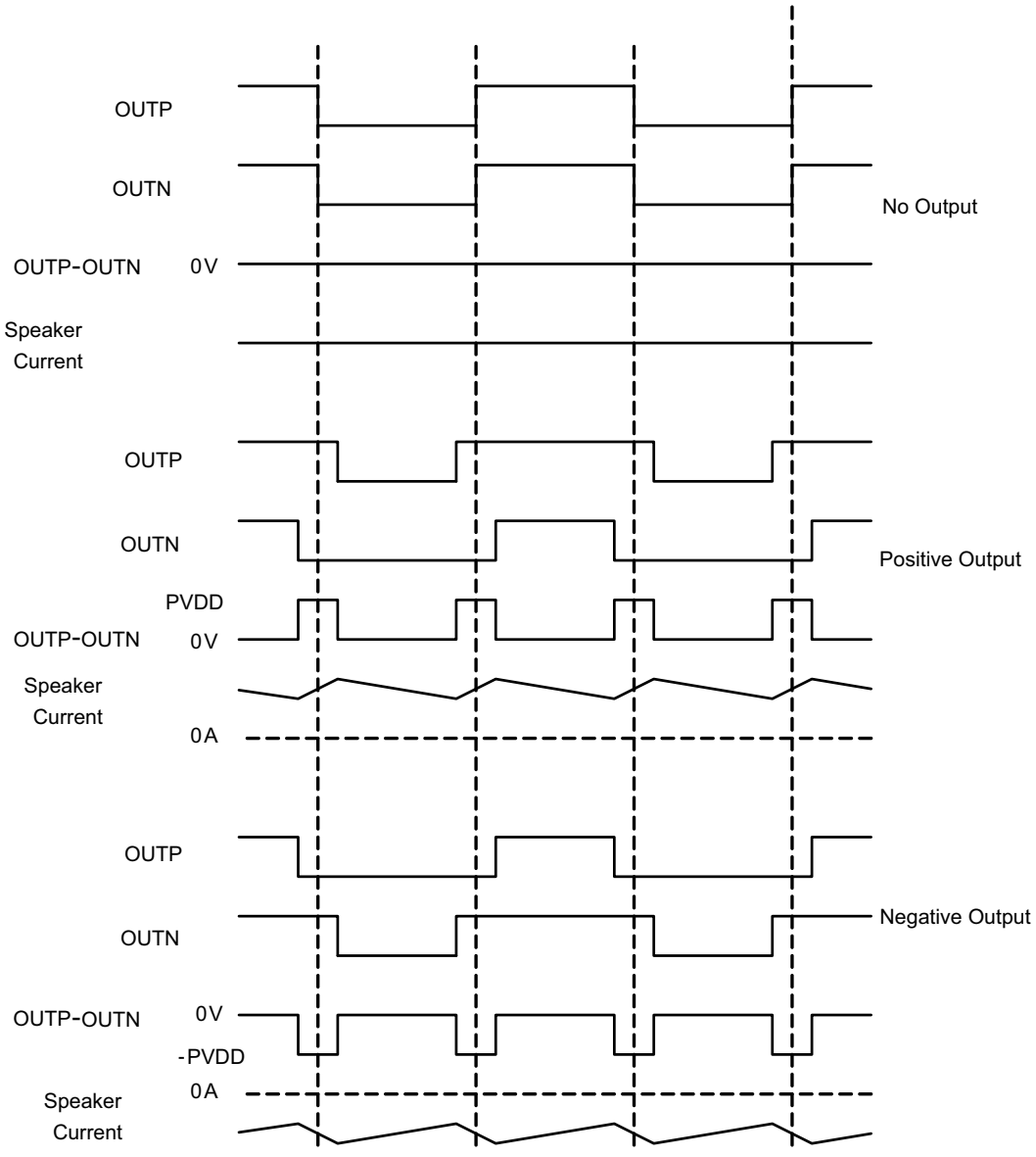


Figure 6-8. BD Mode Modulation

6.4.6.2 1SPW Modulation

The 1SPW mode alters the typical modulation scheme to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode, the outputs operate at approximately 17% modulation during idle conditions. When an audio signal is applied, one output decreases, and one increases. The decreasing output signal rails to GND. At this point, all the audio modulation takes place through the rising output. The result is that only one output is switching during the bulk of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

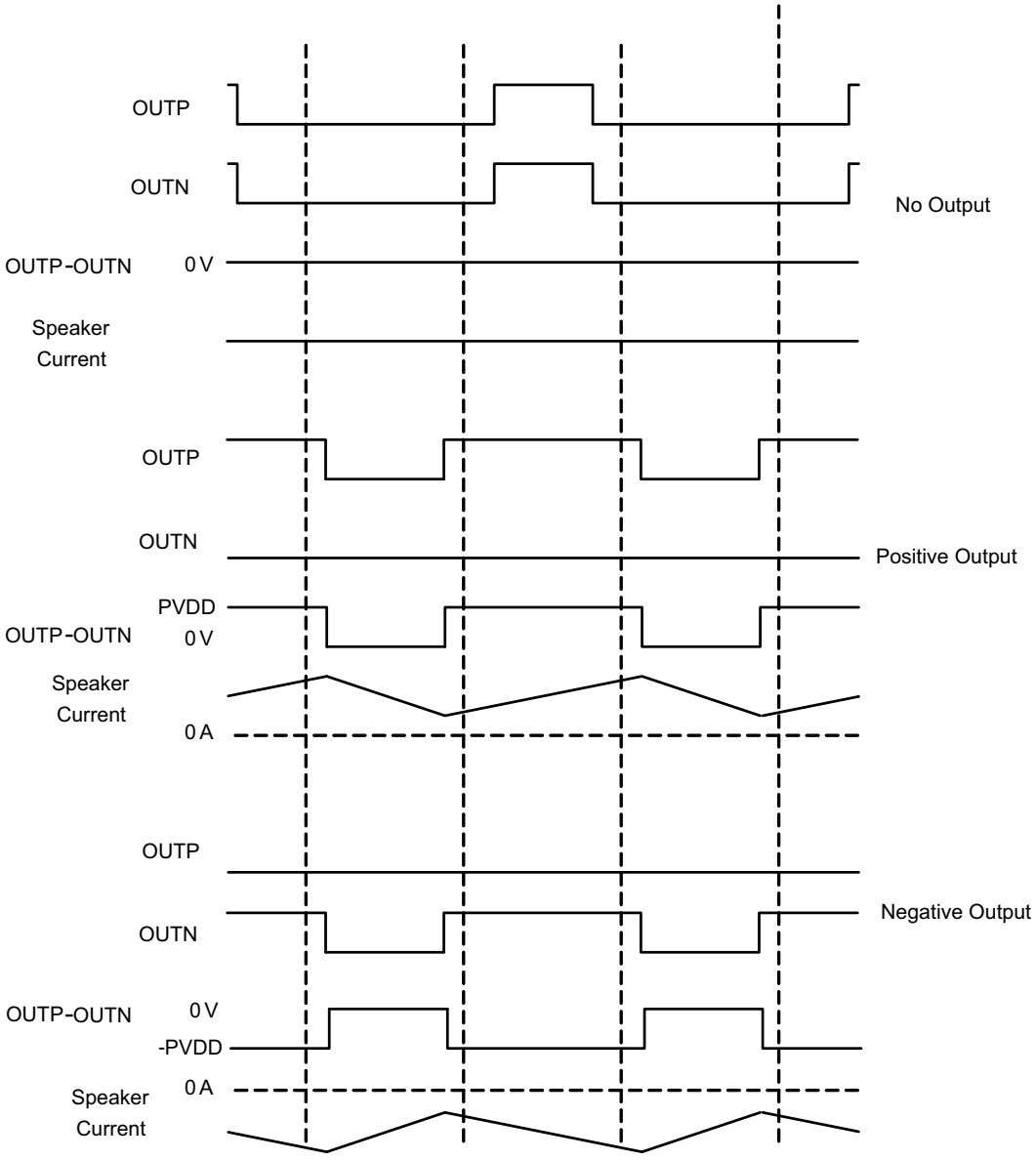


Figure 6-9. 1SPW Mode Modulation

6.4.6.3 Hybrid Modulation

Hybrid Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation, TAS5830 detects the input signal level and adjusts the PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra-low idle current and maintains the same audio performance level as the BD Modulation.

Note

Hybrid Modulation needs the internal DSP to detect the input signal level and adjust the PWM duty cycle dynamically. To use the Hybrid Modulation, users need to select the corresponding process flows which support Hybrid Modulation in TAS5830 PPC3 App. Look into TAS5830 PPC3 App for more information about TAS5830 flexible audio process flows.

6.4.7 Programming and Control

6.4.7.1 I²C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with I²C bus protocol and supports Standard-mode, Fast-mode(FM) and Fast-mode Plus(FM+) data transfer rates for random and sequential write and read operations as a target device. Because the TAS5830 register map and DSP memory spans multiple pages and books, the user changes from book to book first and then page to page before writing to the individual registers or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255. All registers listed in TAS5830 data sheet belong to Page 0.

6.4.7.2 Hardware Control Mode

For systems that do not require the advanced flexibility of the I²C registers control or does not have an available I²C host controller, the TAS5830 can be used in Hardware Control Mode. Then the device operates in Hardware mode default configurations and any change is accomplished via the Hardware control pins. The audio performance between Hardware and Software Control modes with the same configuration is identical, however, more features are accessible under Software Control Mode through registers.

Several I/O's on the TAS5830 needs to be taken into consideration during schematic design for desired start up settings. The method for going into Hardware Control Mode is to pull high HW_MODE pin 8 to DVDD.

The TAS5830 default Hardware configuration is BTL mode, 768kHz switching frequency, 1SPW mode, 175kHz Class D amplifier loop bandwidth, 29.5Vp/FS analog gain, CBC threshold with 80% of OCP threshold. It requires the HW_SEL0 pin 16 and HW_SEL1 pin 15 directly tied to GND.

Table 6-3. Hardware Control - HW_SEL0 Pin16

Pin Configuration	Analog Gain	H-Bridge Output Configuration
0Ω to GND	33.1V_P/FS	BTL
1kΩ to GND	23.4V_P/FS	BTL
4.7kΩ to GND	16.6V_P/FS	BTL
15kΩ to GND	8.3V_P/FS	BTL
33kΩ to DVDD	8.3V_P/FS	PBTL
6.8kΩ to DVDD	16.6V_P/FS	PBTL
1.5kΩ to DVDD	23.4V_P/FS	PBTL
0Ω to DVDD	33.1V_P/FS	PBTL

Table 6-4. Hardware Control - HW_SEL1 Pin15

Pin Configuration	F_{SW}&Class D Loop Bandwidth	Cycle By Cycle Current Limit Threshold	Spread Spectrum	Modulation
0Ω to GND	768kHz F_{SW}, 175kHz BW	CBC Threshold = 80% OCP	Disable	1SPW
1kΩ to GND	768kHz F_{SW}, 175kHz BW	CBC Disable	Disable	1SPW
4.7kΩ to GND	768kHz F_{SW}, 175kHz BW	CBC Threshold = 40% OCP	Disable	1SPW
15kΩ to GND	768kHz F_{SW}, 175kHz BW	CBC Threshold = 60% OCP	Disable	1SPW
33kΩ to DVDD	480kHz F_{SW}, 100kHz BW	CBC Disable	Enable	BD

Table 6-4. Hardware Control - HW_SEL1 Pin15 (continued)

Pin Configuration	F_{SW}&Class D Loop Bandwidth	Cycle By Cycle Current Limit Threshold	Spread Spectrum	Modulation
6.8kΩ to DVDD	480kHz F_{SW}, 100kHz BW	CBC Threshold = 80% OCP	Enable	BD
1.5kΩ to DVDD	480kHz F_{SW}, 100kHz BW	CBC Threshold = 40% OCP	Enable	BD
0Ω to DVDD	480kHz F_{SW}, 100kHz BW	CBC Threshold = 60% OCP	Enable	BD

Example 1:

BTL Mode, FSW = 768kHz, 1SPW Modulation, 175kHz Loop Bandwidth, CBC Threshold = 80% OCP, Analog Gain = 29.5V_P/FS, Spread spectrum disabled.

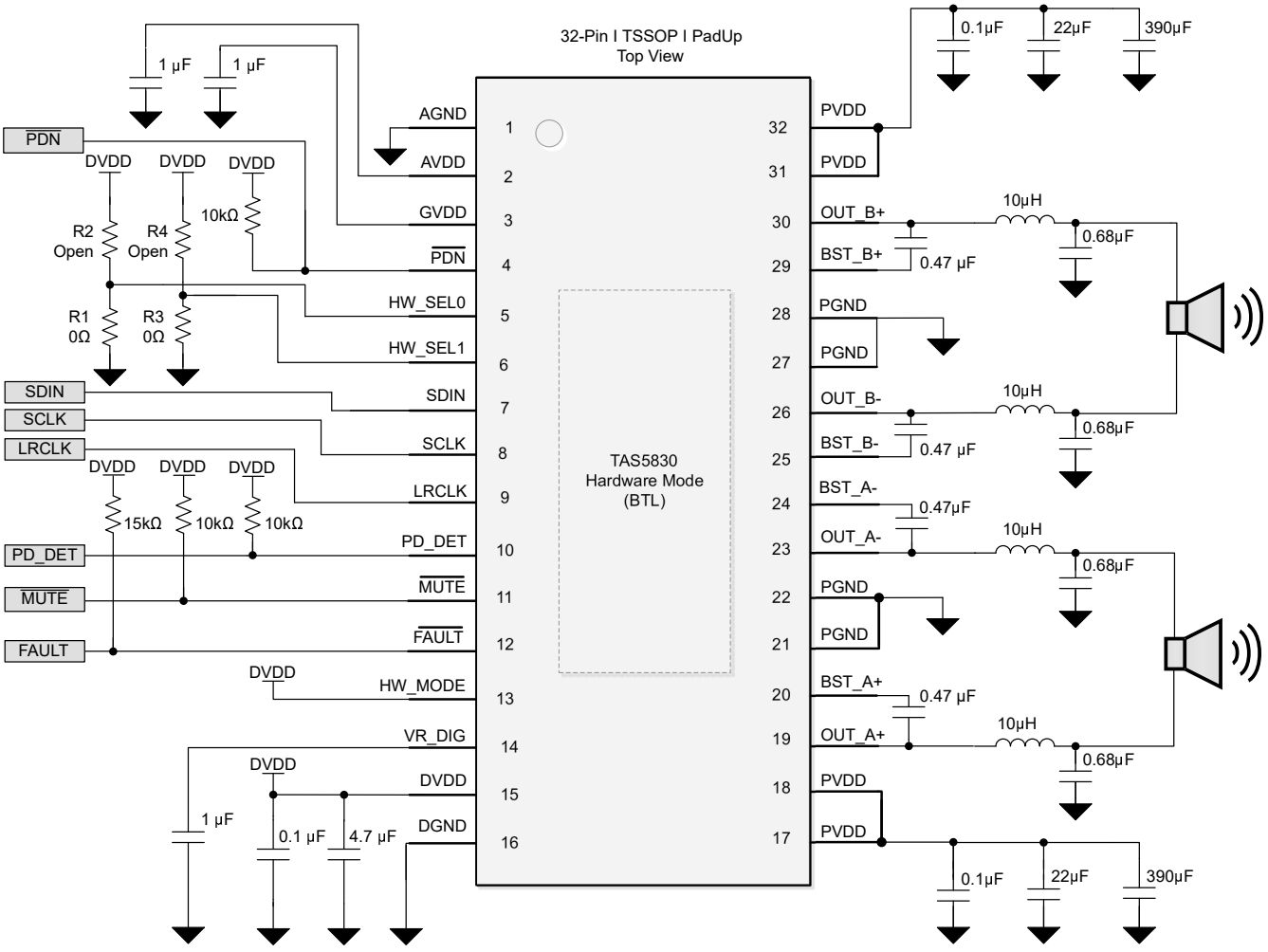


Figure 6-10. Typical Hardware Control Mode Application Schematic-BTL Mode

Example 2:

PBTL Mode, FSW = 768kHz, 1 SPW Modulation, 175kHz Loop Bandwidth, CBC Threshold = 80% OCP, Analog Gain = 29.5V_P/FS, Spread spectrum disabled.

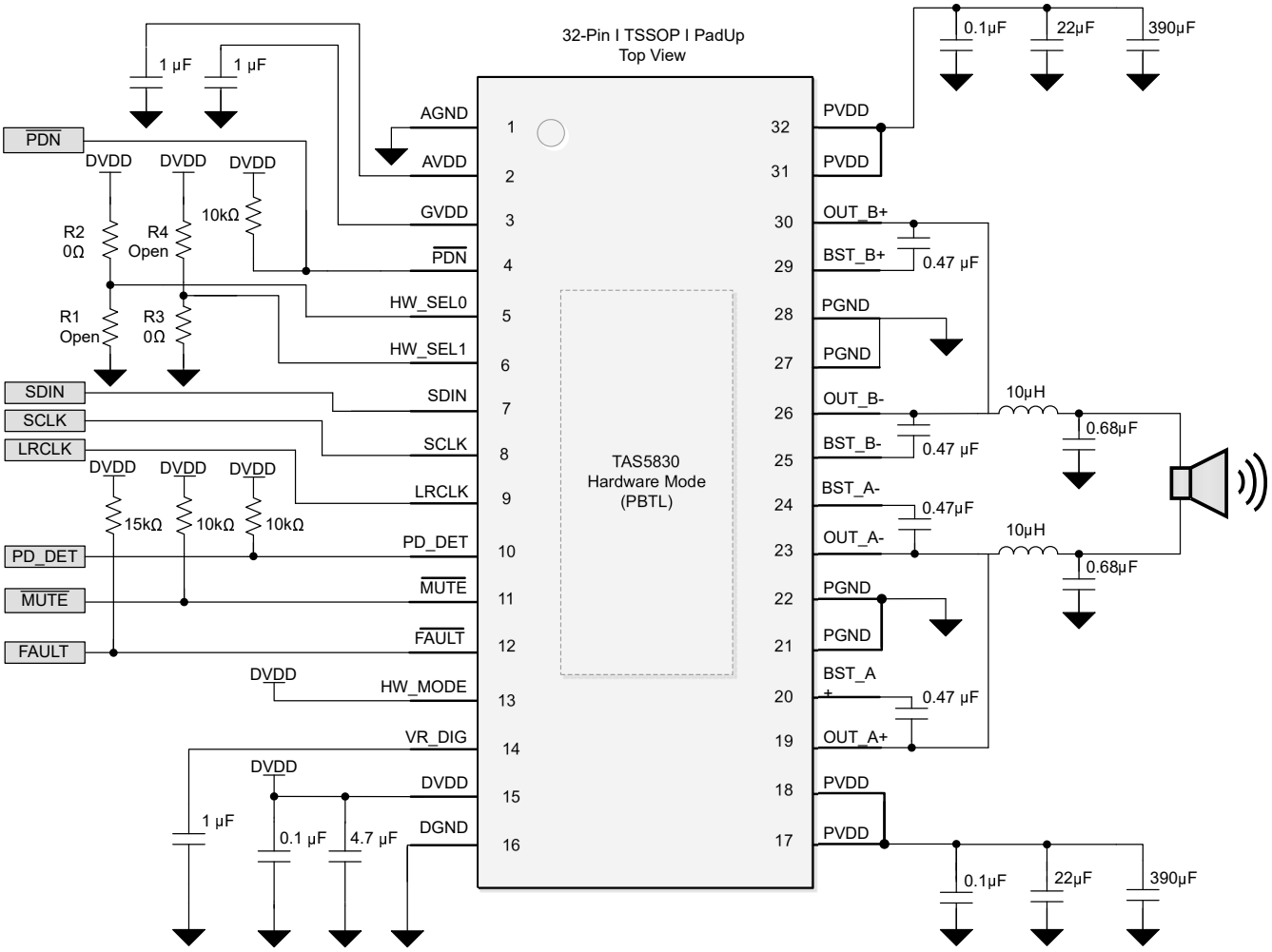


Figure 6-11. Typical Hardware Control Mode Application Schematic-PBTL Mode

6.4.7.3 I²C Target Address

The TAS5830 device has 7 bits for the target address. The user-defined address through ADR pin is listed in Table 6-5.

Table 6-5. I² C Target Address Configuration

ADR PIN Configuration	MSBs				User Define			LSB
0Ω to GND	1	1	0	0	0	0	0	R/ $\overline{W}$
1kΩ to GND	1	1	0	0	0	0	1	R/ $\overline{W}$
4.7kΩ to GND	1	1	0	0	0	1	0	R/ $\overline{W}$
15kΩ to GND	1	1	0	0	0	1	1	R/ $\overline{W}$
33kΩ to DVDD	1	1	0	0	1	0	0	R/ $\overline{W}$
6.8kΩ to DVDD	1	1	0	0	1	0	1	R/ $\overline{W}$

6.4.7.3.1 Random Write

As shown in Figure 6-12, a single-byte data-write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the controller transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the controller device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the controller device transmits a stop condition to complete the single-byte data-write transfer.

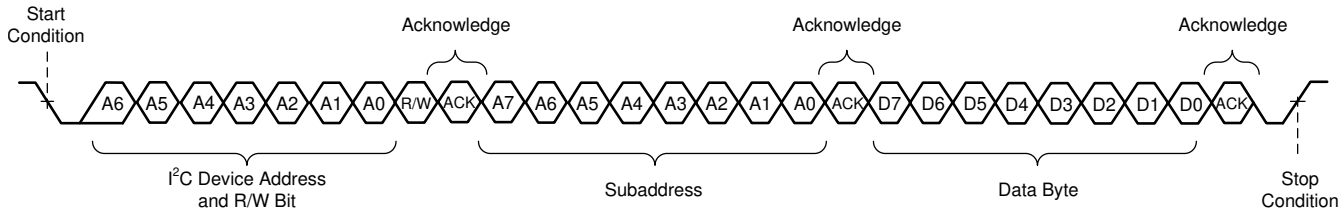


Figure 6-12. Random Write Transfer

6.4.7.3.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the controller to the device as shown in Figure 6-13. After receiving each data byte, the device responds with an acknowledge bit and the I² subaddress is automatically incremented by one.

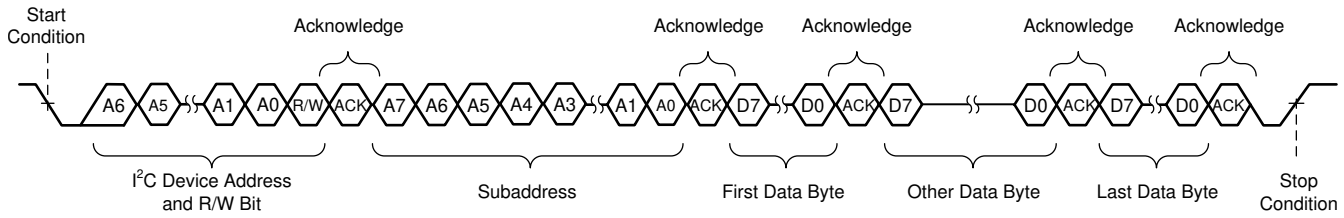


Figure 6-13. Sequential Write Transfer

6.4.7.3.3 Random Read

As shown in Figure 6-14, a single-byte data-read transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the controller device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

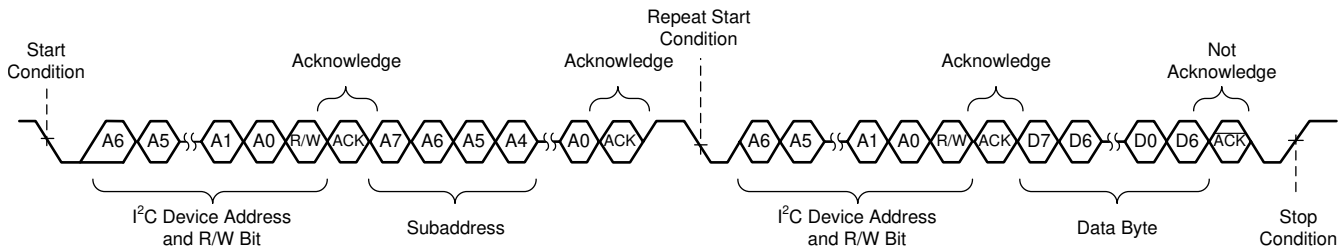


Figure 6-14. Random Read Transfer

6.4.7.3.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the controller device as shown in Figure 6-15. Except for the last data byte, the controller device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C sub address by one. After receiving the last data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the transfer.

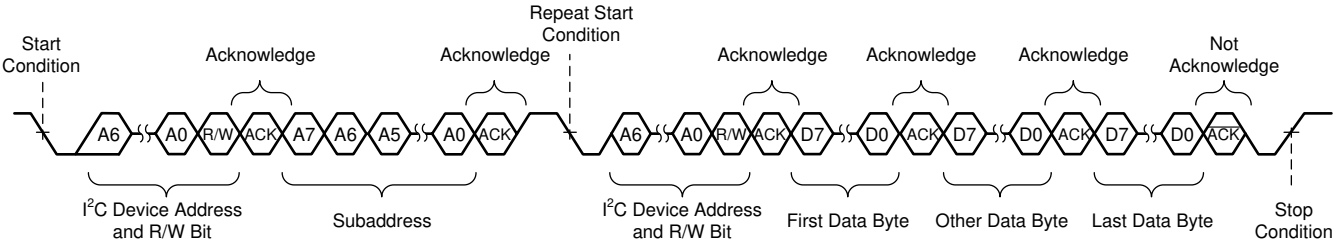


Figure 6-15. Sequential Read Transfer

6.4.7.3.5 DSP Memory Book, Page and BQ update

On Page 0x00 of each book, Register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a Page first write 0x00 to Register 0x00 to switch to Page 0 then write the book number to Register 0x7f on Page 0. To switch between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in book 0xAA. The five coefficients of every Biquad Filter is written entirely and sequentially from the lowest address to the highest address. The address of all Biquad Filters can be found in Register Maps

All DSP/Audio Process Flow Related Register are listed in Application Note, TAS5830 Process Flows

6.4.7.3.6 Checksum

This device supports two different checksum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers changes the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (for example. 0x 00 00 00 00) to the respective 4-byte register locations.

6.4.7.3.6.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1 + x1 + x2 + x8)). A major advantage of the CRC checksum is that the checksum is input order sensitive. The CRC supports all I²C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

6.4.7.3.6.2 Exclusive or (XOR) Checksum

The XOR checksum is a simpler checksum scheme. The checksum performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where the checksum is read.

6.4.7.4 Control via Software

- Startup Procedures
- Shutdown Procedures

6.4.7.4.1 Startup Procedures

1. Configure ADR pin with proper setting for I^2C device address or Hardware Mode with proper HW_SEL0 and HW_SEL1 settings.
2. Bring up power supplies (it does not matter if PVDD or DVDD comes up first).
3. Once power supplies are stable, wait at least 100 µs, bring up $\overline{PDN}$ to High to enable internal LDO.
4. I^2C control port to configure desired settings. This process includes Deep Sleep to Hi-Z, register map configurations, DSP coefficients, and set into Play mode. Hardware Mode does not need this step I^2C writing.
5. Once I^2S clocks are stable, TAS5830 is going to normal operation music playing.

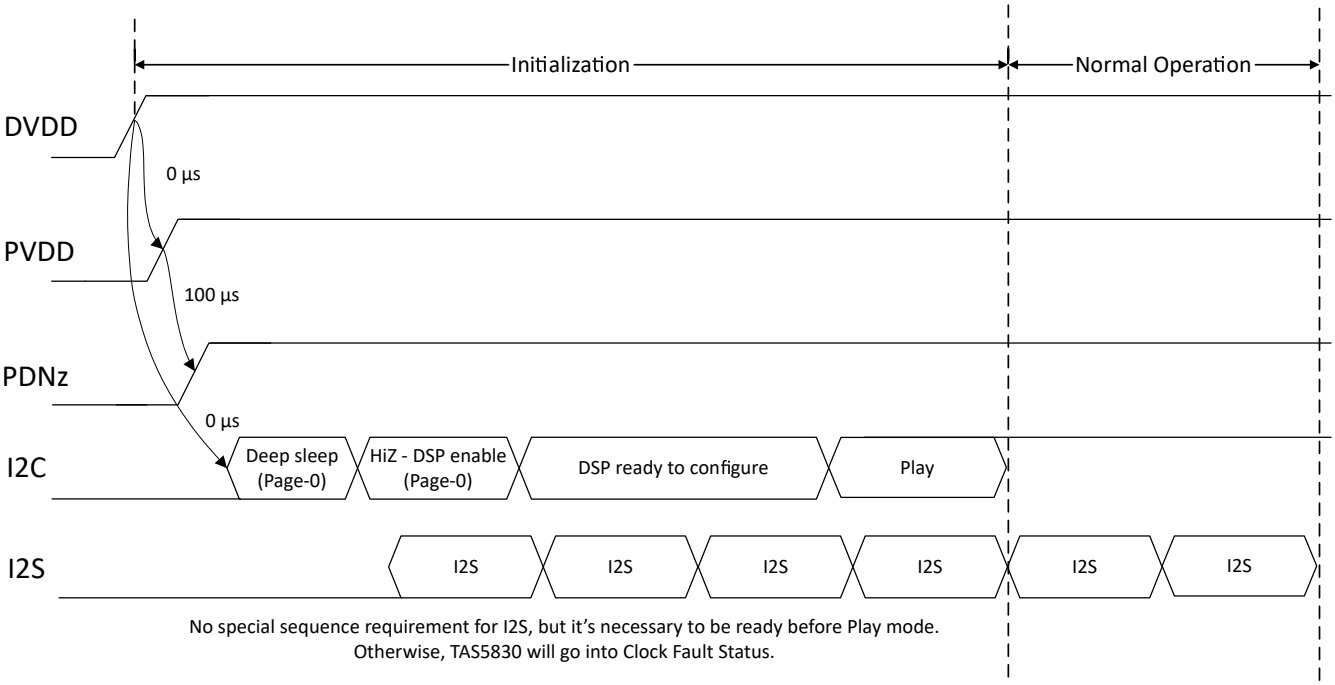
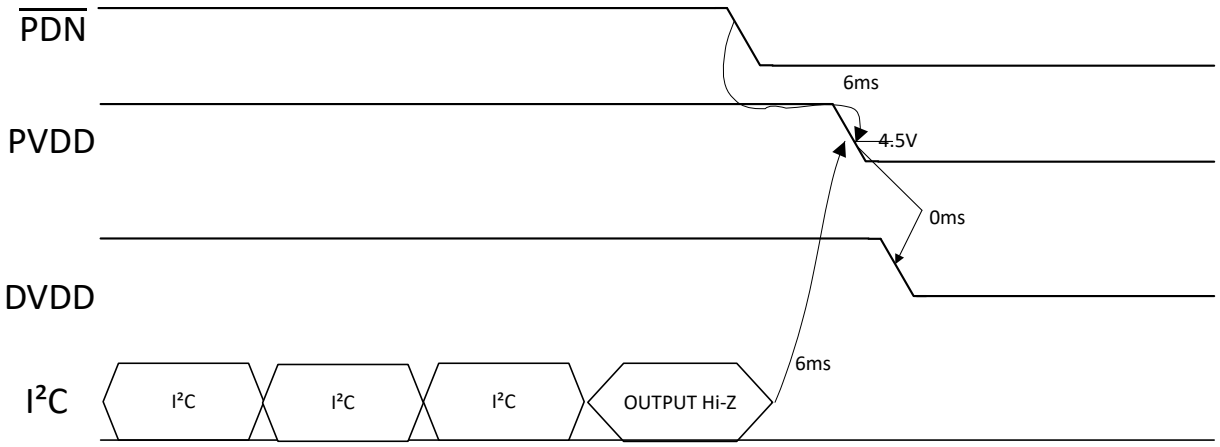


Figure 6-16. TAS5830 Startup Sequence

6.4.7.4.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h] -D[1:0]=10 (Hi-Z) via the I²C control port or Pull $\overline{PDN}$ low.
3. Wait at least 6ms (this time depends on the LRCLK rate, digital volume, and digital volume ramp-down rate).
4. Bring down power supplies.
5. The device is now fully shut down and powered off.



Before PVDD/DVDD power down, Class D Output driver needs to be disabled by PDN or by I²C.
At least 6ms delay needed based on LRCLK(Fs) = 48kHz, digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume = 24dB. Change the value of register 0x4C and 0x4E or change LRCLK rate, the delay changes.

Figure 6-17. Power-Down Sequence

6.4.7.5 Protection and Monitoring

6.4.7.5.1 Overcurrent Limit (Cycle-By-Cycle)

Instead of direct Overcurrent Shutdown to mute audio output, TAS5830 also provides CBC current limiting protection. The purpose is to reduce output current ahead of the Overcurrent Shutdown level by inserting pulse into PWM switching, and the threshold (list in Section 5.5) is configurable through Register CBC_CONTROL Register (Offset = 77h) [Reset = 00h] -D[4:3] Reg_CBC_Level_Sel.

The overall effect on the audio is quite similar to a voltage-clipping, which temporarily limits music signal peak power to maintain continuous music playing without disruption on the removal of the overload.

6.4.7.5.2 Overcurrent Shutdown (OCSD)

If there is a severe short-circuit event, such as output short to PVDD or ground, the TAS5830 starts the shutdown process less than 100ns once the peak-current detector is over the Overcurrent Threshold (list in Section 5.5). The shutdown speed depends on several factors, such as the impedance of the short circuit, supply voltage, and switching frequency.

If an OCSD event occurs, the fault GPIO is pulled low and I^2C fault register fault status (CHAN_FAULT Register (Offset = 70h) [Reset = 00h] -D[1:0]) is reported, then outputs transfer to high impedance Hi-Z status, signifying a fault. This is a latched error, and the user needs to restart output via I^2C clear fault operation by setting FAULT_CLEAR Register (Offset = 78h) [Reset = 00h] -D[0] = 1.

6.4.7.5.3 DC Detect Error

If the TAS5830 detects a DC offset in the output voltage cross speaker over DC error protection threshold DCR_{THRES}, and this status period is over T_{DCDET} (list in Section 5.5), the FAULTZ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault. This latched DC Protection error requires I^2C clear fault operation by setting FAULT_CLEAR Register (Offset = 78h) [Reset = 00h] -D[0] = 1 to restart the audio output.

6.4.7.5.4 Overtemperature Shutdown (OTSD)

The TAS5830 device continues to monitor die temperature to maintain that the temperature does not exceed the over-temperature threshold specified in Section 5.5. If an OTE event occurs, the fault GPIO is pulled low and I^2C fault status (GLOBAL_FAULT2 Register (Offset = 72h) [Reset = 00h] -D[0]) is reported, then audio output transfers to high impedance Hi-Z mode, signifying a fault. This is a latched error, and the error requires I^2C clear fault operation by setting FAULT_CLEAR Register (Offset = 78h) [Reset = 00h] -D[0] = 1 to restart the audio playing.

6.4.7.5.5 PVDD Overvoltage and Undervoltage Error

If the voltage presented on the PVDD supply rises over the $OVE_{THRES(PVDD)}$ or drops below the $UVE_{THRES(PVDD)}$ listed in Section 5.5, the fault GPIO is pulled to low and I^2C fault status (GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h] -D[1:0]) is reported, then the audio output transfers to high impedance Hi-Z mode. These are self-clearing errors, which means that once the PVDD level is back to normal operation, the device resumes audio playing.

6.4.7.5.6 PVDD Drop Detection

TAS5830 not only provides PVDD Undervoltage Shutdown protection but also optional PVDD drop detection. Based on internal PVDD real-time sensing voltage, TAS5830 can be configured to expected behavior, which could toggle pin10 PD_DET from high to low to indicate PVDD drops below a specific level (default 8 V), and whether TAS5830 automatically goes into Hi-Z mode to shut down the audio output.

The purpose is to feedback on PVDD voltage drop information through GPIO to the user product control system, which can implement a flexible protection strategy. For example, SOC could start the audio volume fade-out process once the PD_DET pin goes too low. This process could provide effective pop-click free control shutdown.

6.4.7.5.7 Clock Fault

When a clock error is detected on the incoming data clock, the TAS5830 device switches to an internal oscillator and continues to the driving DAC, which attenuates the data from the last known value. Once this process is completed, the DAC output is hard-muted to the ground, and the audio output stops. This non-latched clock fault status is reported I^2C fault status (GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h] -D[2]), and the device automatically returns to play mode once the correct clock is back.

7 Register Maps

7.1 reg_map Registers

Table 7-1 lists the memory-mapped registers for the reg_map registers. All register offset addresses not listed in Table 7-1 are considered as reserved locations and the register contents are not modified.

Table 7-1. REG_MAP Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Reset control	Go
2h	DEVICE_CTRL1	Device control 1	Go
3h	DEVICE_CTRL2	Device control 2	Go
4h	PVDD_UV_CONTROL	PVDD UV Control	Go
Fh	I2C_PAGE_AUTO_INC	I2C DSP memory access page auto increment	Go
28h	SIG_CH_CTRL	Signal chain control	Go
29h	CLOCK_DET_CTRL	Clock detection control	Go
30h	SDOUT_SEL	SDOUT selection	Go
31h	I2S_CTRL	I2S control 0	Go
33h	SAP_CTRL1	I2S control 1	Go
34h	SAP_CTRL2	I2S control 2	Go
35h	SAP_CTRL3	I2S control 3	Go
37h	FS_MON	FS monitor	Go
38h	BCLK_MON	BCLK monitor	Go
39h	CLKDET_STATUS	Clock detection status	Go
40h	DSP_PGM_MODE	DSP program mode	Go
46h	DSP_CTRL	DSP control	Go
4Ch	DIG_VOL	Digital volume	Go
4Eh	DIG_VOL_CTRL2	Digital volume control 2	Go
4Fh	DIG_VOL_CTRL3	Digital volume control 3	Go
50h	AUTO_MUTE_CTRL	Auto mute control	Go
51h	AUTO_MUTE_TIME	Auto mute time	Go
53h	ANA_CTRL	Analog control	Go
54h	AGAIN	Analog gain	Go
5Eh	ADC_RPT	ADC(PVDD voltage) report	Go
60h	GPIO_CTRL	GPIO control	Go
61h	GPIO1_SEL	GPIO1 output selection	Go
62h	GPIO2_SEL	GPIO2 output selection	Go
63h	GPIO0_SEL	GPIO0 output selection	Go
64h	GPIO_INPUT_SEL	GPIO input selection	Go
65h	MISC_CTRL1	misc control 1	Go
66h	MISC_CTRL2	misc control 2	Go
67h	DIE_ID	DIE ID	Go
68h	POWER_STATE	Power State	Go
69h	AUTOMUTE_STATE	Auto mute state	Go
6Ah	RAMP_PHASE_CTRL	Switching clock phase control	Go
6Bh	RAMP_SS_CTRL0	Spread spectrum control 0	Go
6Ch	RAMP_SS_CTRL1	Spread spectrum control 1	Go
70h	CHAN_FAULT	Channel fault	Go
71h	GLOBAL_FAULT1	Global fault 1	Go

Table 7-1. REG_MAP Registers (continued)

Offset	Acronym	Register Name	Section
72h	GLOBAL_FAULT2	Global fault 2	Go
73h	WARNING	Warning	Go
74h	PIN_CONTROL1	Pin control 1	Go
75h	PIN_CONTROL2	Pin control 2	Go
76h	MISC_CONTROL3	MISC control 3	Go
77h	CBC_CONTROL	CBC control	Go
78h	FAULT_CLEAR	Fault clear	Go

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. reg_map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 RESET_CTRL Register (Offset = 1h) [Reset = 00h]

Return to the Summary Table.

Reset control

Figure 7-1. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
W-0h			W-0h	W-0h			W-0h

Table 7-3. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	W	0h	
4	RST_MOD	W	0h	WRITE CLEAR BIT Reset Modules This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in Hi-Z mode. **0: Normal** 1: Reset modules
3-1	RESERVED	W	0h	
0	RST_REG	W	0h	WRITE CLEAR BIT Reset Registers This bit resets the mode registers back to their initial values. The RAM content is not cleared. This bit is auto cleared and must be set only when the DAC is in Hi-Z mode (resetting registers when the DAC is running is prohibited and not supported). **0: Normal** 1: Reset mode registers

7.1.2 DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h]

Return to the Summary Table.

Device control 1

Figure 7-2. DEVICE_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	PBTL_MODE	MODULATION	
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	

Table 7-4. DEVICE_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	FSW_SEL	R/W	0h	Select PWM switching frequency(Fsw) **3'b 000:384kHz** 3'b 010:480kHz 3'b 011:576kHz 3'b 100:768kHz 3'b 101:1.024MHz Others reserved
3	RESERVED	R/W	0h	
2	PBTL_MODE	R/W	0h	**0: Set device to BTL mode** 1:Set device to PBTL mode
1-0	MODULATION	R/W	0h	**00:BD mode** 01:1SPW mode 10:Hybrid mode 11: Reserved

7.1.3 DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h]

Return to the Summary Table.

Device control 2

Figure 7-3. DEVICE_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED			DSP_RST	MUTE	RESERVED	STATE_CTL	
R/W-0h			R/W-1h	R/W-0h	R/W-0h	R/W-0h	

Table 7-5. DEVICE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	DSP_RST	R/W	1h	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation **1: Reset the DSP**
3	MUTE	R/W	0h	Mute This bit issues soft mute request for both channels. The volume will be smoothly ramped down/up to avoid pop/click noise. **0: Normal volume** 1: Mute
2	RESERVED	R/W	0h	
1-0	STATE_CTL	R/W	0h	Device state control register **00: Deep Sleep** 01: Sleep 10: Hi-Z 11: PLAY

7.1.4 PVDD_UV_CONTROL Register (Offset = 4h) [Reset = 00h]

Return to the Summary Table.

PVDD UV Control

Figure 7-4. PVDD_UV_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED				UV_SEQ	UV_AVG		UV_BYP
R/W-0h				R/W-0h	R/W-0h		R/W-0h

Table 7-6. PVDD_UV_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	UV_SEQ	R/W	0h	**0: Disable when have PVDD UV, device jump to Hi-Z** 1: Enable when have PVDD UV, device jump to Hi-Z
2-1	UV_AVG	R/W	0h	**00: cycle by cycle, no average** 01: 16 samples 10: 32 samples 11: 64 samples
0	UV_BYP	R/W	0h	**0: Disable PVDD drop function** 1: Enable PVDD drop function

7.1.5 I2C_PAGE_AUTO_INC Register (Offset = Fh) [Reset = 00h]

Return to the Summary Table.

I2C DSP memory access page auto increment

Figure 7-5. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_INC	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 7-7. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	PAGE_INC	R/W	0h	Page auto increment disable Disable page auto increment mode. for non-zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. **0: Enable Page auto increment** 1: Disable Page auto increment
2-0	RESERVED	R/W	0h	

7.1.6 SIG_CH_CTRL Register (Offset = 28h) [Reset = 00h]

Return to the Summary Table.

Signal chain control

Figure 7-6. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
BCLK_RATIO				FS_MODE			
R/W-0h				R/W-0h			

Table 7-8. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BCLK_RATIO	R/W	0h	These bits indicate the configured BCLK ratio, the number of BCLK clocks in one audio frame. **4'b0000: Auto detection** 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS Others reserved.
3-0	FS_MODE	R/W	0h	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. **4'b0000 Auto detection** 4'b0010 8kHz 4'b0100 16kHz 4'b0110 32kHz 4'b1000 44.1kHz 4'b1001 48kHz 4'b1010 88.2kHz 4'b1011 96kHz 4'b1100 176.4kHz 4'b1101 192kHz Others Reserved

7.1.7 CLOCK_DET_CTRL Register (Offset = 29h) [Reset = 00h]

Return to the Summary Table.

Clock detection control

Figure 7-7. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DET_PLL	BCLK_RANGE	DET_FS	DET_BCLK	DET_BCLKMISS	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 7-9. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	DET_PLL	R/W	0h	Ignore PLL overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. **0: Regard PLL overrate detection** 1: Ignore PLL overrate detection
5	BCLK_RANGE	R/W	0h	Ignore BCLK Range Detection This bit controls whether to ignore the BCLK range detection. The BCLK must be stable between 256kHz and 50MHz or an error will be reported. When ignored, a BCLK range error will not cause a clock error. **0: Regard BCLK Range detection** 1: Ignore BCLK Range detection
4	DET_FS	R/W	0h	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error. But CLKDET_STATUS will report fs error. **0: Regard FS detection** 1: Ignore FS detection
3	DET_BCLK	R/W	0h	Ignore BCLK Detection This bit controls whether to ignore the BCLK detection against LRCLK. The BCLK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCLK error will not cause a clock error. **0: Regard BCLK detection** 1: Ignore BCLK detection
2	DET_BCLKMISS	R/W	0h	Ignore BCLK Missing Detection This bit controls whether to ignore the BCLK missing detection. When ignored an BCLK missing will not cause a clock error. **0: Regard BCLK missing detection** 1: Ignore BCLK missing detection
1-0	RESERVED	R/W	0h	

7.1.8 SDOUT_SEL Register (Offset = 30h) [Reset = 00h]

Return to the Summary Table.

SDOUT selection

Figure 7-8. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED							SDOUT_SEL
R/W-0h							R/W-0h

Table 7-10. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SDOUT_SEL	R/W	0h	SDOUT Select This bit selects what is being output as SDOUT via GPIO pins. **0: SDOUT is the DSP output (post-processing)** 1: SDOUT is the DSP input (pre-processing)

7.1.9 I2S_CTRL Register (Offset = 31h) [Reset = 00h]

Return to the Summary Table.

I2S control 0

Figure 7-9. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_INV	RESERVED				
R/W-0h		R/W-0h	R/W-0h				

Table 7-11. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	BCLK_INV	R/W	0h	BCLK Polarity This bit sets the inverted BCLK mode. In inverted BCLK mode, the DAC assumes that the LRCLK and DIN edges are aligned to the rising edge of the BCLK. Normally they are assumed to be aligned to the falling edge of the BCLK. **0: Normal BCLK mode** 1: Inverted BCLK mode
4-0	RESERVED	R/W	0h	

7.1.10 SAP_CTRL1 Register (Offset = 33h) [Reset = 02h]

Return to the Summary Table.

I2S control 1

Figure 7-10. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
I2SSHIFT_MSB	RESERVED	DATA_FMT		LRCLK_PULSE		FRAME_LENGTH	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-2h	

Table 7-12. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2SSHIFT_MSB	R/W	0h	I2S Shift MSB. Combine with the 8 bits in low register 34h.
6	RESERVED	R/W	0h	
5-4	DATA_FMT	R/W	0h	I2S Data Format These bits control both input and output audio interface formats for DAC operation. **00: I2S** 01: DSP/TDM 10: RTJ 11: LTJ
3-2	LRCLK_PULSE	R/W	0h	If the LRCLK pulse is shorter than 8 x BCLK, set bit 0-1 to '01' Otherwise, keep these bits as default value '00' 00: High width of LRCLK pulse is equal or greater than 8 cycles of BCLK 01: High width of LRCLK pulse is less than 8 cycles of BCLK
1-0	FRAME_LENGTH	R/W	2h	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits **10: 24 bits** 11: 32 bits

7.1.11 SAP_CTRL2 Register (Offset = 34h) [Reset = 00h]

Return to the Summary Table.

I2S control 2

Figure 7-11. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
I2SSHIFT_LSB							
R/W-0h							

Table 7-13. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2SSHIFT_LSB	R/W	0h	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. **8'b00000000: offset = 0 BCLK (no offset)** 8'b00000001: offset = 1 BCLK 8'b00000010: offset = 2 BCLKs … 8'b11111111: offset = 512 BCLKs

7.1.12 SAP_CTRL3 Register (Offset = 35h) [Reset = 11h]

Return to the Summary Table.

I2S control 3

Figure 7-12. SAP_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		CH1_DAC		RESERVED		CH2_DAC	
R/W-0h		R/W-1h		R/W-0h		R/W-1h	

Table 7-14. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	CH1_DAC	R/W	1h	Channel 1 DAC Data Path These bits control the channel 1 audio data path connection. 00: Zero data (mute) **01: Ch1 data** 10: Ch2 data 11: Reserved (do not set)
3-2	RESERVED	R/W	0h	
1-0	CH2_DAC	R/W	1h	Channel 2 DAC Data Path These bits control the channel 2 audio data path connection. 00: Zero data (mute) **01: Ch2 data** 10: Ch1 data 11: Reserved (do not set)

7.1.13 FS_MON Register (Offset = 37h) [Reset = 00h]

Return to the Summary Table.

FS monitor

Figure 7-13. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		BCLKRATIO_MSB		FS_MON			
R-0h		R-0h		R-0h			

Table 7-15. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	BCLKRATIO_MSB	R	0h	2 MSB of detected BCLK ratio. These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. Combine with the 8 bits in low register 38h. BCLK = 32 FS~512 FS
3-0	FS_MON	R	0h	These bits indicate the currently detected audio sampling rate. **4'b0000 FS Error** 4'b0010 8kHz 4'b0100 16kHz 4'b0110 32kHz 4'b1000 Reserved 4'b1001 48kHz 4'b1011 96kHz 4'b1101 192kHz Others Reserved

7.1.14 BCLK_MON Register (Offset = 38h) [Reset = 00h]

Return to the Summary Table.

BCLK monitor

Figure 7-14. BCLK_MON Register

7	6	5	4	3	2	1	0
BCLKRATIO_LSB							
R-0h							

Table 7-16. BCLK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLKRATIO_LSB	R	0h	These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. BCLK = 32 FS~512 FS

7.1.15 CLKDET_STATUS Register (Offset = 39h) [Reset = 00h]

Return to the Summary Table.

Clock detection status

Figure 7-15. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_OVERRATE	PLL_OVERRATE	PLL_LOCKED	BCLK_MISSING	BCLK_VALID	FS_VALID
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-17. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	BCLK_OVERRATE	R	0h	This bit indicates whether the BCLK is overrate or underrate. 0: BCLK is underrate 1: BCLK is overrate
4	PLL_OVERRATE	R	0h	This bit indicates whether the PLL is overrate or not. 0: PLL is underrate 1: PLL is overrate
3	PLL_LOCKED	R	0h	This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is not locked
2	BCLK_MISSING	R	0h	This bit indicates whether the BCLK is missing or not. 0: BCLK is normal 1: BCLK is missing
1	BCLK_VALID	R	0h	This bit indicates whether the BCLK is valid or not. The BCLK ratio must be stable and in the range of 32-512FS to be valid. 0: BCLK is valid 1: BCLK is not valid
0	FS_VALID	R	0h	In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid. In non auto detection mode(reg_fsmode!=0), FS error indicates that configured sampling frequency set by LRCLK(FS) is different with detected sampling frequency. Even if FS Error Detection Ignore is set, this flag will be also asserted. 0: Sampling rate is valid 1: Not valid

7.1.16 DSP_PGM_MODE Register (Offset = 40h) [Reset = 01h]

Return to the Summary Table.

DSP program mode

Figure 7-16. DSP_PGM_MODE Register

7	6	5	4	3	2	1	0
RESERVED				CH1_HIZ	CH2_HIZ	DSP_MODE	
R/W-0h				R/W-0h	R/W-0h	R/W-1h	

Table 7-18. DSP_PGM_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	CH1_HIZ	R/W	0h	1: Force CH1 to Hi-Z mode **0: Normal operation**
2	CH2_HIZ	R/W	0h	1: Force CH2 to Hi-Z mode **0: Normal operation**
1-0	DSP_MODE	R/W	1h	DSP Program Selection These bits select the DSP program to use for audio processing. 00: RAM mode **01: ROM mode** Others reserved.

7.1.17 DSP_CTRL Register (Offset = 46h) [Reset = 01h]

Return to the Summary Table.

DSP control

Figure 7-17. DSP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			PROC_RATE		RESERVED	IRAM_BOOT	DEF_COEF
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-1h

Table 7-19. DSP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	PROC_RATE	R/W	0h	**00:input** 01:48kHz 10:96kHz 11:192kHz
2	RESERVED	R/W	0h	
1	IRAM_BOOT	R/W	0h	DSP boots from IRAM When set DSP will boot from IRAM instead of IROM **0: Boot DSP from IROM** 1: Boot DSP from IRAM
0	DEF_COEF	R/W	1h	Use default coefficients from ZROM This bit controls whether to use default coefficients from ZROM or use the non-default coefficients downloaded to device by the Host 0 : Don't use default coefficients from ZROM **1 : Use default coefficents from ZROM**

7.1.18 DIG_VOL Register (Offset = 4Ch) [Reset = 30h]

Return to the Summary Table.

Digital volume

Figure 7-18. DIG_VOL Register

7	6	5	4	3	2	1	0
DAC_GAIN							
R/W-30h							

Table 7-20. DIG_VOL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DAC_GAIN	R/W	30h	Digital Volume Control These bits control the digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 8'b00000000: +24.0 dB 8'b00000001: +23.5 dB … 8'b00101111: +0.5 dB **8'b00110000: 0.0 dB** 8'b00110001: -0.5 dB ... 8'b11111110: -103 dB 8'b11111111: Mute

7.1.19 DIG_VOL_CTRL2 Register (Offset = 4Eh) [Reset = 33h]

Return to the Summary Table.

Digital volume control 2

Figure 7-19. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
VNUS		VNUF		VNDS		VNDF	
R/W-0h		R/W-3h		R/W-0h		R/W-3h	

Table 7-21. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VNUS	R/W	0h	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VNUF	R/W	3h	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update **11: Decrement by 0.5 dB for each update**
3-2	VNDS	R/W	0h	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	VNDF	R/W	3h	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update **11: Increment by 0.5 dB for each update**

7.1.20 DIG_VOL_CTRL3 Register (Offset = 4Fh) [Reset = 30h]

Return to the Summary Table.

Digital volume control 3

Figure 7-20. DIG_VOL_CTRL3 Register

7	6	5	4	3	2	1	0
VEDS		VEDF		RESERVED			
R/W-0h		R/W-3h		R/W-0h			

Table 7-22. DIG_VOL_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VEDS	R/W	0h	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VEDF	R/W	3h	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update **11: Decrement by 0.5 dB for each update**
3-0	RESERVED	R/W	0h	

7.1.21 AUTO_MUTE_CTRL Register (Offset = 50h) [Reset = 07h]

Return to the Summary Table.

Auto mute control

Figure 7-21. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					AM_CTL	AMUTE_CH2	AMUTE_CH1
R/W-0h					R/W-1h	R/W-1h	R/W-1h

Table 7-23. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	AM_CTL	R/W	1h	0: Auto mute ch1 and ch2 independently **1: Auto mute ch1 and ch2 only when both channels are about to be auto muted**
1	AMUTE_CH2	R/W	1h	Auto Mute Channel 2 This bit enables or disables auto mute on Channel 2 0: Disable Channel 2 auto mute **1: Enable Channel 2 auto mute**
0	AMUTE_CH1	R/W	1h	Auto Mute Channel 1 This bit enables or disables auto mute on Channel 1 0: Disable Channel 1 auto mute **1: Enable Channel 1 auto mute**

7.1.22 AUTO_MUTE_TIME Register (Offset = 51h) [Reset = 00h]

Return to the Summary Table.

Auto mute time

Figure 7-22. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	CH1_AMT			RESERVED	CH2_AMT		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 7-24. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	CH1_AMT	R/W	0h	Auto Mute Time for Channel 1 These bits specify the length of consecutive zero samples at ch1 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. **000: 11.5 ms** 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0h	
2-0	CH2_AMT	R/W	0h	Auto Mute Time for Channel 2 These bits specify the length of consecutive zero samples at ch2 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. **000: 11.5 ms** 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

7.1.23 ANA_CTRL Register (Offset = 53h) [Reset = 00h]

Return to the Summary Table.

Analog control

Figure 7-23. ANA_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	BW_CTL		RESERVED				PHASE_CTL
R/W-0h	R/W-0h		R/W-0h				R/W-0h

Table 7-25. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-5	BW_CTL	R/W	0h	Class D Loop Bandwidth **00: 100kHz** 01: 80kHz 10: 120kHz 11: 175kHz When Fsw=384kHz, 100kHz bandwidth is selected for high audio performance. With Fsw=768kHz, 175kHz bandwidth should be selected for high audio performance.
4-1	RESERVED	R/W	0h	
0	PHASE_CTL	R/W	0h	**0: Out of phase** 1: In phase

7.1.24 AGAIN Register (Offset = 54h) [Reset = 00h]

Return to the Summary Table.

Analog gain

Figure 7-24. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED			AGAIN				
R/W-0h			R/W-0h				

Table 7-26. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-0	AGAIN	R/W	0h	Analog Gain Control This bit controls the analog gain **00000: 0 dB** 00001:-0.5 dB …… 11111: -15.5 dB

7.1.25 ADC_RPT Register (Offset = 5Eh) [Reset = 00h]

Return to the Summary Table.

ADC(PVDD voltage) report

Figure 7-25. ADC_RPT Register

7	6	5	4	3	2	1	0
PVDD_RPT							
R-0h							

Table 7-27. ADC_RPT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PVDD_RPT	R	0h	PVDD ADC reading. Each LSB means 0.12V For PVDD = 12V, the AD data = 8'b 01100100 For PVDD = 24V, the AD data = 8'b 11001000

7.1.26 GPIO_CTRL Register (Offset = 60h) [Reset = 00h]

Return to the Summary Table.

GPIO control

Figure 7-26. GPIO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					GPIO0OE	GPIO2OE	GPIO1OE
R/W-0h					R/W-0h	R/W-0h	R/W-0h

Table 7-28. GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	GPIO0OE	R/W	0h	GPIO0 Output Enable This bit sets the direction of the GPIO0 pin **0: GPIO0 is input** 1: GPIO0 is output
1	GPIO2OE	R/W	0h	GPIO2 Output Enable This bit sets the direction of the GPIO2 pin **0: GPIO2 is input** 1: GPIO2 is output
0	GPIO1OE	R/W	0h	GPIO1 Output Enable This bit sets the direction of the GPIO1 pin **0: GPIO1 is input** 1: GPIO1 is output

7.1.27 GPIO1_SEL Register (Offset = 61h) [Reset = 00h]

Return to the Summary Table.

GPIO1 output selection

Figure 7-27. GPIO1_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO1SEL			
R/W-0h				R/W-0h			

Table 7-29. GPIO1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-0	GPIO1SEL	R/W	0h	**4'b0000: off (low)** 4'b1000: GPIO1 as WARNZ output 4'b1011: GPIO1 as FAULTZ output 4'b1100: GPIO1 as PVDD_DROP_DETECTION 4'b1101: GPIO1 as Serial audio interface data output (SDOUT) 4'b1110: GPIO1 as RAMP clk Others reserved

7.1.28 GPIO2_SEL Register (Offset = 62h) [Reset = 00h]

Return to the Summary Table.

GPIO2 output selection

Figure 7-28. GPIO2_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO2SEL			
R/W-0h				R/W-0h			

Table 7-30. GPIO2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-0	GPIO2SEL	R/W	0h	**0000: off (low)** 1000: GPIO2 as WARNZ output 1011: GPIO2 as FAULTZ output 1100: GPIO2 as PVDD_UV_DETECTION 1101: GPIO2 as Serial audio interface data output (SDOUT) 1110: GPIO2 as RAMP clk Others reserved

7.1.29 GPIO0_SEL Register (Offset = 63h) [Reset = 00h]

Return to the Summary Table.

GPIO0 output selection

Figure 7-29. GPIO0_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO0_SEL			
R/W-0h				R/W-0h			

Table 7-31. GPIO0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-0	GPIO0_SEL	R/W	0h	**4'b0000: off (low)** 4'b1000: GPIO0 as WARNZ output 4'b1011: GPIO0 as FAULTZ output 4'b1100: GPIO0 as PVDD_DROP_DETECTION 4'b1101: GPIO0 as Serial audio interface data output (SDOUT) 4'b1110: GPIO0 as RAMP clk 4'b1111: Reserved

7.1.30 GPIO_INPUT_SEL Register (Offset = 64h) [Reset = 00h]

Return to the Summary Table.

GPIO input selection

Figure 7-30. GPIO_INPUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED		GPIOSYNC_SEL		GPIORST_SEL		GPIOM_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 7-32. GPIO_INPUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	GPIOSYNC_SEL	R/W	0h	**00: N/A** 01: GPIO1 10: GPIO2 11: GPIO0
3-2	GPIORST_SEL	R/W	0h	**00: N/A** 01: GPIO1 10: GPIO2 11: GPIO0
1-0	GPIOM_SEL	R/W	0h	**00: N/A** 01: GPIO1 10: GPIO2 11: GPIO0

7.1.31 MISC_CTRL1 Register (Offset = 65h) [Reset = 00h]

D

Return to the Summary Table.

misc control 1

Figure 7-31. MISC_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED					GPIO_OUTPUT		
R/W					R/W		

Table 7-33. MISC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2-0	GPIO_OUTPUT	R/W	0h	bit0: GPIO1 output bit1: GPIO2 output bit2: GPIO0 output

7.1.32 MISC_CTRL2 Register (Offset = 66h) [Reset = 00h]

Return to the Summary Table.

misc control 2

Figure 7-32. MISC_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED					GPIO_INV		
R/W					R/W		

Table 7-34. MISC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2-0	GPIO_OUTPUT	R/W	0h	bit0: GPIO1 output invert bit1: GPIO2 output invert bit2: GPIO0 output invert

7.1.33 DIE_ID Register (Offset = 67h) [Reset = 98h]

Return to the Summary Table.

DIE ID

Figure 7-33. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R-98h							

Table 7-35. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	98h	Die ID for TAS5830.

7.1.34 POWER_STATE Register (Offset = 68h) [Reset = 00h]

Return to the Summary Table.

Power State

Figure 7-34. POWER_STATE Register

7	6	5	4	3	2	1	0
RESERVED						STATE_RPT	
R-0h						R-0h	

Table 7-36. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1-0	STATE_RPT	R	0h	**00: Deep sleep** 01: Sleep 10: Hi-Z 11: Play others: reserved

7.1.35 AUTOMUTE_STATE Register (Offset = 69h) [Reset = 00h]

Return to the Summary Table.

Auto mute state

Figure 7-35. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						CH2MUTE_STATUS	CH1MUTE_STATUS
R-0h						R-0h	R-0h

Table 7-37. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	CH2MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 2. **0: Not auto muted** 1: Auto muted
0	CH1MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 1. **0: Not auto muted** 1: Auto muted

7.1.36 RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h]

Return to the Summary Table.

Switching clock phase control

Figure 7-36. RAMP_PHASE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				RAMPPHASE_SEL		RAMPSYNC_SEL	RAMPSYNC_EN
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Table 7-38. RAMP_PHASE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-2	RAMPPHASE_SEL	R/W	0h	Select ramp clock phase when multi devices are integrated in one system to reduce EMI and peak supply peak current, it is recomended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. **00: 0 degree** 01: 45 degree 10: 90 degree 11: 135 degree all of above have a 45 degree of phase shift
1	RAMPSYNC_SEL	R/W	0h	Ramp phase sync source **0: GPIO sync** 1: Internal sync
0	RAMPSYNC_EN	R/W	0h	1: Enable ramp phase sync **0: Disable ramp phase sync**

7.1.37 RAMP_SS_CTRL0 Register (Offset = 6Bh) [Reset = 00h]

Return to the Summary Table.

Spread spectrum control 0

Figure 7-37. RAMP_SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED						RDM_EN	TRI_EN
R/W-0h						R/W-0h	R/W-0h

Table 7-39. RAMP_SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	RDM_EN	R/W	0h	1: Random SS enable **0: Random SS disable**
0	TRI_EN	R/W	0h	1: Triangle SS enable **0: Triangle SS disable**

7.1.38 RAMP_SS_CTRL1 Register (Offset = 6Ch) [Reset = 00h]

Return to the Summary Table.

Spread spectrum control 1

Figure 7-38. RAMP_SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RDM_CTL			TRI_CTL			
R/W-0h	R/W-0h			R/W-0h			

Table 7-40. RAMP_SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	RDM_CTL	R/W	0h	Random SS range control For Fsw of 384kHz **3'b000: SS range +/- 0.62%** 3'b010: SS range +/- 1.88% 3'b011: SS range +/- 4.38% 3'b100: SS range +/- 9.38% 3'b101: SS range +/- 19.38% Others: reserved For Fsw of 576kHz 3'b000: SS range +/- 0.95% 3'b010: SS range +/- 2.86% 3'b011: SS range +/- 6.67% 3'b100: SS range +/- 14.29% 3'b101: SS range +/- 29.52% Others: reserved
3-0	TRI_CTL	R/W	0h	Triangle SS frequency and range control **4'b0000: 24kHz SS +/- 5%** 4'b0001: 24kHz SS +/- 10% 4'b0010: 24kHz SS +/- 20% 4'b0011: 24kHz SS +/- 25% 4'b0100: 48kHz SS +/- 5% 4'b0101: 48kHz SS +/- 10% 4'b0110: 48kHz SS +/- 20% 4'b0111: 48kHz SS +/- 25% 4'b1000: 32kHz SS +/- 5% 4'b1001: 32kHz SS +/- 10% 4'b1010: 32kHz SS +/- 20% 4'b1011: 32kHz SS +/- 25% 4'b1100: 16kHz SS +/- 5% 4'b1101: 16kHz SS +/- 10% 4'b1110: 16kHz SS +/- 20% 4'b1111: 16kHz SS +/- 25%

7.1.39 CHAN_FAULT Register (Offset = 70h) [Reset = 00h]

Return to the Summary Table.

Channel fault

Figure 7-39. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1DC	CH2DC	CH1OC	CH2OC
R-0h				R-0h	R-0h	R-0h	R-0h

Table 7-41. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	CH1DC	R	0h	Channel 1 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
2	CH2DC	R	0h	Channel 2 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	CH1OC	R	0h	Channel 1 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	CH2OC	R	0h	Channel 2 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

7.1.40 GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h]

Return to the Summary Table.

Global fault 1

Figure 7-40. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
RESERVED	BQWRTFAULT_FLAG	EEPROMFAULT_FLAG	RESERVED		CLKFAULT_FLAG	PVDDOV_FLAG	PVDDUV_FLAG
R-0h	R-0h	R-0h	R-0h		R-0h	R-0h	R-0h

Table 7-42. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	BQWRTFAULT_FLAG	R	0h	**0: The recent BQ is written successfully** 1: The recent BQ writed failed
5	EEPROMFAULT_FLAG	R	0h	**0: EEPROM boot load was done successfully** 1: EEPROM boot load was done unsuccessfully
4-3	RESERVED	R	0h	
2	CLKFAULT_FLAG	R	0h	Clock fault. Once there is a Clock fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clock fault works with an auto-recovery mode, once the clock error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	PVDDOV_FLAG	R	0h	PVDD OV fault. Once there is a OV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	PVDDUV_FLAG	R	0h	PVDD UV fault. Once there is a UV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). UV fault works with an auto-recovery mode, once the UV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

7.1.41 GLOBAL_FAULT2 Register (Offset = 72h) [Reset = 00h]

Return to the Summary Table.

Global fault 2

Figure 7-41. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED					CH2CBC_FLAG	CH1CBC_FLAG	OTSD_FLAG
R-0h					R-0h	R-0h	R-0h

Table 7-43. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	CH2CBC_FLAG	R	0h	**0: No CBC fault on Channel 2** 1: CBC fault triggered on Channel 2
1	CH1CBC_FLAG	R	0h	**0: No CBC fault on Channel 1** 1: CBC fault triggered on Channel 1
0	OTSD_FLAG	R	0h	Over temperature shut down fault Once there is a OT fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an autorecovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

7.1.42 WARNING Register (Offset = 73h) [Reset = 00h]

Return to the Summary Table.

Warning

Figure 7-42. WARNING Register

7	6	5	4	3	2	1	0
RESERVED		CH1CBCW_FLAG	CH2CBCW_FLAG	OTW4_FLAG	OTW3_FLAG	OTW2_FLAG	OTW1_FLAG
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-44. WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	CH1CBCW_FLAG	R	0h	**0: No CBC warning on Channel 1** 1: CBC warning triggered on Channel 1
4	CH2CBCW_FLAG	R	0h	**0: No CBC warning on Channel 2** 1: CBC warning triggered on Channel 2
3	OTW4_FLAG	R	0h	**0: No temperature level 4 warning** 1: Over temperature warning level 4 is triggered
2	OTW3_FLAG	R	0h	**0: No temperature level 3 warning** 1: Over temperature warning level 3 is triggered
1	OTW2_FLAG	R	0h	**0: No temperature level 2 warning** 1: Over temperature warning level 2 is triggered
0	OTW1_FLAG	R	0h	**0: No temperature level 1 warning** 1: Over temperature warning level 1 is triggered

7.1.43 PIN_CONTROL1 Register (Offset = 74h) [Reset = 00h]

Return to the Summary Table.

Pin control 1

Figure 7-43. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDDUV	MASK_DVDDOV	MASK_CLKERROR	MASK_PVDDUV	MASK_PVDDOV	MASK_DC	MASK_OC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-45. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0h	**0: Enable OTSD fault report** 1: Mask OTSD fault report
6	MASK_DVDDUV	R/W	0h	**0: Enable DVDD UV fault report** 1: Mask DVDD UV report
5	MASK_DVDDOV	R/W	0h	**0: Enable DVDD OV fault report** 1: Mask DVDD OV fault report
4	MASK_CLKERROR	R/W	0h	**0: Enable CLK fault report** 1: Mask CLK fault report
3	MASK_PVDDUV	R/W	0h	**0: Enable UV fault report** 1: Mask UV fault report
2	MASK_PVDDOV	R/W	0h	**0: Enable OV fault report** 1: Mask OV fault report
1	MASK_DC	R/W	0h	**0: Enable DC fault report** 1: Mask DC fault report
0	MASK_OC	R/W	0h	**0: Enable OC fault report** 1: Mask OC fault report

7.1.44 PIN_CONTROL2 Register (Offset = 75h) [Reset = F8h]

Return to the Summary Table.

Pin control 2

Figure 7-44. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
CBCFAULTLATCH_EN	CBCWARNLATCH_EN	CLKFAULTLATCH_EN	OTSDLATCH_EN	OTWLATCH_EN	MASK_OTW	MASK_CBCWARN	MASK_CBCFAULT
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 7-46. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CBCFAULTLATCH_EN	R/W	1h	0: Disable CBC fault latch **1: Enable CBC fault latch**
6	CBCWARNLATCH_EN	R/W	1h	0: Disable CBC warning latch **1: Enable CBC warning latch**
5	CLKFAULTLATCH_EN	R/W	1h	0: Disable CLK fault latch **1: Enable CLK fault latch**
4	OTSDLATCH_EN	R/W	1h	0: Disable OTSD fault latch **1: Enable OTSD fault latch**
3	OTWLATCH_EN	R/W	1h	0: Disable OTW warning latch **1: Enable OTW warning latch**
2	MASK_OTW	R/W	0h	**0: Enable OTW warning report** 1: Mask OTW warning report
1	MASK_CBCWARN	R/W	0h	**0: Enable CBC warning report** 1: Mask CBC warning report
0	MASK_CBCFAULT	R/W	0h	**0: Enable CBC fault report** 1: Mask CBC fault report

7.1.45 MISC_CONTROL3 Register (Offset = 76h) [Reset = 00h]

Return to the Summary Table.

MISC control 3

Figure 7-45. MISC_CONTROL3 Register

7	6	5	4	3	2	1	0
CLKDET_LATCH	RESERVED		OTSD_AUTOREC	RESERVED			
R/W-0h	R/W-0h		R/W-0h	R/W-0h			

Table 7-47. MISC_CONTROL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLKDET_LATCH	R/W	0h	1:Latch clock detection status **0:No latch clock detection status**
6-5	RESERVED	R/W	0h	
4	OTSD_AUTOREC	R/W	0h	**0: Disable OTSD auto recovery** 1: Enable OTSD auto recovery
3-0	RESERVED	R/W	0h	

7.1.46 CBC_CONTROL Register (Offset = 77h) [Reset = 00h]

Return to the Summary Table.

CBC control

Figure 7-46. CBC_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED			CBCLEVEL_SEL		CBC_EN	CBCWARN_EN	CBCFAULT_EN
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h

Table 7-48. CBC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	CBCLEVEL_SEL	R/W	0h	These bits set Cycle-By-Cycle current limiting level, which is a percentage of the Over-Current Threshold: **2b'00: 80%** 2b'10: 60% 2b'01: 40% 2b'11: reserved
2	CBC_EN	R/W	0h	**0: Disable CBC function** 1: Enable CBC function
1	CBCWARN_EN	R/W	0h	**0: Disable CBC warning** 1: Enable CBC warning
0	CBCFAULT_EN	R/W	0h	**0: Disable CBC fault** 1: Enable CBC fault

7.1.47 FAULT_CLEAR Register (Offset = 78h) [Reset = 00h]

Return to the Summary Table.

Fault clear

Figure 7-47. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
FAULT_CLR	RESERVED						
W-0h	W-0h						

Table 7-49. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT_CLR	W	0h	WRITE CLEAR BIT **0: No fault clear** 1: Clear analog fault
6-0	RESERVED	W	0h	

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Applications

8.1.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

Figure 8-1 shows the 2.0 (Stereo BTL) system application.

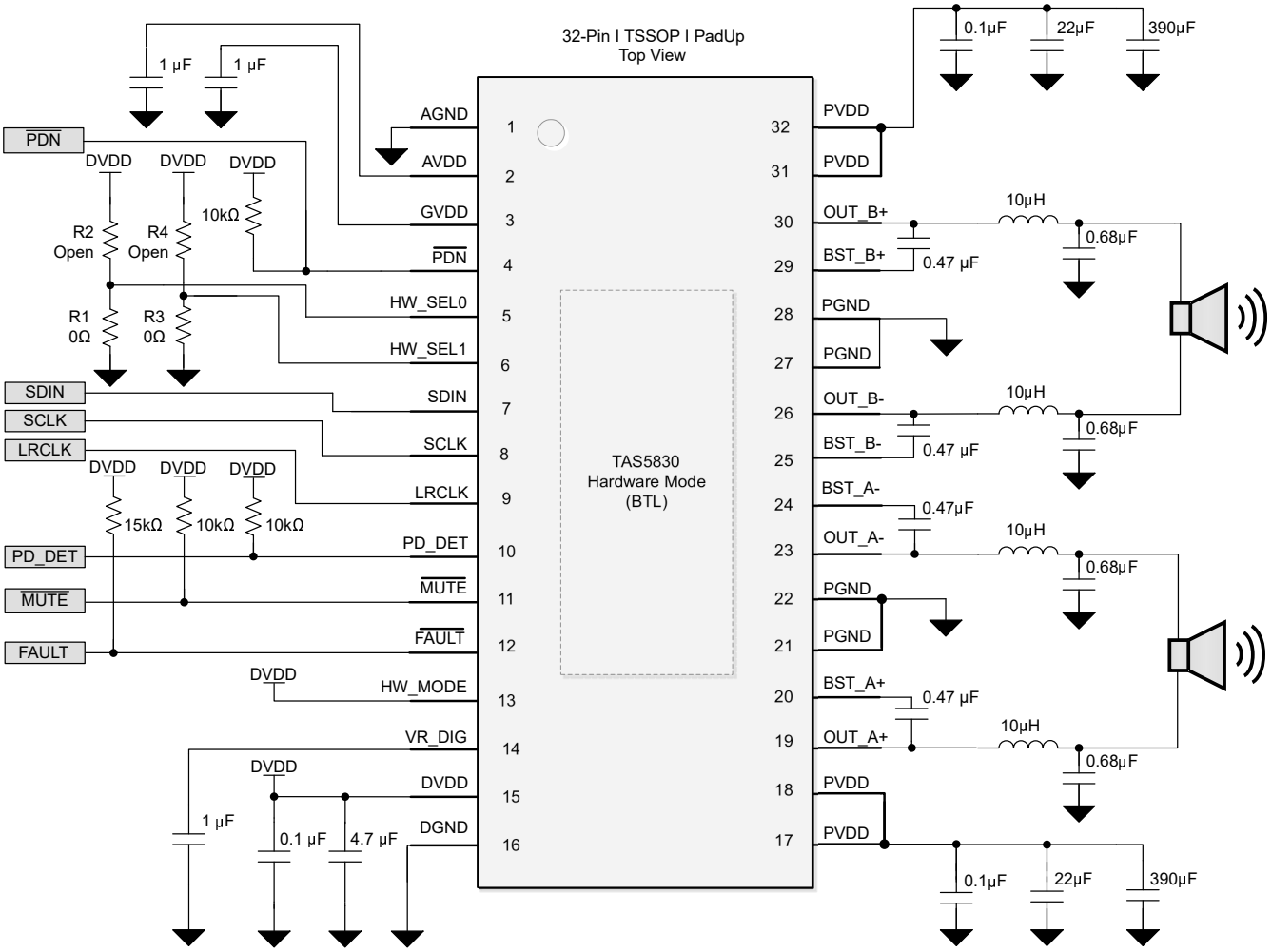


Figure 8-1. 2.0 (Stereo BTL) System Application Schematic

8.1.2 Mono (PBTL) Systems

In Mono mode, TAS5830 can be used as PBTL mode to drive sub-woofer with more output power.

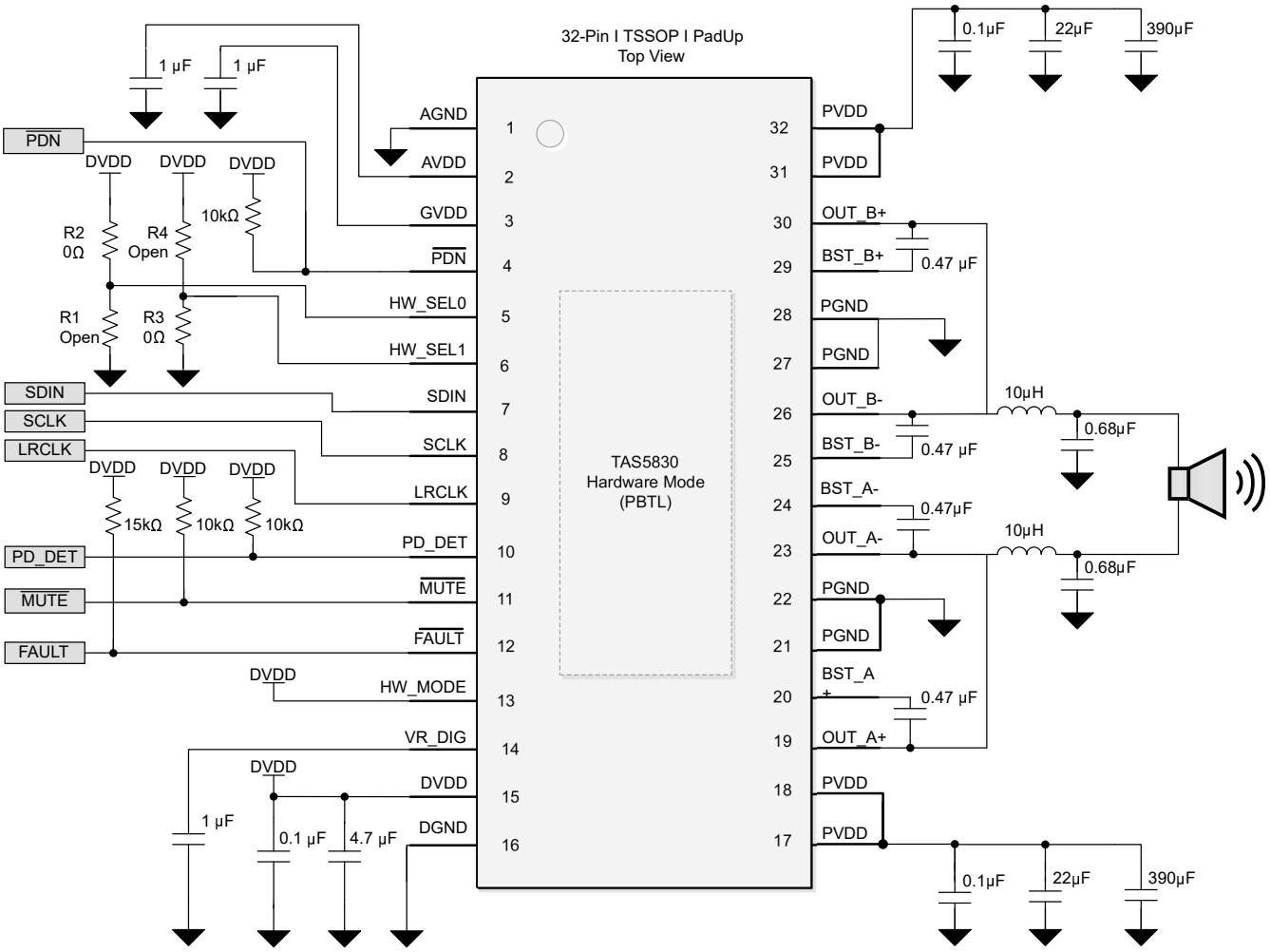


Figure 8-2. Sub-woofer (PBTL) Application Schematic

8.2 Power Supply Recommendations

The TAS5830 device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the Section 5.3 table. The two power supplies do not have a required power up sequence. The power supplies can be powered on in any order.

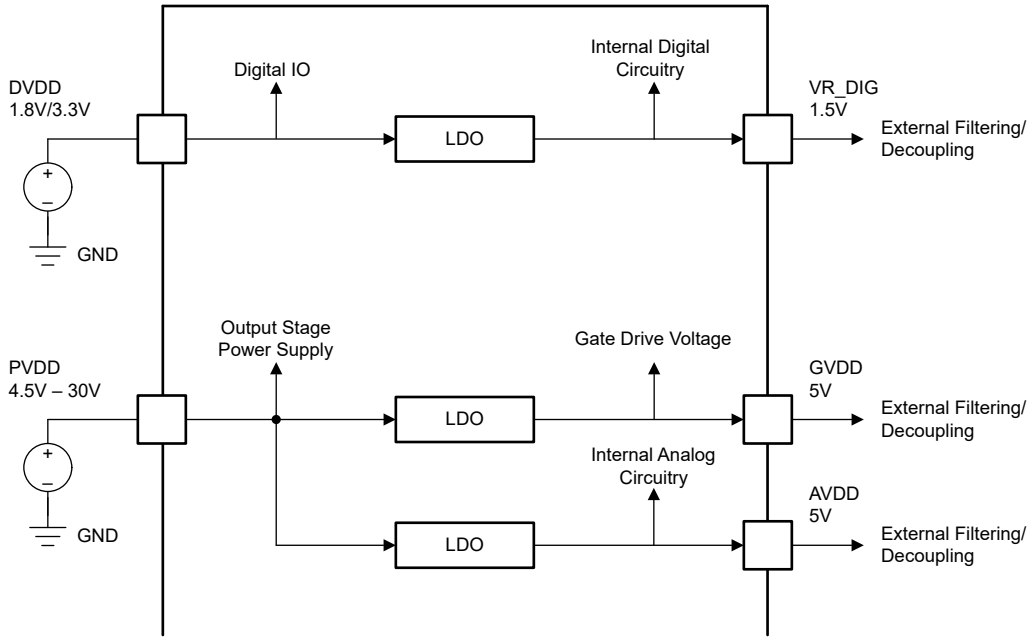


Figure 8-3. Power Supply Functional Block Diagram

8.2.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in Power Supply Functional Block Diagram, the DVDD supply provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the *Section 8* section and the *Section 8.3.2* section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5830 device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and the output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. Note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and is not to be used to power any additional external circuitry. Additional loading on this pin can cause the voltage to sag, negatively affecting the performance and operation of the device.

8.2.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5830EVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5830 device *Importance of PVDD Bypass Capacitor Placement on PVDD Network*. Lack of proper decoupling, like that shown in the *Importance of PVDD Bypass Capacitor Placement on PVDD Network*, results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply that is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5830 internal circuitry. It is

important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

8.3 Layout

8.3.1 Layout Guidelines

8.3.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to the layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

The guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in *Section 8.3.2*. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, design size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, TI recommends to start from the guidance shown in *Section 8.3.2* and work with TI field application engineers or through the E2E community to modify the example based upon the application specific goals.

8.3.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, GVDD and PVDD. However, the capacitors on the PVDD net for the TAS5830 device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only dose placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5830 device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the Section 5.1 table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from the associated PVDD pins than what is shown in the example layouts in the *Section 8.3.2* section.

8.3.1.3 Optimizing Thermal Performance

Follow the Layout Example section to achieve the best balance of design size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. The system designer maintains that the heat can get out of the device and into the ambient air surrounding the device. The TAS5830 device utilizes a TSSOP-DAD, pad up, package to maximize the thermal dissipation away from the device. Heat is transferred from the device to the ambient air through a low impedance heat sink path. The use of a heat sink is required. TI recommends using ATS-TI10P-519-C1-R3 from www.qats.com, shown in Figure 8-4. The size of the heat sink can deviate from the suggested heat sink in space constrained environments, but thermal performance can degrade.

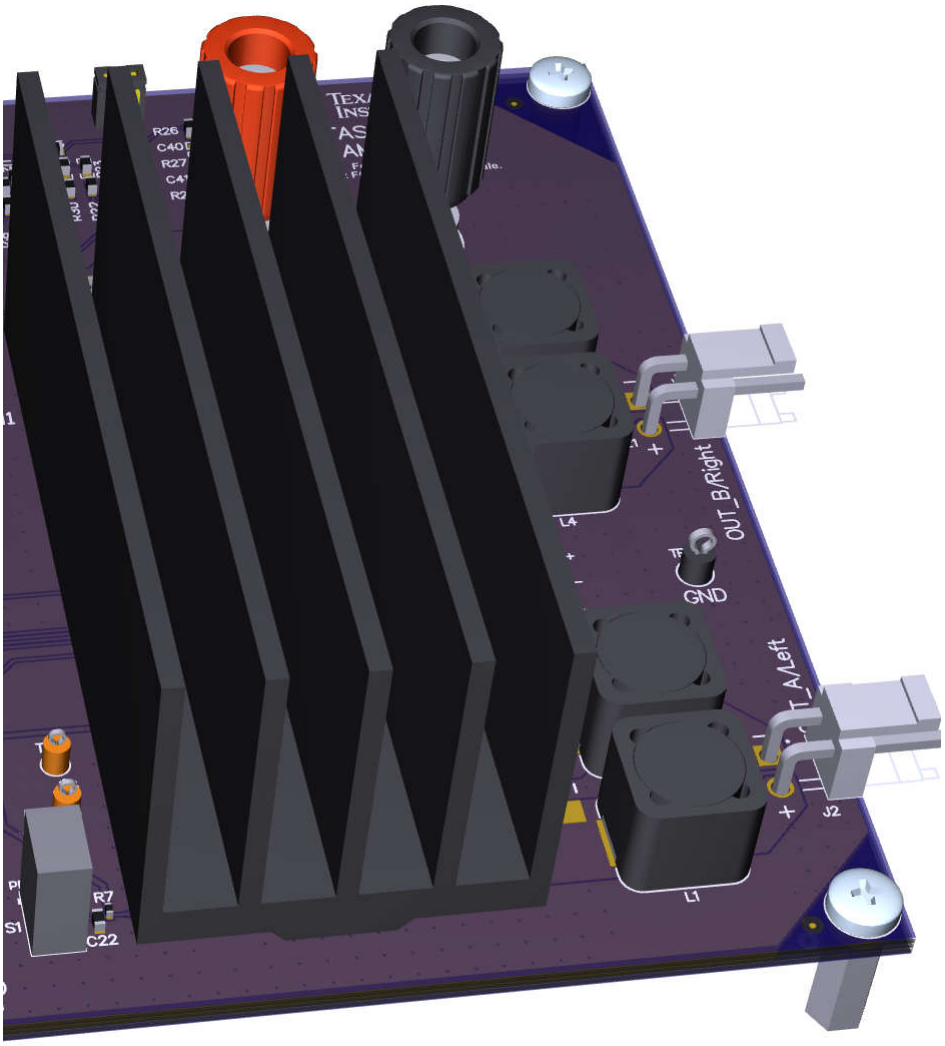


Figure 8-4. 2.0 (Stereo BTL) EVM 3D Top View with Heatsink

8.3.2 Layout Example

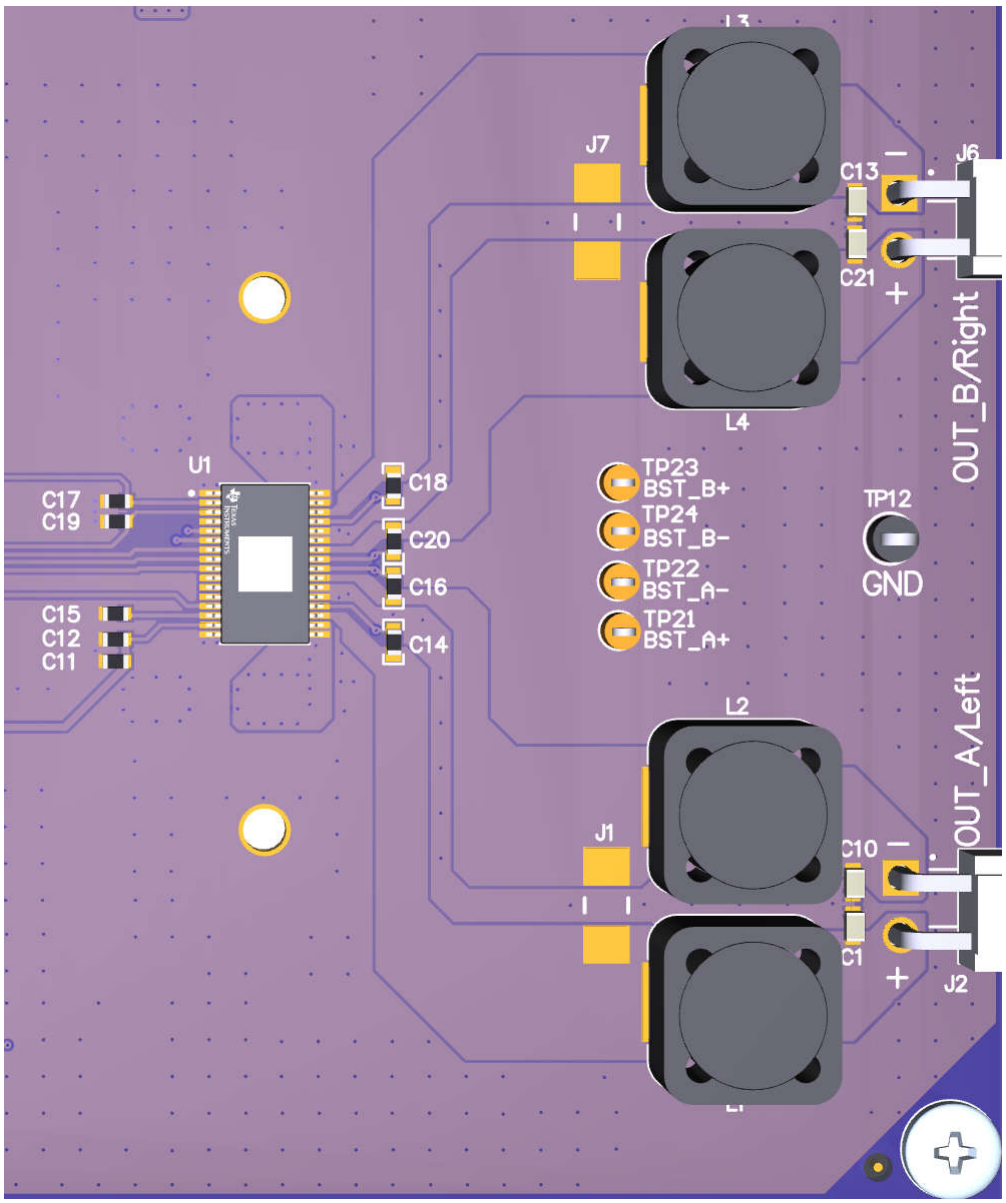
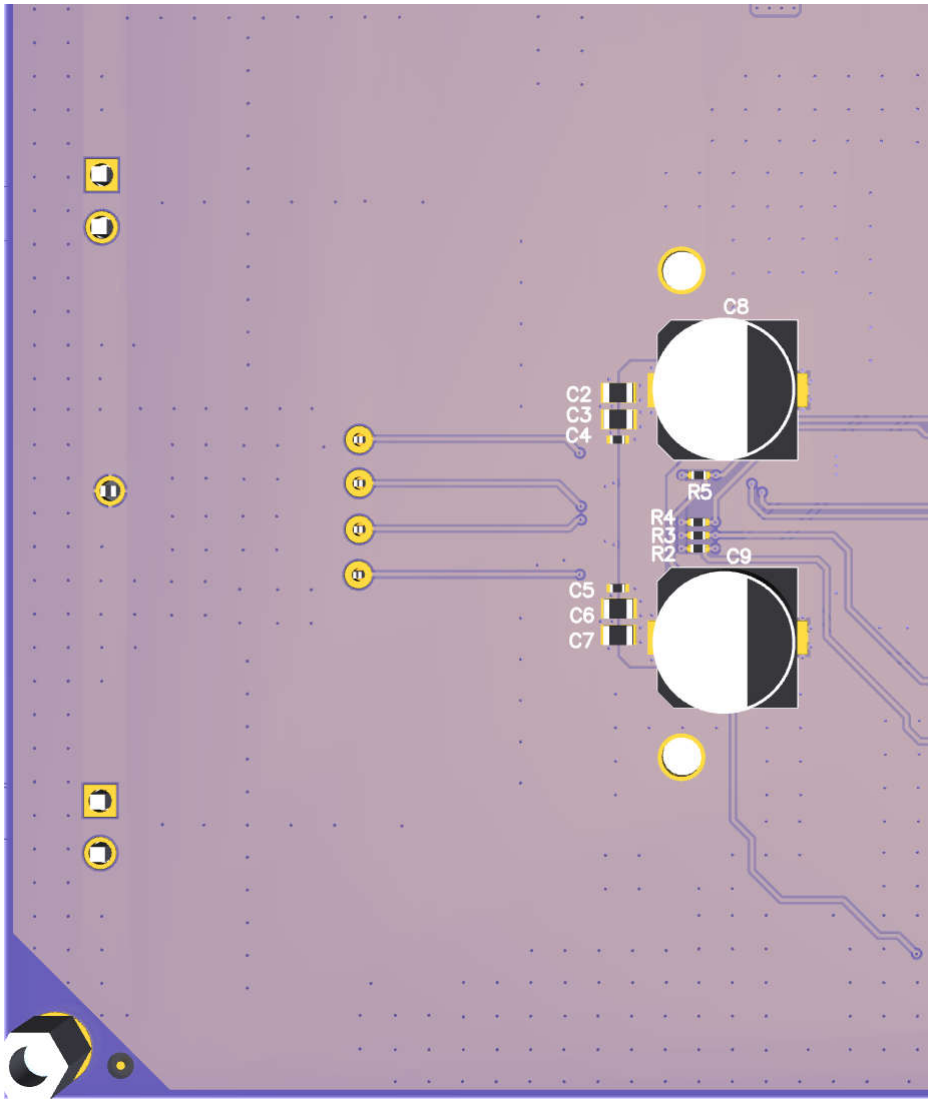


Figure 8-5. 2.0 (Stereo BTL) 3-D Top View



Note

From bottom view. Flipped along Y-axis.

Figure 8-6. 2.0 (Stereo BTL) 3-D Bottom View

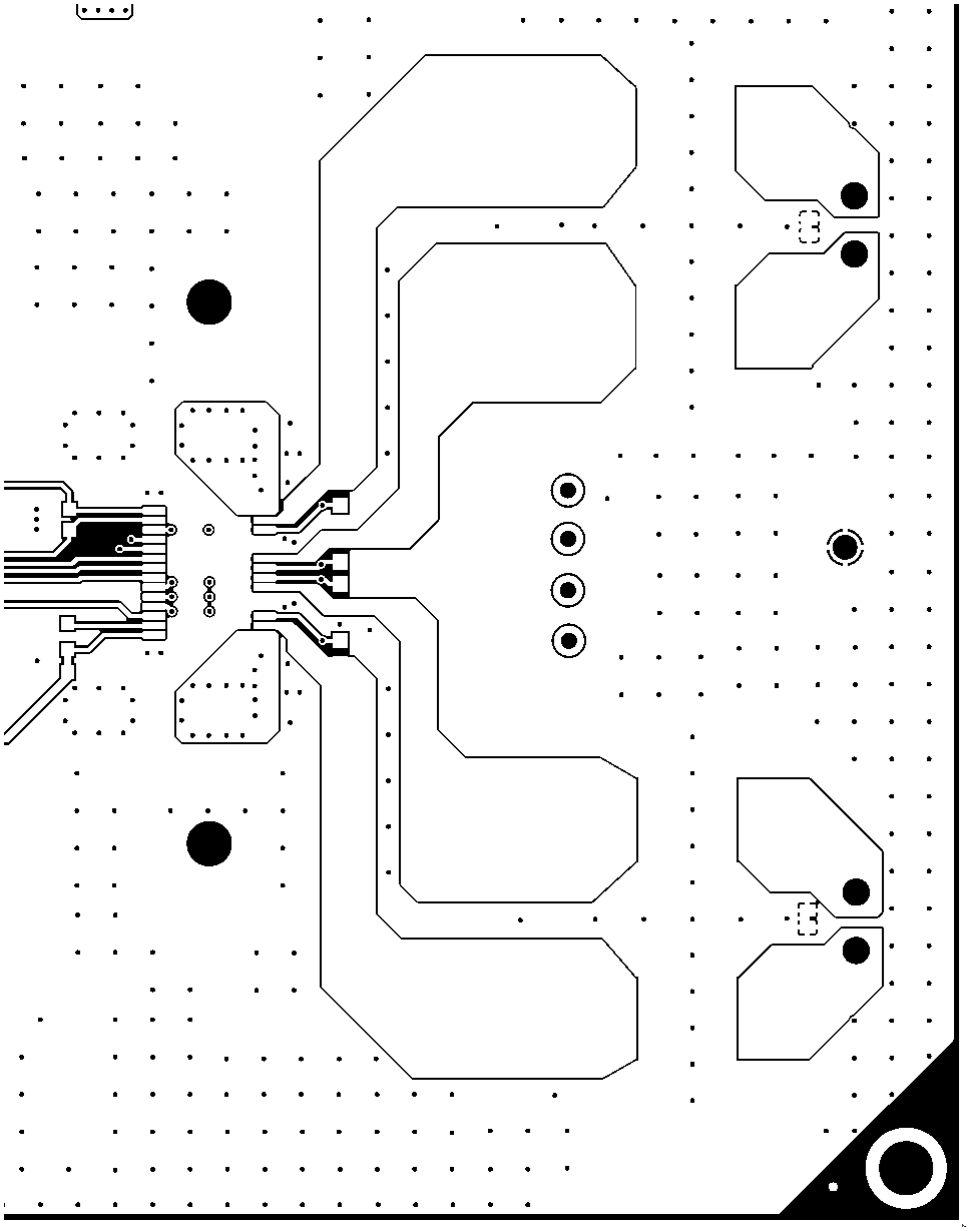


Figure 8-7. 2.0 (Stereo BTL) PCB Top Layer Plot (Top View)

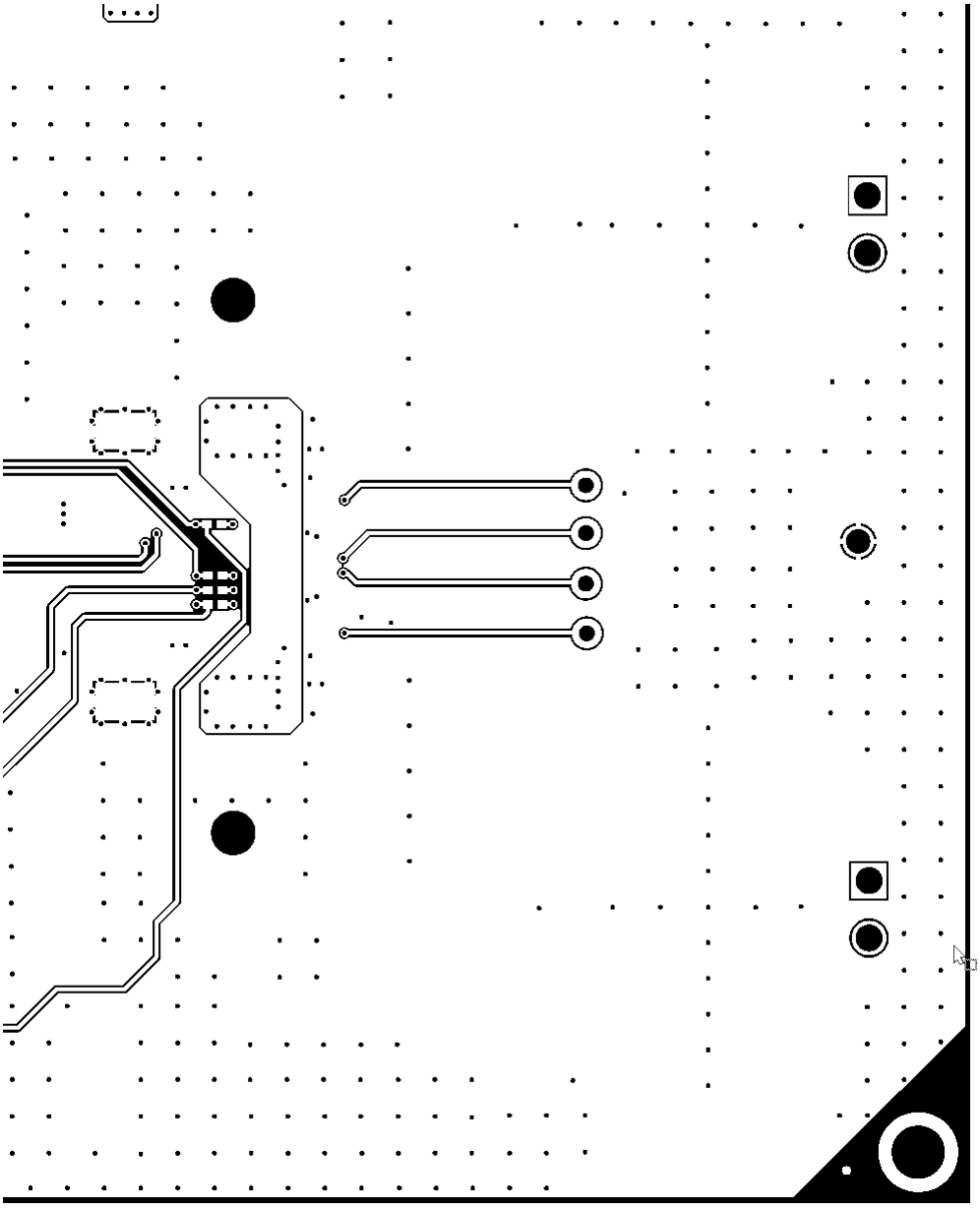


Figure 8-8. 2.0 (Stereo BTL) PCB Bottom Layer Plot (Top View)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

The glossary section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplfier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. The pin is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to device which serves as a central system controller, providing control information to devices connected to the host processor as well as gathering audio source data from devices upstream from the host processor and distributing the data to other devices. This device often configures the controls of the audio processing devices (like the TAS5830) in the audio path to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that the temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$r_{DS(on)}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

9.1.2 Development Support

For RDGUI software, please consult your local field support engineer.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5830DADR	Active	Production	HTSSOP (DAD) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	5830

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

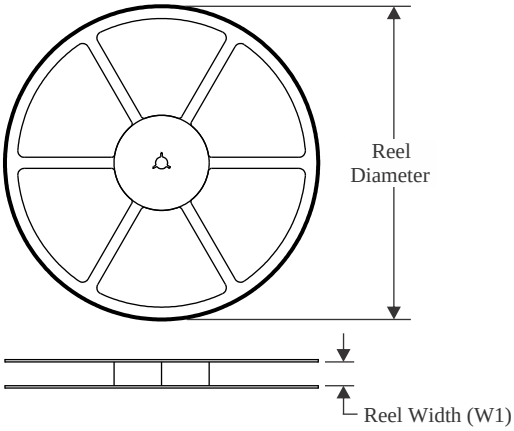
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

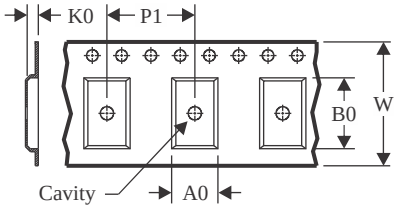
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

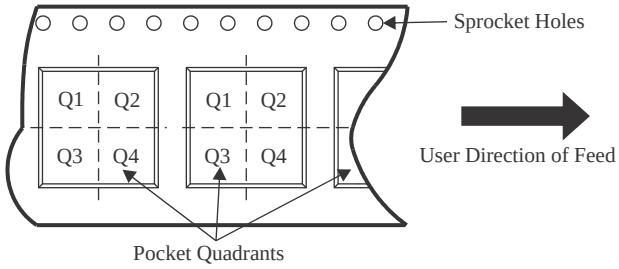


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

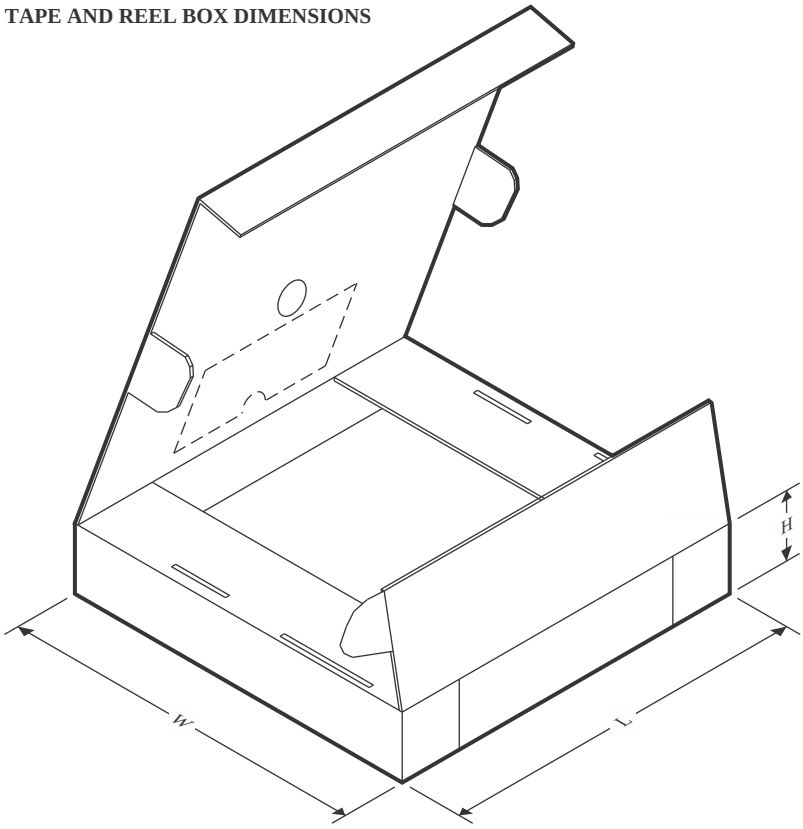
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5830DADR	HTSSOP	DAD	32	2000	330.0	24.4	8.8	11.8	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

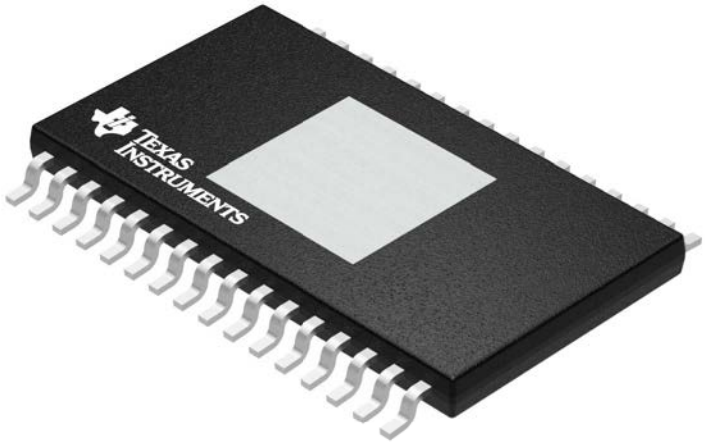


*All dimensions are nominal

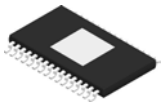
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5830DADR	HTSSOP	DAD	32	2000	356.0	356.0	45.0

DAD 32 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

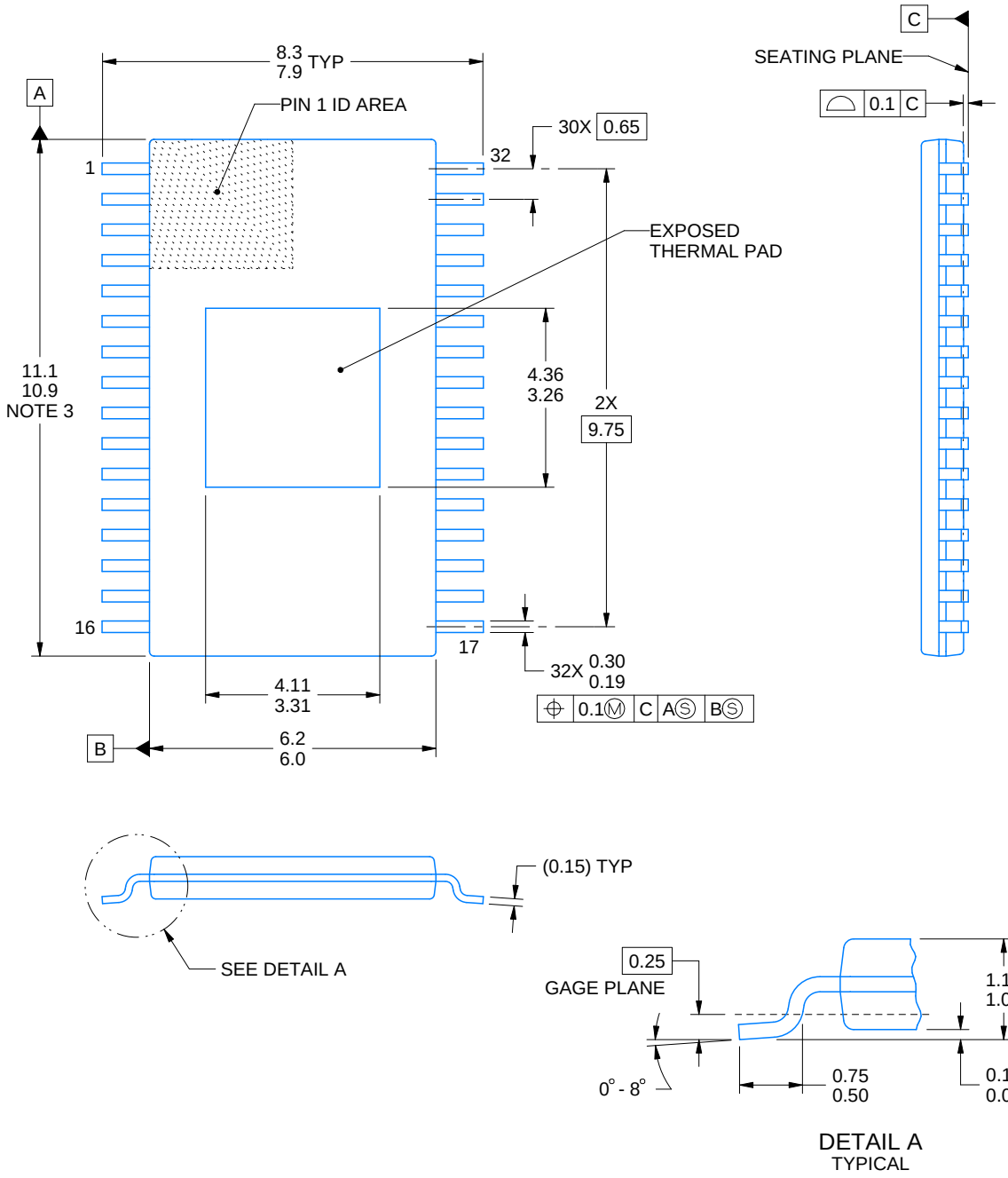


PACKAGE OUTLINE

DAD0032A

PowerPAD ™TSSOP - 1.15 mm max height

PLASTIC SMALL OUTLINE

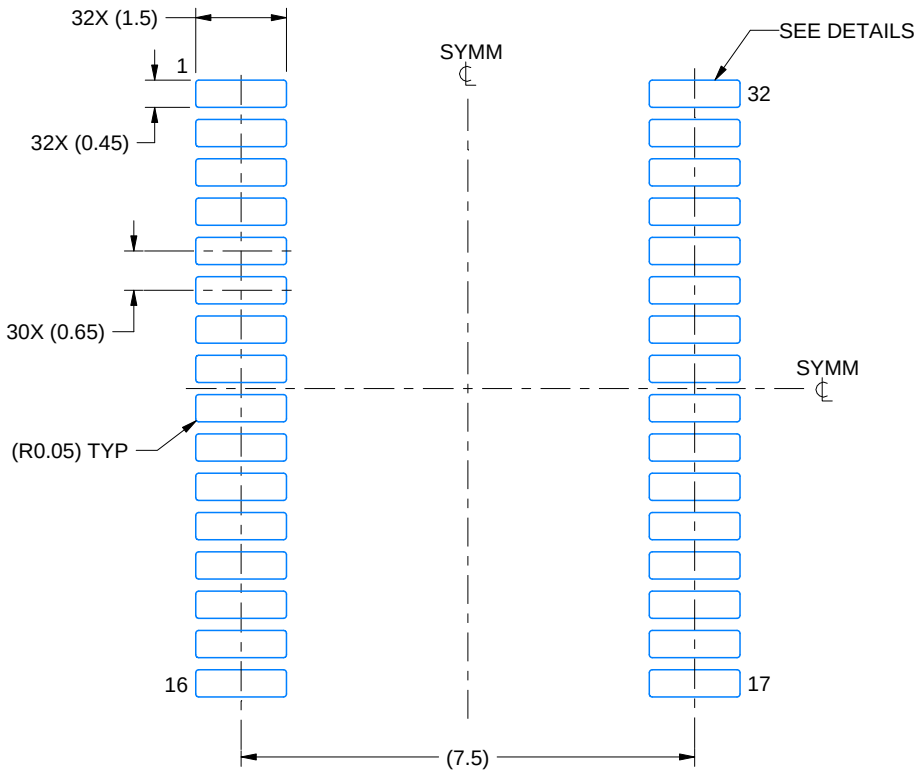


4222646/B 02/2020

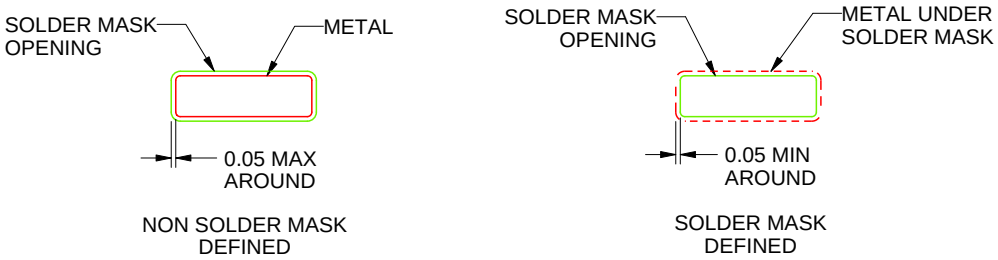
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:8X

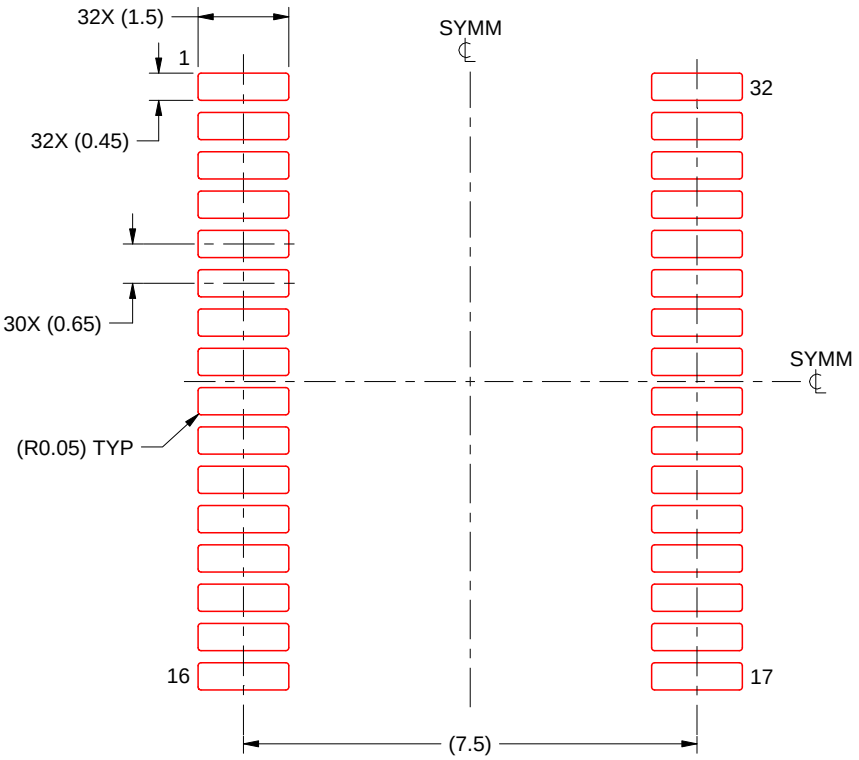


SOLDER MASK DETAILS
NOT TO SCALE

4222646/B 02/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222646/B 02/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265