SLRS028A - SEPTEMBER 1988 - REVISED NOVEMBER 2004

- Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds
- Output Supply Voltage Range From 5 V to 24 V
- Low Standby Power Dissipation
- V<sub>CC3</sub> Supply Maximizes Output Source Voltage

#### description/ordering information

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

#### **DORNPACKAGE** (TOP VIEW) $V_{CC1}$ $V_{CC2}$ 15∏ 4Y 1Y 14 A 1A 3 1E1 4 13∏ 2E2 12 1 2E1 1E2 11 1 3A 2A 2Y 10 3Y 8 **GND** 9 V<sub>CC3</sub>

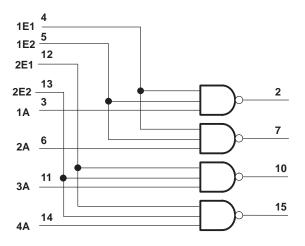
The outputs can be switched very close to the  $V_{CC2}$  supply rail when  $V_{CC3}$  is about 3 V higher than  $V_{CC2}$ .  $V_{CC3}$  also can be tied directly to  $V_{CC2}$  when the source voltage requirements are lower.

#### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP (N)	Tube of 25	SN75374N	SN75374N	
0°C to 70°C	COIC (D)	SOIC (D) Tube of 40		SN75374D	SN75374
	30IC (D)	Reel of 2500	SN75374DR	31175374	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### logic diagram (positive logic)

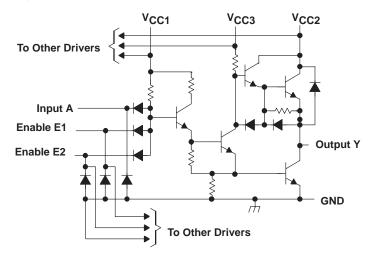




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#### schematic (each driver)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1): V <sub>CC1</sub>	
V <sub>CC2</sub>	–0.5 V to 25 V
	0.5 V to 30 V
Input voltage, V <sub>I</sub>	5.5 V
Peak output current, I <sub>I</sub> (t <sub>w</sub> < 10 ms, duty cycle < 50%)	500 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3):	
	N package 67°C/W
Operating virtual junction temperature, T <sub>J</sub>	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
  - 2. Maximum power dissipation is a function of T<sub>J</sub>(max), θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC1</sub>	Supply voltage	4.75	5	5.25	V
V <sub>CC2</sub>	Supply voltage	4.75	20	24	V
V <sub>CC3</sub>	Supply voltage	V <sub>CC2</sub>	24	28	V
V <sub>CC3</sub> -V <sub>CC2</sub>	Voltage difference between supply voltages	0	4	10	V
VIH	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
loн	High-level output current			-10	mA
lOL	Low-level output current			40	mA
TA	Operating free-air temperature	0		70	°C



# electrical characteristics over recommended ranges of $\rm V_{CC1}, \rm V_{CC2}, \rm V_{CC3},$ and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST	T CONDITIONS	MIN	TYP	MAX	UNIT	
VIK	Input clamp vol	tage	I <sub>I</sub> = -12 mA					-1.5	V
			$V_{CC3} = V_{CC2} + 3 V$ ,	$V_{IL} = 0.8 V$ ,	$I_{OH} = -100  \mu A$	V <sub>CC2</sub> - 0.3	V <sub>CC2</sub> - 0.1		
Vou	High-level output voltage		$V_{CC3} = V_{CC2} + 3 V$	$V_{IL} = 0.8 V,$	$I_{OH} = -10 \text{ mA}$	V <sub>CC2</sub> - 1.3	V <sub>CC2</sub> - 0.9		V
VOH			$V_{CC3} = V_{CC2}$	$V_{IL} = 0.8 V$ ,	$I_{OH} = -50 \mu\text{A}$	V <sub>CC2</sub> - 1	V <sub>CC2</sub> - 0.7		V
			$V_{CC3} = V_{CC2}$	$V_{IL} = 0.8 V$ ,	$I_{OH} = -10 \text{ mA}$	V <sub>CC2</sub> – 2.5	V <sub>CC2</sub> – 1.8		
V <sub>OL</sub>	Low-level outpu	ıt voltane	V <sub>IH</sub> = 2 V,	$I_{OL} = 10 \text{ mA}$			0.15	0.3	V
· OL	2011 10101 04100	voltago	$V_{CC2} = 15 \text{ V to } 28 \text{ V},$	$V_{IH} = 2 V$	$I_{OL} = 40 \text{ mA}$		0.25	0.5	·
٧ <sub>F</sub>	Output clamp-d forward voltage		$V_I = 0$ ,	$I_F = 20 \text{ mA}$				1.5	٧
I <sub>I</sub>	Input current at maximum input		V <sub>I</sub> = 5.5 V					1	mA
	High-level	Any A	V 0.4.V					40	•
lн	input current	Any E	V <sub>I</sub> = 2.4 V					80	μΑ
1	Low-level	Any A	V <sub>I</sub> = 0.4 V				-1	-1.6	mA
IL	input current Any E		current Any E				-2	-3.2	IIIA
ICC1(H)	Supply current to VCC1, all output						4	8	
I <sub>CC2(H)</sub>	Supply current to VCC2, all output		V <sub>CC1</sub> = 5.25 V, All inputs at 0 V,	V <sub>CC2</sub> = 24 V, No load	V <sub>CC3</sub> = 28 V,		-2.2	0.25	mA
ICC3(H)	Supply current to V <sub>CC3</sub> , all output						2.2	3.5	
ICC1(L)	Supply current to VCC1, all output						31	47	
I <sub>CC2(L)</sub>	Supply current to VCC2, all output		V <sub>CC1</sub> = 5.25 V, All inputs at 5 V,	V <sub>CC2</sub> = 24 V, No load	V <sub>CC3</sub> = 28 V,			2	mA
I <sub>CC3(L)</sub>	Supply current to V <sub>CC1</sub> , all output						16	27	
I <sub>CC2(H)</sub>	Supply current from		V <sub>CC1</sub> = 5.25 V,	Vcc2 = 24 V.	V <sub>CC3</sub> = 24 V,			0.25	
ICC3(H)	Supply current	from	All inputs at 0 V,	No load	000 =,				mA
	V <sub>CC3</sub> , all outputs high							0.5	
I <sub>CC2(S)</sub>	Supply current to VCC2, standby		V <sub>CC1</sub> = 0,	V <sub>CC2</sub> = 24 V,	V <sub>CC3</sub> = 24 V,			0.25	m ^
ICC3(S)	Supply current to VCC3, standby		All inputs at 0 V,	No load				0.5	mA

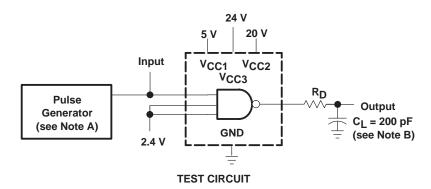
<sup>†</sup> All typical values are at V<sub>CC1</sub> = 5 V, V<sub>CC2</sub> = 20 V, V<sub>CC3</sub> = 24 V, and T<sub>A</sub> = 25°C, except for V<sub>OH</sub> for which V<sub>CC2</sub> and V<sub>CC3</sub> are as stated under test conditions.

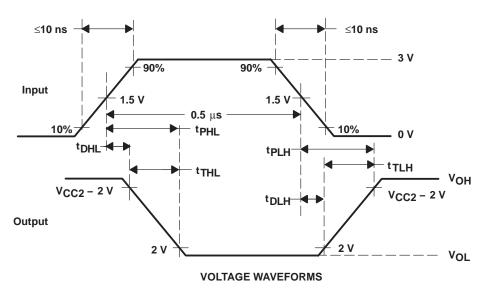
## switching characteristics, $V_{CC1}$ = 5 V, $V_{CC2}$ = 20 V, $V_{CC3}$ = 24 V, $T_A$ = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<sup>t</sup> DLH	Delay time, low- to high-level output			20	30	ns
tDHL	Delay time, high- to low-level output			10	20	ns
<sup>t</sup> PLH	Propagation delay time, low- to high-level output	C <sub>L</sub> = 200 pF,	10	40	60	ns
tPHL	Propagation delay time, high- to low-level output	$R_D = 24 \Omega$ , See Figure 1	10	30	50	ns
tTLH	Transition time, low- to high-level output			20	30	ns
tTHL	Transition time, high- to low-level output			20	30	ns



#### PARAMETER MEASUREMENT INFORMATION





NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz,  $Z_0 \approx 50 \,\Omega$ .

B. C<sub>L</sub> includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

#### **TYPICAL CHARACTERISTICS**

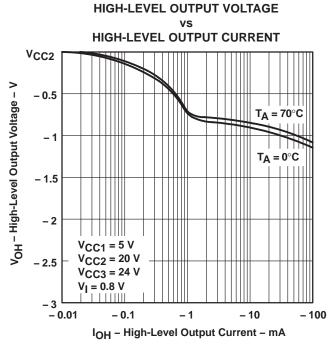


Figure 2

## **LOW-LEVEL OUTPUT VOLTAGE** LOW-LEVEL OUTPUT CURRENT 0.5 V<sub>CC1</sub> = 5 V $V_{CC2} = 20 V$ V<sub>OL</sub> - Low-Level Output Voltage - V $V_{CC3} = 24 V$ 0.4 $V_I = 2 V$ $T_A = 70^{\circ}C$ 0.3 $T_A = 0^{\circ}C$ 0.2 0.1 0 0 40 80 100

IOL - Low-Level Output Current - mA

Figure 4

## HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

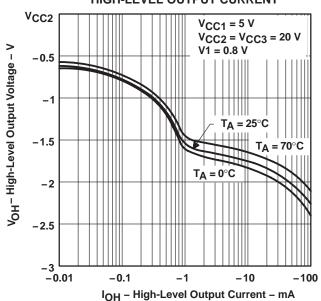


Figure 3

#### **VOLTAGE TRANSFER CHARACTERISTICS**

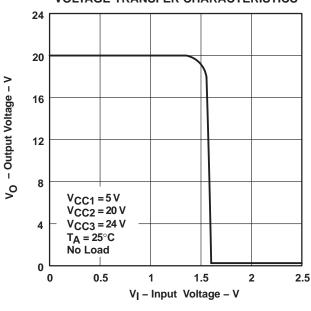


Figure 5

#### TYPICAL CHARACTERISTICS

## PROPAGATION DELAY TIME LOW- TO HIGH-LEVEL OUTPUT

### FREE-AIR TEMPERATURE

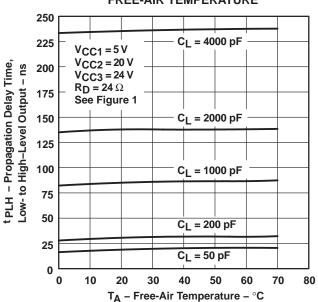


Figure 6

## PROPAGATION DELAY TIME LOW-TO HIGH-LEVEL OUTPUT

## V<sub>CC2</sub> SUPPLY VOLTAGE

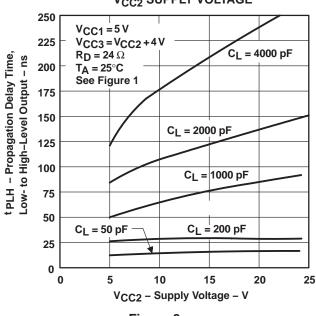


Figure 8

## PROPAGATION DELAY TIME HIGH- TO LOW-LEVEL OUTPUT

### FREE-AIR TEMPERATURE

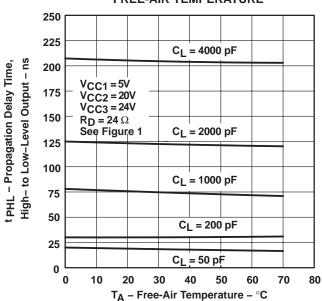


Figure 7

## PROPAGATION DELAY TIME HIGH- TO LOW-LEVEL OUTPUT

## V<sub>CC2</sub> SUPPLY VOLTAGE

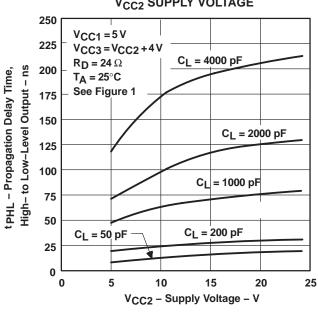
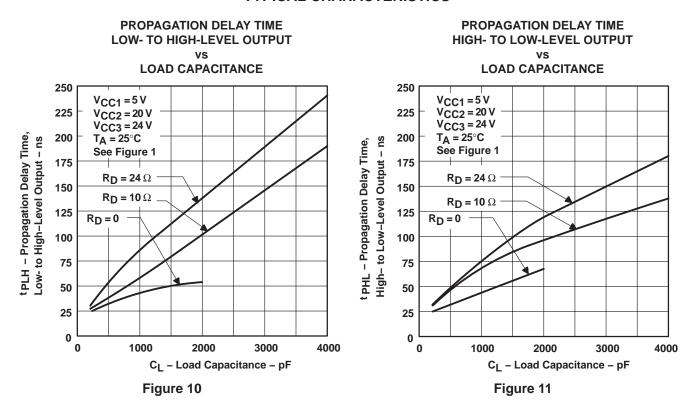


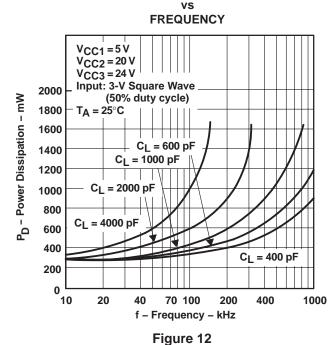
Figure 9



#### TYPICAL CHARACTERISTICS



## POWER DISSIPATION (ALL DRIVERS)



NOTE: For  $R_D = 0$ , operation with  $C_L > 2000$  pF violates absolute maximum current rating.

#### THERMAL INFORMATION

#### power-dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where  $P_{DC(AV)}$  is the steady-state power dissipation with the output high or low,  $P_{C(AV)}$  is the power level during charging or discharging of the load capacitance, and  $P_{S(AV)}$  is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load, and all are averaged over a full cycle.

The power components per driver channel are:

$$\mathsf{P}_{\mathsf{DC}(\mathsf{AV})} = \frac{\left(\mathsf{P}_{\mathsf{H}}\mathsf{t}_{\mathsf{H}} \,+\, \mathsf{P}_{\mathsf{L}}\mathsf{t}_{\mathsf{L}}\right)}{\mathsf{T}}$$

$$P_{C(AV)} \approx CV^{2_c^f}$$

$$\mathsf{P}_{\mathsf{S}(\mathsf{AV})} = \frac{\left(\mathsf{P}_{\mathsf{LH}}\mathsf{t}_{\mathsf{LH}} + \mathsf{P}_{\mathsf{HL}}\mathsf{t}_{\mathsf{HL}}\right)}{\mathsf{T}}$$

where the times are as defined in Figure 15.

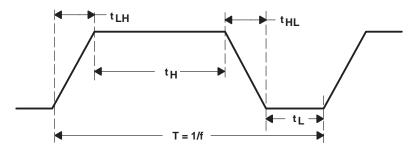


Figure 13. Output-Voltage Waveform

#### THERMAL INFORMATION

#### power-dissipation precautions (continued)

 $P_L$ ,  $P_H$ ,  $P_{LH}$ , and  $P_{HL}$  are the respective instantaneous levels of power dissipation, and C is the load capacitance.  $V_C$  is the voltage across the load capacitance during the charge cycle shown by the equation:

$$V_C = V_{OH} - V_{OL}$$

P<sub>S(AV)</sub> may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz,  $V_{OH} = 19.9$  V and  $V_{OL} = 0.15$  V with  $V_{CC1} = 5$  V,  $V_{CC2} = 20$  V,  $V_{CC3} = 24$  V,  $V_{C} = 19.75$  V, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for  $C_L < 2000$  pF,  $P_{S(AV)}$  is negligible and can be ignored. When the output voltage is low,  $I_{CC2}$  is negligible and can be ignored.

On a per-channel basis using data-sheet values,

$$P_{DC(AV)} = \left[ 5 V \left( \frac{4 \text{ mA}}{4} \right) + 20 V \left( \frac{-2.2 \text{ mA}}{4} \right) + 24 V \left( \frac{2.2 \text{ mA}}{4} \right) \right] 0.6 + \left[ 5 V \left( \frac{31 \text{ mA}}{4} \right) + 20 V \left( \frac{0 \text{ mA}}{4} \right) + 24 V \left( \frac{16 \text{ mA}}{4} \right) \right] 0.4$$

P<sub>DC(AV)</sub> = 58.2 mW per channel

Power during the charging time of the load capacitance is

$$P_{C(AV)} = (1000 \text{ pF})(19.75 \text{ V})^2(0.2 \text{ MHz}) = 78 \text{ mW per channel}$$

Total power for each driver is:

$$P_{T(AV)} = 58.2 \text{ mW} + 78 \text{ mW} = 136.2 \text{ mW}$$

The total package power is:

$$P_{T(AV)} = (136.2)(4) = 544.8 \text{ mW}$$

#### **APPLICATION INFORMATION**

#### driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of an FET consists of a reverse-biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 14a, an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a  $470-\Omega$  pullup resistor. The input capacitance ( $C_{ISS}$ ) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time, due to the product of input capacitance and the pullup resistor, is shown in Figure 14b.

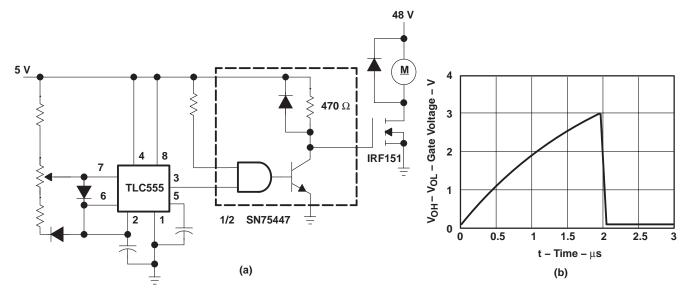


Figure 14. Power MOSFET Drive Using SN75447

A faster, more efficient drive circuit uses an active pullup, as well as an active pulldown output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type (see Figure 15a). The resulting faster switching speeds are shown in Figure 15b.

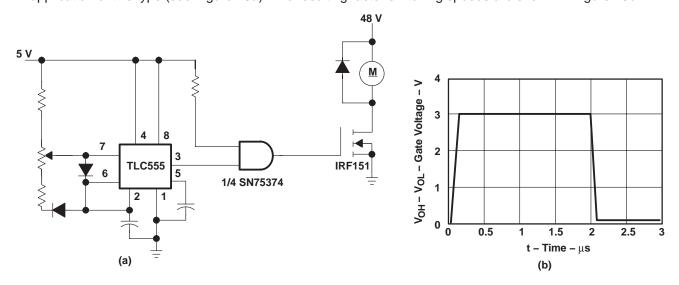


Figure 15. Power MOSFET Drive Using SN75374



#### **APPLICATION INFORMATION**

#### driving power MOSFETs (continued)

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation:

$$I_{PK} = \frac{VC}{t_r}$$

where C is the capacitive load and  $t_r$  is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14a, V is found by the equation:

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14a is:

$$I_{PK} = \frac{(3-0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a  $V_{CC}$  of 5 V and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of  $V_{CC2}$  must be supplied to the MOSFET gate,  $V_{CC3}$  should be at least 3 V higher than  $V_{CC2}$ .

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/			Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN75374D	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374
SN75374D.A	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374
SN75374DE4	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374
SN75374DR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374
SN75374DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374
SN75374DRG4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374
SN75374N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75374N
SN75374N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75374N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE OPTION ADDENDUM**

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	•	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75374DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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#### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	SN75374DR	SOIC	D	16	2500	353.0	353.0	32.0	

## **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75374D	D	SOIC	16	40	507	8	3940	4.32
SN75374D.A	D	SOIC	16	40	507	8	3940	4.32
SN75374DE4	D	SOIC	16	40	507	8	3940	4.32
SN75374N	N	PDIP	16	25	506	13.97	11230	4.32
SN75374N.A	N	PDIP	16	25	506	13.97	11230	4.32

## D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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