







SN74LXC1T45 SCES934A - SEPTEMBER 2021 - REVISED DECEMBER 2021

SN74LXC1T45 Single-Bit Dual-Supply Bus Transceiver With Configurable Level **Shifting**

1 Features

- Fully configurable dual-rail design allows each port to operate from 1.1 V to 5.5 V
- Robust, glitch-free power supply sequencing
- Up to 420-Mbps support for 3.3 V to 5.0 V
- Schmitt-trigger inputs allow for slow or noisy inputs
- I/O's with integrated dynamic pull-down resistors help reduce external component count
- Control inputs with integrated static pull-down resistors allow for floating control inputs
- High drive strength (up to 32 mA at 5 V)
- Low power consumption
 - 3-µA maximum (25°C)
 - 6-μA maximum (–40°C to 125°C)
- V_{CC} isolation and V_{cc} disconnect (I $_{off-float}$) feature
 - If either V_{CC} supply is < 100 mV or disconnected, all I/O's get pulled-down and then become high-impedance
- I_{off} supports partial-power-down mode operation
- Compatible with LVC family level shifters
- Control logic (DIR and \overline{OE}) are referenced to V_{CCA}
- Operating temperature from -40°C to +125°C
- Latch-up performance exceeds 100 mA per JESD 78. class II
- ESD protection exceeds JESD 22
 - 4000-V human-body model
 - 1000-V charged-device model

2 Applications

- Eliminate slow or noisy input signals
- Driving indicator LEDs or buzzers
- Debouncing a mechanical switch
- General purpose I/O level shifting

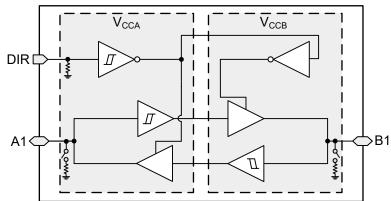
3 Description

SN74LXC1T45 is 1-bit. noninverting bidirectional voltage level translation device. The I/O pin A and control pin (DIR) are referenced to V_{CCA} logic levels, and the I/O pin B are referenced to V_{CCB} logic levels. The A pin is able to accept I/O voltages ranging from 1.1 V to 5.5 V, while the B pin can accept I/O voltages from 1.1 V to 5.5 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A. See Device Functional Modes for a summary of the operation of the control logic.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LXC1T45DRL	SOT (6)	1.60 mm × 1.20 mm
SN74LXC1T45DRY	SON (6)	1.45 mm × 1.00 mm
SN74LXC1T45DBV	SOT-23 (6)	2.90 mm × 1.60 mm
SN74LXC1T45DCK	SC70 (6)	2.00 mm × 1.25 mm
SN74LXC1T45DTQ	X2SON (6)	1.00 mm × 0.80 mm

For all available packages, see the orderable addendum at the end of the data sheet.



SN74LXC1T45 Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2021) to Revision A (December 2021)Page• Changed the status of the data sheet from: Advanced Information to: Production Data1

Product Folder Links: SN74LXC1T45



5 Pin Configuration and Functions

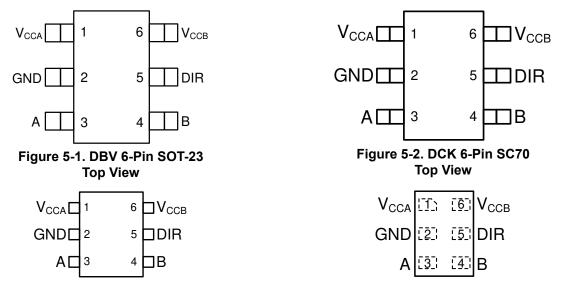


Figure 5-3. DRL Package Preview 6-Pin SOT Top View

Figure 5-4. DRY Package Preview 6-Pin SON Top View

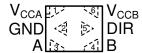


Figure 5-5. DTQ Package Preview 6-Pin X2SON Transparent Top View

Table 5-1. Pin Functions

	PIN		
NAME	DBV, DCK, DRL, DRY, DTQ	TYPE	DESCRIPTION
A	3	I/O	Input or output A. Referenced to V _{CCA} .
В	4	I/O	Input or output B. Referenced to V _{CCB} .
DIR	5	I	Direction-control signal for all ports. Referenced to V _{CCA} .
GND	2	_	Ground.
DIR	5	I	Direction-control signal for all ports. Referenced to V _{CCA} .
V _{CCA}	1	_	A-port supply voltage. 1.1 V \leq V _{CCA} \leq 5.5 V.
V _{CCB}	6	_	B-port supply voltage. 1.1 V \leq V _{CCB} \leq 5.5 V.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CCA}	Supply voltage A		-0.5	6.5	V
V _{CCB}	Supply voltage B		-0.5	6.5	V
		I/O Ports (A Port)	-0.5	6.5	
VI	Input Voltage ⁽²⁾	I/O Ports (B Port)	-0.5	6.5	V
		Control Inputs	-0.5	6.5	
.,	Voltage applied to any output in the high-impedance or power-off	A Port	-0.5	6.5	.,
Vo	state ⁽²⁾	B Port	-0.5	6.5	V
.,	Value as a sufficient to a superior to the birth and accordance (2) (3)	A Port	-0.5	V _{CCA} + 0.5	V
Vo	Voltage applied to any output in the high or low state ^{(2) (3)}	B Port		V _{CCB} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50		mA
I _{OK}	Output clamp current	V _O < 0	-50		mA
Io	Continuous output current	,	-50	50	mA
	Continuous current through V _{CC} or GND		-200	200	mA
Tj	Junction Temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, this device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Electrostatic discharge	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

				MIN	MAX	UNIT
V _{CCA}	Supply voltage A			1.1	5.5	V
V _{CCB}	Supply voltage B			1.1	5.5	V
			V _{CCO} = 1.1 V		-0.1	
			V _{CCO} = 1.4 V		-4	
ı	High lovel output of	urront	V _{CCO} = 1.65 V		-8	mA
I _{OH}	High-level output o	urrent	V _{CCO} = 2.3 V		-12	IIIA
			V _{CCO} = 3 V		-24	
			V _{CCO} = 4.5 V		-32	
			V _{CCO} = 1.1 V		0.1	
			V _{CCO} = 1.4 V		4	
	Law lavel autaut a	irrant	V _{CCO} = 1.65 V		8	A
l _{OL}	Low-level output co	urrent	V _{CCO} = 2.3 V		12	mA
			V _{CCO} = 3 V		24	
			V _{CCO} = 4.5 V		32	
VI	Input voltage (3)		·	0	5.5	V
\/	Output valtage	Active State		0	V _{CCO}	V
Vo	Output voltage	Tri-State	0	5.5	V	
T _A	Operating free-air	temperature		-40	125	°C

⁽¹⁾ V_{CCI} is the V_{CC} associated with the input port.

6.4 Thermal Information

				SN74LXC1T45			
	THERMAL METRIC(1)	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTQ (X2SON)	UNIT
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	217.4	216.1	TBD	TBD	TBD	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance	136.0	143.6	TBD	TBD	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	98.5	75.9	TBD	TBD	TBD	°C/W
Y _{JT}	Junction-to-top characterization parameter	75.8	58.5	TBD	TBD	TBD	°C/W
Y _{JB}	Junction-to-board characterization parameter	98.2	75.6	TBD	TBD	TBD	°C/W
R _θ JC(bottom)	Junction-to-case (bottom) thermal resistance	N/A	N/A	TBD	TBD	TBD	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ V_{CCO} is the V_{CC} associated with the output port.

⁽³⁾ All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under the Electrical Characteristics.



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

		air temperature rang					peratir	ng free	air temperat	ure (T	7)		
PA	RAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}		25°C		-40°	C to 85°C	-40°	C to 12	5°C	UNI
					MIN	TYP	MAX	MIN	TYP MAX	MIN	TYP	MAX	
			1.1 V	1.1 V				0.44	0.88	0.44		0.88	
			1.4 V	1.4 V				0.60	0.98	0.60		0.98	
		Data Inputs	1.65 V	1.65 V				0.76	1.13	0.76		1.13	
		(Ax Bx)	2.3 V	2.3 V				1.08	1.56	1.08		1.56	V
		(Referenced to V _{CCI})	3 V	3 V				1.48	1.92	1.48		1.92	
	Positive-		4.5 V	4.5 V				2.19	2.74	2.19		2.74	
,	going input-		5.5 V	5.5 V				2.65	3.33	2.65		3.33	
/ _{T+}	threshold		1.1 V	1.1 V				0.44	0.88	0.44		0.88	
	voltage		1.4 V	1.4 V				0.60	0.98	0.60		0.98	
		Control Input	1.65 V	1.65 V				0.76	1.13	0.76		1.13	
		(DIR) (Referenced to	2.3 V	2.3 V				1.08	1.56	1.08		1.56	V
		V _{CCA})	3 V	3 V				1.48	1.92	1.48		1.92	
			4.5 V	4.5 V				2.19	2.74	2.19		2.74	
			5.5 V	5.5 V				2.65	3.33	2.65		3.33	
			1.1 V	1.1 V				0.17	0.48	0.17		0.48	
			1.4 V	1.4 V				0.28	0.59	0.28		0.59	
		Data Inputs	1.65 V	1.65 V				0.35	0.69	0.35		0.69	
		(Ax, Bx)	2.3 V	2.3 V				0.56	0.97	0.56		0.97	٧
			3 V	3 V				0.89	1.5	0.89		1.5	
	Negative- going input- threshold		4.5 V	4.5 V				1.51	1.97	1.51		1.97	
,			5.5 V	5.5 V				1.88	2.4	1.88		2.4	
T-			1.1 V	1.1 V				0.17	0.48	0.17	,	0.48	
	voltage		1.4 V	1.4 V				0.28	0.6	0.28		0.6	
		Control Input	1.65 V	1.65 V				0.35	0.71	0.35		0.71	V
		(DIR) (Referenced to	2.3 V	2.3 V				0.56	1	0.56		1	
		V _{CCA})	3 V	3 V				0.89	1.5	0.89		1.5	
			4.5 V	4.5 V				1.51	2	1.51	,	2	
			5.5 V	5.5 V				1.88	2.46	1.88		2.46	
			1.1 V	1.1 V				0.2	0.4	0.2		0.4	
			1.4 V	1.4 V				0.25	0.5	0.25		0.5	
		Data Inputs	1.65 V	1.65 V				0.3	0.55	0.3		0.55	
		(Av By)	2.3 V	2.3 V				0.38	0.65	0.38		0.65	V
		(Referenced to V _{CCI})	3 V	3 V				0.46	0.72	0.46		0.72	
	Input-		4.5 V	4.5 V				0.58	0.93	0.58		0.93	
V _T	threshold		5.5 V	5.5 V				0.69	1.06	0.69		1.06	
νT	hysteresis		1.1 V	1.1 V				0.2	0.4	0.2		0.4	
	$(V_{T+}-V_{T-})$		1.4 V	1.4 V				0.25	0.5	0.25		0.5	
		Control Input	1.65 V	1.65 V				0.3	0.55	0.3		0.55	
		(DIR) (Referenced to	2.3 V	2.3 V				0.38	0.65	0.38		0.65	5 V
		V _{CCA})	3 V	3 V				0.46	0.72	0.46		0.72	
			4.5 V	4.5 V				0.58	0.93	0.58		0.93	
			5.5 V	5.5 V				0.69	1.06	0.69		1.06	



6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2)

						0	peratii	ng free	-air ter	npera	ture (T)		
PA	RAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}		25°C		–40°	'C to 8	5°C	-40°0	C to 12	25°C	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
		I _{OH} = -100 μA	1.1V – 5.5V	1.1V – 5.5V				V _{CCO} - 0.1			V _{CCO} - 0.1			
	High-level	I _{OH} = -4 mA	1.4 V	1.4 V				1			1			
V_{OH}	output	$I_{OH} = -8 \text{ mA}$	1.65 V	1.65 V				1.2			1.2			V
	voltage (3)	I _{OH} = -12 mA	2.3 V	2.3 V				1.9			1.9			
		I _{OH} = -24 mA	3 V	3 V				2.4			2.4			
		$I_{OH} = -32 \text{ mA}$	4.5 V	4.5 V				3.8			3.8			
		I _{OL} = 100 μA	1.1V - 5.5V	1.1V - 5.5V						0.1			0.1	
		I _{OL} = 4 mA	1.4 V	1.4 V						0.3			0.3	
.,	Low-level	I _{OL} = 8 mA	1.65 V	1.65 V						0.45			0.45	V
V_{OL}	output voltage ⁽⁴⁾	I _{OL} = 12 mA	2.3 V	2.3 V						0.3			0.3	V
		I _{OL} = 24 mA	3 V	3 V						0.55			0.55	
		I _{OL} = 32 mA	4.5 V	4.5 V						0.55			0.55	
	Input leakage	Control input (DIR) V _I = V _{CCA} or GND	1.1V – 5.5V	1.1V – 5.5V	-0.1		1	-0.1		2	-0.1		2	μA
I _I	current	Data Inputs ⁽⁵⁾ (Ax, Bx) V _I = V _{CCI} or GND	1.1V – 5.5V	1.1V – 5.5V	-0.3		1	-1		1	-2		2	μA
_	Partial power	A Port or B Port	0 V	0 V - 5.5 V	-1		1	-2		2	-2.5		2.5	
l _{off}	down current	V _I or V _O = 0 V - 5.5 V	0 V - 5.5 V	0 V	-1		1	-2		2	-2.5		2.5	μA
	Floating		Floating (6)	0 V - 5.5 V	-1.5		1.5	-2		2	-2.5		2.5	
I _{off-float}	supply Partial power down current	A Port or B Port V_1 or V_0 = GND	0 V - 5.5 V	Floating (6)	-1.5		1.5	-2		2	-2.5		2.5	μA
			1.1V – 5.5V	1.1V - 5.5V			2			2			4	
	\/ aunnh	$V_I = V_{CCI}$ or GND $I_O = 0$	0 V	5.5 V	-0.2			-0.5			-1			
I_{CCA}	V _{CCA} supply current	10 0	5.5 V	0 V			1			1			2	μΑ
		V _I = GND I _O = 0	5.5 V	Floating (6)			1			1			2	
			1.1V – 5.5V	1.1V - 5.5V			2			2			4	
	.,	$V_I = V_{CCI}$ or GND $I_O = 0$	0 V	5.5 V			1			1			2	
I_{CCB}	V _{CCB} supply current	10 - 0	5.5 V	0 V	-0.2			-0.5			-1			μΑ
		$V_I = GND$ $I_O = 0$	Floating ⁽⁶⁾	5.5 V			1			1			2	
I _{CCA} + I _{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.1V – 5.5V	1.1V – 5.5V			3			4			6	μA
ΔI _{CCA}	V _{CCA} additional supply	Control input (DIR): $V_1 = V_{CCA} - 0.6 \text{ V}$ A port = VCCA or GND B Port = open	3.0V - 5.5V	3.0V - 5.5V						50			75	μA
(current per input	A Port: V _I = V _{CCA} – 0.6 V DIR = V _{CCA} , B Port = open	3.0V - 5.5V	3.0V - 5.5V						50			75	-

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2)

						0	peratir	ng free	-air te	mperat	ure (T	()		
PA	RAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}		25°C		–40°	-40°C to 85°C		to 85°C -40°C to 125°C		25°C	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ΔI _{CCB}	V _{CCB} additional supply current per input	B Port: V _I = V _{CCB} - 0.6 V DIR = GND, A Port = open	3.0V - 5.5V	3.0V - 5.5V						50			75	μА
C _i	Control Input Capacitance	V _I = 3.3 V or GND	3.3 V	3.3 V		2.2				5			5	pF
C _{io}	Data I/O Capacitance	V_{CCO} = 0V V_{O} = 1.65V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V		4.3				10.5			10.5	pF

- (1) V_{CCI} is the V_{CC} associated with the input port (2) V_{CCO} is the V_{CC} associated with the output port (3) Tested at $V_I = V_{T+(MAX)}$

- (4) Tested at V_I = V_{I-(MIN)}
 (5) For I/O ports, the parameter I_I includes the I_{OZ} current
 (6) Floating is defined as a node that is both not actively driven by an external device and has leakage not exceeding 10nA

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6.6 Switching Characteristics, $V_{CCA} = 1.2 \pm 0.1 \text{ V}$

									B-Port	Supply	Voltage (V _{CC}	:в)																
	PARAMETER	FROM	то	Test Conditions	1.2 ± 0.1	٧	1.5 ± 0.1	I V	1.8 ± 0.1	5 V	2.5 ± 0.2	2 V	3.3 ± 0.	3 V	5.0 ± 0	.5 V	UNIT											
					MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX												
		Α	В	-40°C to 85°C	6	85	4	41	3	36	1	33	1	34	1	44												
	Propagation	^		-40°C to 125°C	8	55	6	37	5	33	3	30	3	30	2	33	ns											
t _{pd}	delay	В	Α	-40°C to 85°C	6	85	5	71	4	67	3	60	3	57	3	58	1115											
	В	В	^	-40°C to 125°C	8	55	6	47	6	43	5	38	4	37	4	36												
	DIR	DIB	۸	-40°C to 85°C	5	53	5	53	5	53	5	53	5	53	4	53												
	Disable time	DIK	Α	-40°C to 125°C	7	47	7	47	7	47	7	47	7	47	7	47												
t _{dis}	Disable time	DIR	В	-40°C to 85°C	10	85	7	47	6	41	5	34	5	33	4	32	ns											
			DIR	DIR	DIR	DIR	DIR		-40°C to 125°C	14	71	11	48	10	41	8	34	8	33	6	32							
		DID.	DID	DID	515	DIR	DIP	DID	DID	DIP	DIP	DIP A	DIR A	Α	-40°C to 85°C	21	150	17	110	16	99	13	86	13	83	12	85	
	Enable time	DIK	A	-40°C to 125°C	27	121	23	89	21	80	17	68	17	65	15	63]											
t _{en}	Enable time DIF	חום ו	DIB I	DIB I	DIP	DIB	DIB	DIB			В	-40°C to 85°C	16	118	14	89	13	84	12	81	11	82	11	92	ns			
		אוט	B	-40°C to 125°C	19	97	18	79	17	73	16	68	15	67	14	70												



6.7 Switching Characteristics, $V_{CCA} = 1.5 \pm 0.1 \text{ V}$

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

									B-Port S	Supply	Voltage (V _{CC}	в)													
	PARAMETER	FROM	то	Test Conditions	1.2 ± 0.1	٧	1.5 ± 0.1	٧	1.8 ± 0.1	5 V	2.5 ± 0.2	V	3.3 ± 0.3	S V	5.0 ±	0.5 V	UNIT								
					MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TY	P MAX									
		Α	В	-40°C to 85°C	5	71	3	29	1	24	1	20	1	19	1	19									
	Propagation	^		-40°C to 125°C	6	47	4	30	3	25	2	21	2	20	1	20	ns								
t _{pd}	delay B	D	Α	-40°C to 85°C	4	41	3	29	2	27	1	23	1	22	1	21	115								
				-40°C to 125°C	6	37	4	30	4	27	3	24	3	22	2	22									
	DIR	DIB	Α	-40°C to 85°C	2	26	2	26	2	26	2	26	2	26	2	26									
	Disable time	DIK	A	-40°C to 125°C	4	27	4	27	4	27	4	27	4	27	4	27	ns								
t _{dis}	Disable time	DID	В	-40°C to 85°C	8	71	6	38	5	32	3	25	3	24	2	22	115								
		DIR	DIR	DIR	DIR	DIR	DIR	DIK	DIK		-40°C to 125°C	12	61	10	39	9	34	6	26	6	25	4	23		
		DID	DID	DID	DID	DID	DIR	DIR	DIP	DID	Α	-40°C to 85°C	17	106	13	63	12	54	9	44	9	41	8	39	
	Enable time	DIK	A	-40°C to 125°C	23	92	19	64	17	56	14	45	14	42	12	40									
t _{en}	Lilable tille	DIR E	DIB I	DIB I	DIB I	DIR	B	-40°C to 85°C	12	90	10	51	9	45	8	40	7	39	7	39	ns				
			В	-40°C to 125°C	16	69	14	51	13	47	12	42	11	40	10	40									

Product Folder Links: SN74LXC1T45

6.8 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15 \text{ V}$

									B-Port	Supply	Voltage (V _{CC}	:в)										
	PARAMETER	FROM	то	Test Conditions	1.2 ± 0.1	٧	1.5 ± 0.1	V	1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		5.0 ± 0.5 V		UNIT					
					MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TY	P MAX						
		_	В	-40°C to 85°C	4	67	2	27	1	22	1	18	1	16	1	16						
	Propagation	A		-40°C to 125°C	6	43	4	27	3	22	2	18	1	17	1	16	ns					
t _{pd}	delay	В	Α	-40°C to 85°C	3	36	1	24	1	22	1	19	1	18	1	17	1115					
		В	^	-40°C to 125°C	5	33	3	25	3	22	2	19	2	18	1	18						
	DIR Disable time	DIB	Α	-40°C to 85°C	2	21	2	21	2	21	2	21	2	21	1	21						
			-40°C to 125°C	3	22	3	22	3	22	3	22	3	22	3	22	ns						
t _{dis}	Disable time	DIR	В	-40°C to 85°C	7	65	5	35	4	29	2	22	2	21	1	19	1 115					
		DIK		-40°C to 125°C	10	56	8	36	7	30	6	24	5	22	3	20						
			DIB	DIR	DIR	DIR	DIR	^	-40°C to 85°C	15	96	11	54	10	46	8	36	7	34	6	31	
	Enable time		DIR A	DIR A	R A	-40°C to 125°C	20	82	17	56	15	48	13	38	12	35	10	33]			
t _{en}	Enable time	DIR E	Р	-40°C to 85°C	11	80	9	42	7	37	7	33	6	31	6	30	ns					
	D		P	-40°C to 125°C	14	60	12	43	11	39	10	34	9	33	9	32						



6.9 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2 \text{ V}$

									B-Po	rt Supply	Voltage (V _C	:в)					
	PARAMETER	FROM	то	Test Conditions	1.2 ± 0	.1 V	1.5 ± 0.1	٧	1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		5.0 ± 0.5 V		UNIT
					MIN TYP	MAX	MIN TYP	MAX	MIN TY	P MAX	MIN TYP	MAX	MIN T	TYP MAX	MIN	TYP MAX	
		Α	В	-40°C to 85°C	3	60	1	23	1	19	1	15	1	14	1	13	
	Propagation	٥	-40°C to 125°C	5	38	3	24	2	19	1	15	1	14	1	13	ns	
t _{pd}	delay	elay	Α	-40°C to 85°C	1	33	1	20	1	18	1	15	1	14	1	14	
		B		-40°C to 125°C	3	30	2	21	2	18	1	15	1	14	1	14	
	DIB	DIR	А	-40°C to 85°C	1	15	1	15	1	15	1	15	1	15	1	15	
	Disable time	DIIX	^	-40°C to 125°C	1	15	1	15	1	15	1	15	1	15	1	15	ns
t _{dis}	Disable time	DIR	В	-40°C to 85°C	5	54	4	30	3	25	2	19	2	18	1	16	
		DIK		-40°C to 125°C	8	47	7	31	6	26	5	21	4	19	2	17	
		DIR	Α	-40°C to 85°C	12	82	9	44	8	37	6	29	6	27	5	24	
		DIK	^	-40°C to 125°C	17	68	14	45	13	39	11	31	10	29	8	26	
t _{en}	Enable time	DIR		-40°C to 85°C	8	67	6	33	5	29	4	25	4	23	4	22	ns
	l	DIK	D	-40°C to 125°C	11	49	9	34	8	30	7	26	7	24	6	23	

6.10 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3 \text{ V}$

									B-Port	Supply	Voltage (V _{CC}	:в)											
	PARAMETER	FROM	то	Test Conditions	1.2 ± 0.1	٧	1.5 ± 0.1	V	1.8 ± 0.15 V		2.5 ± 0.2	2 V	3.3 ± 0.3 V		5.0 ± 0.5 V		UNIT						
					MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TY	P MAX	MIN T	YP MAX							
		Α	В	-40°C to 85°C	3	57	1	22	1	18	1	14	1	13	1	12							
	Propagation	A	В	-40°C to 125°C	4	37	3	22	2	18	1	14	1	13	1	12	ns						
t _{pd}	delay	В	Α	-40°C to 85°C	1	34	1	19	1	16	1	13	1	13	1	12							
		В	A	-40°C to 125°C	3	30	2	20	1	17	1	14	1	13	1	12							
	DIR	DIB	Α	-40°C to 85°C	1	14	1	14	1	14	1	14	1	14	1	14							
	Disable time	DIK		-40°C to 125°C	1	14	1	14	1	14	1	14	1	14	1	14	ns						
t _{dis}	Disable time	DIR	В	-40°C to 85°C	5	49	3	27	3	23	1	18	2	17	1	15							
		DIK	В	-40°C to 125°C	8	44	6	28	5	24	4	19	4	18	2	16							
			DIR /	DIR	DIR	DIR	DIR	DIR	^	-40°C to 85°C	12	78	8	39	7	33	6	26	5	25	4	22	
				OIR A	Α	-40°C to 125°C	16	64	13	40	11	35	9	28	9	26	7	23					
t _{en}	Enable time	DIR	IR B	-40°C to 85°C	8	64	6	30	5	26	4	23	4	21	4	20	ns						
	D	אוט	В	-40°C to 125°C	11	46	9	31	8	27	7	24	6	22	6	21							



6.11 Switching Characteristics, $V_{CCA} = 5.0 \pm 0.5 \text{ V}$

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

						<u> </u>			B-Poi	rt Supply	Voltage (V _{CC}	:в)						
	PARAMETER	FROM	то	Test Conditions	1.2 ± 0	.1 V	1.5 ± 0.1	V	1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		5.0 ± 0.5 V			UNIT
					MIN TYP	MAX	MIN TYP	MAX	MIN TY	P MAX	MIN TYP	MAX	MIN	TYP MAX	MIN	TYP N	IAX	
		Α	В	-40°C to 85°C	3	58	1	21	1	17	1	14	1	12	1		11	
	Propagation delay			-40°C to 125°C	4	36	2	22	1	18	1	14	1	13	1		11	ns
t _{pd}		delay	Α	-40°C to 85°C	1	44	1	19	1	16	1	13	1	12	1		11	115
		B		-40°C to 125°C	2	33	1	20	1	16	1	13	1	12	1		11	
	DIE	DIR	А	-40°C to 85°C	1	12	1	12	1	12	1	12	1	12	1		12	
	Disable time	DIK	A	-40°C to 125°C	1	12	1	12	1	12	1	12	1	12	1		12	ns
t _{dis}	Disable time	DIR	В	-40°C to 85°C	5	48	3	26	3	21	1	16	2	16	1		14	115
		DIIX		-40°C to 125°C	8	43	6	26	5	22	3	17	3	17	2		15	
		DIR	Α	-40°C to 85°C	11	87	8	38	7	31	5	24	5	22	4		20	
		DIK	A	-40°C to 125°C	15	66	12	39	10	32	8	25	8	24	6		21	no
t _{en}	Enable time	DIR		-40°C to 85°C	7	63	5	28	4	24	3	20	3	19	2		18	ns
		DIK	D	-40°C to 125°C	9	43	7	28	6	25	5	21	4	19	4		18	

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6.12 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

						ting fre erature		UNIT	
PARAMETER	TEST CONDI	TIONS	V _{CCI}	V _{cco}	-40°C to 125°C		UNIT		
					MIN	TYP	MAX		
			3.0 V - 3.6 V	4.5 V - 5.5 V	200	420			
			2.25 V - 2.75 V	4.5 V - 5.5 V	150	300			
		Up Translation	1.65 V - 1.95 V	4.5 V - 5.5 V	100	200			
		Up Translation	1.1 V - 1.3 V	4.5 V - 5.5 V	20	40			
			1.65 V - 1.95 V	3.0 V - 3.6 V	100	210			
	50% Duty Cycle Input		20						
T _{MAX} - Maximum	One channel switching		1.1 V - 1.3 V	1.65 V - 1.95 V	5	10		Mbps	
Data Rate	20% of pulse > 0.7*V _{CCO}		4.5 V - 5.5 V	3.0 V - 3.6 V	100	210		Minhe	
	20% of pulse < 0.3*V _{CCO}		4.5 V - 5.5 V	2.25 V - 2.75 V	75	140			
			4.5 V - 5.5 V	1.65 V - 1.95 V	50	75			
		Down Translation	4.5 V - 5.5 V	1.1 V - 1.3 V	15	30			
			3.0 V - 3.6 V	1.65 V - 1.95 V	40	75			
			3.0 V - 3.6 V	1.1 V - 1.3 V	10	20			
			1.65 V - 1.95 V	1.1 V - 1.3 V	5	10			

6.13 Operating Characteristics

 $T_{\Lambda} = 25^{\circ}C^{(1)}$

			Supply Voltage (V _{CCB} = V _{CCA})							
	PARAMETER	Test Conditions	1.2 ± 0.1V	$2 \pm 0.1 \text{V}$ $1.5 \pm 0.1 \text{V}$ $1.8 \pm 0.15 \text{V}$ $2.5 \pm 0.2 \text{V}$ $3.3 \pm 0.3 \text{V}$		3.3 ± 0.3V	5.0 ± 0.5V	UNIT		
			TYP	TYP	TYP	TYP	TYP	TYP		
	A to B	A Port	3.2	3.4	3.5	3.7	3.9	5.1		
C _{pdA} (2)	B to A	CL = 0, $RL = Openf = 10$ MHz $t_{rise} = t_{fall} = 1$ ns	19.4	19.6	19.8	20.4	21.8	25.7	pF	
	A to B	B Port	19.3	19.5	19.7	20.4	21.6	25.3		
C _{pdB} (2)	B to A	CL = 0, $RL = Openf = 10$ MHz $t_{rise} = t_{fall} = 1$ ns	3.3	3.5	3.6	4.0	4.4	5.0	pF	

For more information about power dissipation capacitance, see the CMOS Power Consumption and C_{pd} Calculation application report C_{pdB} and C_{pdB} are repectively A-Port and B-Port power dissipation capacitances per transceiver



6.14 Typical Characteristics

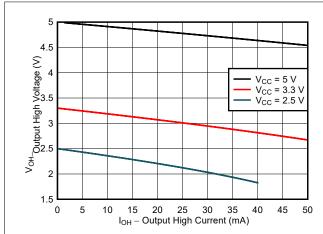


Figure 6-1. Typical (T_A =25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

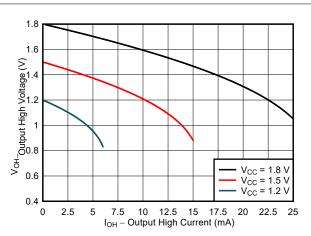


Figure 6-2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

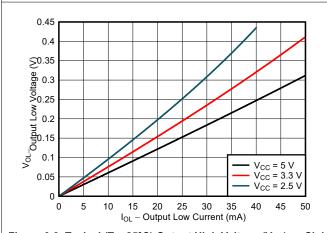


Figure 6-3. Typical (T_A =25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

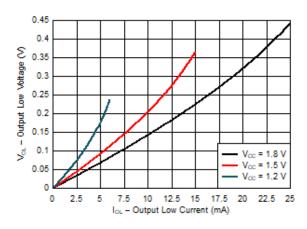


Figure 6-4. Typical (T_A =25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

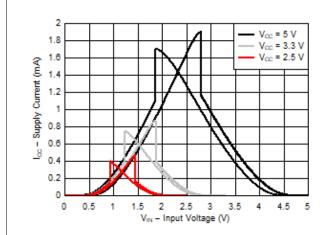


Figure 6-5. Typical (T_A=25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

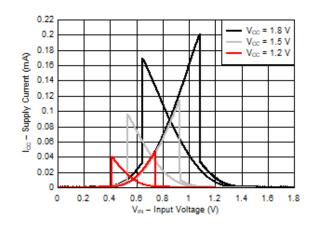


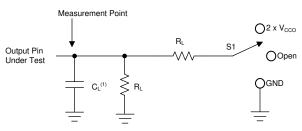
Figure 6-6. Typical (T_A =25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- Δt/ΔV ≤ 1 ns/V

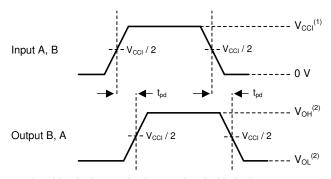


A. C_L includes probe and jig capacitance.

Figure 7-1. Load Circuit

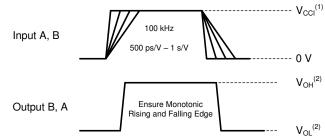
Table 7-1. Load Circuit Conditions

	Parameter	V _{cco}	R_L	C _L	S ₁	V _{TP}
t _{pd}	Propagation (delay) time	1.1 V – 5.5 V	2 kΩ	15 pF	Open	N/A
		1.1 V – 1.6 V	2 kΩ	15 pF	2 × V _{CCO}	0.1 V
t _{en} , t _{dis}	Enable time, disable time	1.65 V – 2.7 V	2 kΩ	15 pF	2 × V _{CCO}	0.15 V
		3.0 V – 5.5 V	2 kΩ	15 pF	2 × V _{CCO}	0.3 V
		1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
t _{en} , t _{dis}	Enable time, disable time	1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
		3.0 V – 5.5 V	2 kΩ	15 pF	GND	0.3 V



- V_{CCI} is the supply pin associated with the input port.
- 2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

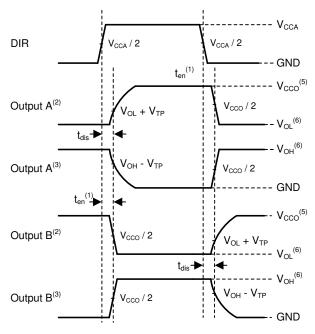
Figure 7-2. Propagation Delay



- 1. V_{CCI} is the supply pin associated with the input port.
- 2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

Figure 7-3. Input Transition Rise and Fall Rate





- A. 1. Illustrative purposes only. Enable time is a calculation as described in *Enable Times*.
 - 2. Output waveform on the condition that input is driven to a valid Logic low.
 - 3. Output waveform on the condition that input is driven to a valid Logic high.
 - 4. V_{CCI} is the supply pin associated with the input port.
 - V_{CCO} is the supply pin associated with the output port.
 - 6. V_{OH} and V_{OL} are typical output voltage levels with specified R_L , C_L , and S_1 .

Figure 7-4. Enable Time And Disable Time

8 Detailed Description

8.1 Overview

The SN74LXC1T45 is an 1-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 1.1 V and as high as 5.5 V. Additionally, the device can be operated with $V_{CCA} = V_{CCB}$. The A port is designed to track V_{CCA} , and the B port is designed to track V_{CCB} .

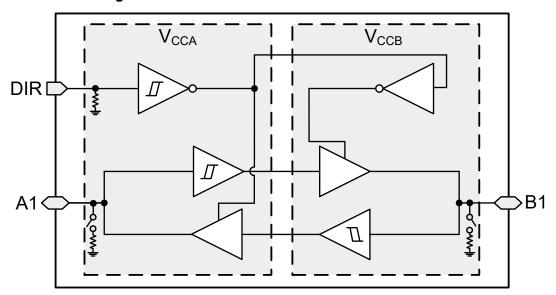
The SN74LXC1T45 device is designed for asynchronous communication between devices and transmits data from A to B or from B to A based on the logic level of the direction-control input (DIR). The control pins of the SN74LXC1T45 (DIR) is referenced to V_{CCA} . The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess ICC and ICCZ.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or sourced into an input, output, or I/O while the device is powered down.

The V_{CC} isolation or V_{CC} disconnect feature ensures that if either V_{CC} is less than 100 mV or disconnected with the complementary supply within the recommended operating conditions, then both I/O ports are weakly pulled-down and then set to the high-impedance state by disabling their outputs while the supply current is maintained. The $I_{off-float}$ circuitry ensures that no excessive current is drawn from or sourced into an input, output, or I/O while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law $(R = V \div I)$.

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, see *Understanding Schmitt Triggers*.

8.3.1.1 I/O's with Integrated Dynamic Pull-Down Resistors

Input circuits of the data I/O's are always active even when the device is disabled. It is recommended to keep a valid voltage level at the I/O's to avoid high current consumption. To help avoid floating inputs on the I/O's during disabling, this device has $100\text{-k}\Omega$ typical integrated weak dynamic pull-downs on all data I/O's. When the device is disabled, the dynamic pull-downs are activated for only a short period of time to help drive and keep low any floating inputs before the device I/O's become high impedance. If the I/O lines are to be floated after the device is disabled, then it is recommended to keep them at a valid input voltage level using the external pull-downs. This feature is ideal for loads of 30 pF or less. If greater capactive loading is present, then external pull-downs are recommended. If an external pull-up is required, then it should be no larger than 15 k Ω to avoid contention with the 100 k Ω internal pull-down.

8.3.1.2 Control Inputs with Integrated Static Pull-Down Resistors

Similar to the data I/O's, a floating control input can cause high current consumption. To help avoid this concern, this device has integrated weak static pull-downs of $5\text{-}M\Omega$ typical on the control input (DIR). These pull-downs are always present. So for example if the DIR pin is left floating, then the B port will be configured as an input and the A port configured as an output.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.4 V_{CC} Isolation and V_{CC} Disconnect (I_{off-float})

This device has I/O's with Integrated Dynamic Pull-Down Resistors. The I/O's will get pulled down and then enter a high-impedance state when either supply is < 100 mV or left floating (disconnected), while the other supply is still connected to the device. It is recommended that the I/O's for this device are not driven and kept at a logic low state prior to floating (disconnecting) either supply.

The maximum supply current is specified by I_{CCx} , while V_{CCx} is floating, in the *Electrical Characteristics*. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off(float)}$ in the *Electrical Characteristics*.

Product Folder Links: SN74LXC1T45



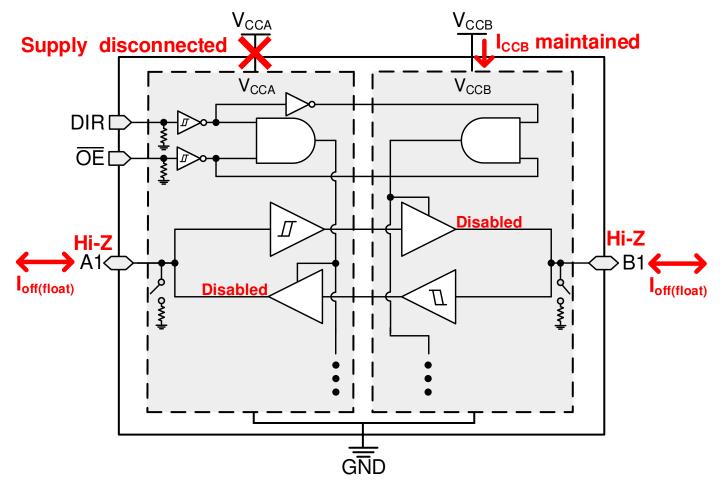


Figure 8-1. V_{CC} Disconnect Feature

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.3.6 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.



8.3.7 Negative Clamping Diodes

Figure 8-2 shows the inputs and outputs to this device that have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative voltage and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

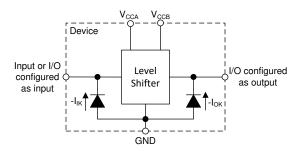


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.8 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.1 V to 5.5 V, making the device suitable for translating between any of the voltage nodes (1.2 V, 1.5 V, 1.8 V, 3.3 V, and 5.0 V).

8.3.9 Supports High-Speed Translation

The SN74LXC1T45 device can support high data rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5.0 V.

8.4 Device Functional Modes

Table 8-1. Function Table

CONTROL INPUTS (1)	PORT	STATUS	OPERATION
DIR	A PORT	B PORT	OPERATION
L	Output (Enabled)	Input (Hi-Z)	B data to A bus
Н	Input (Hi-Z)	Output (Enabled)	A data to B bus

(1) Input circuits of the data I/Os are always active and should be kept at a valid logic level.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LXC1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74LXC1T45 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 420 Mbps when the device translates a signal from 3.3 V to 5.0 V.

9.2 Enable Times

Calculate the enable times for the SN74LXC1T45 using the following formulas:

$$t_{A \text{ en}}$$
 (DIR to A) = t_{dis} (DIR to B) + t_{pd} (B to A) (1)

$$t_{B \text{ en}} \text{ (DIR to B)} = t_{dis} \text{ (DIR to A)} + t_{pd} \text{ (A to B)}$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74LXC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled (t_{dis}) before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay (t_{pd}) . To avoid bus contention, care should be taken to not apply an input signal prior to the output being disabled (t_{dis}) maximum.

9.3 Typical Application

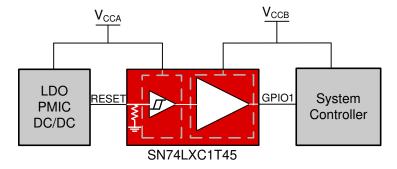


Figure 9-1. LED Driver Application

9.3.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.1 V to 5.5 V
Output voltage range	1.1 V to 5.5 V

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9.3.2 Detailed Design Procedure

To begin the design process, determine the following:

- · Input voltage range
 - Use the supply voltage of the device that is driving the SN74LXC1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{t+}) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{t-}) of the input port.
- · Output voltage range
 - Use the supply voltage of the device that the SN74LXC1T45 device is driving to determine the output voltage range.

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices, as described in *Glitch-free Power Supply Sequencing*.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 μF capacitor is recommended, but transient performance can be improved by having both 1 μF and 0.1 μF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

11.2 Layout Example

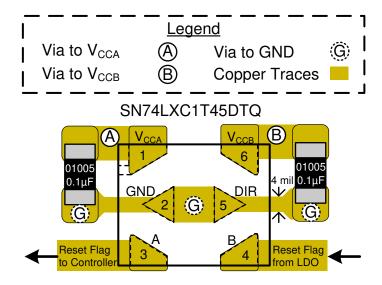


Figure 11-1. Layout Example - SN74LXC1T45

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Regulatory Requirements

No statutory or regulatory requirements apply to this device.

There are no special characteristics for this product.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

· Texas Instruments, Understanding Schmitt Triggers application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74LXC1T45DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2LSF
SN74LXC1T45DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2LSF
SN74LXC1T45DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1L1
SN74LXC1T45DCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1L1
SN74LXC1T45DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MK
SN74LXC1T45DRYR.A	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MK
SN74LXC1T45DTQR	Active	Production	X2SON (DTQ) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ME
SN74LXC1T45DTQR.A	Active	Production	X2SON (DTQ) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ME

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LXC1T45:

Automotive: SN74LXC1T45-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



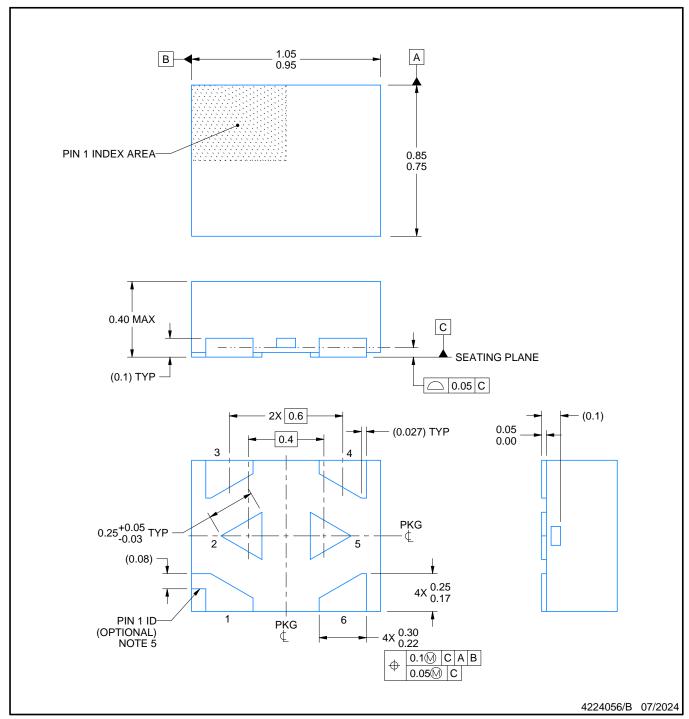


NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





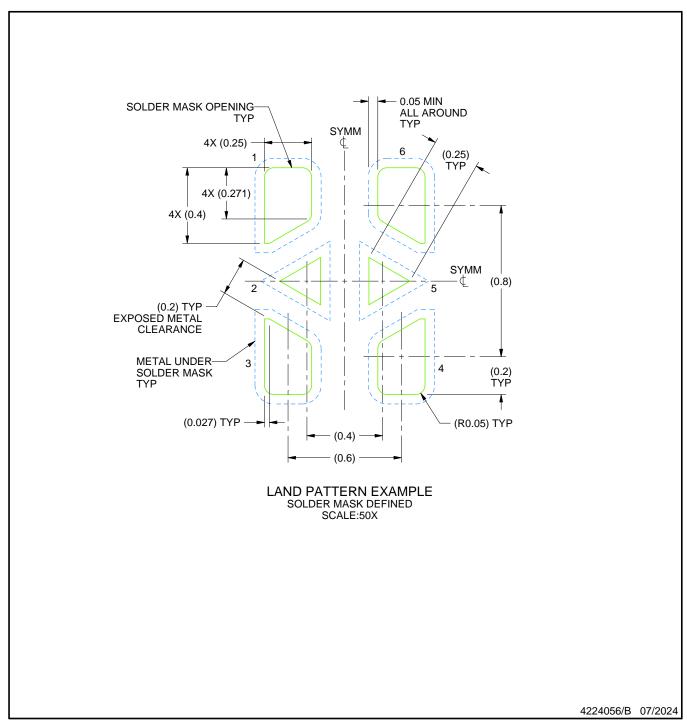


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

 4. The size and shape of this feature may vary.
- 5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.



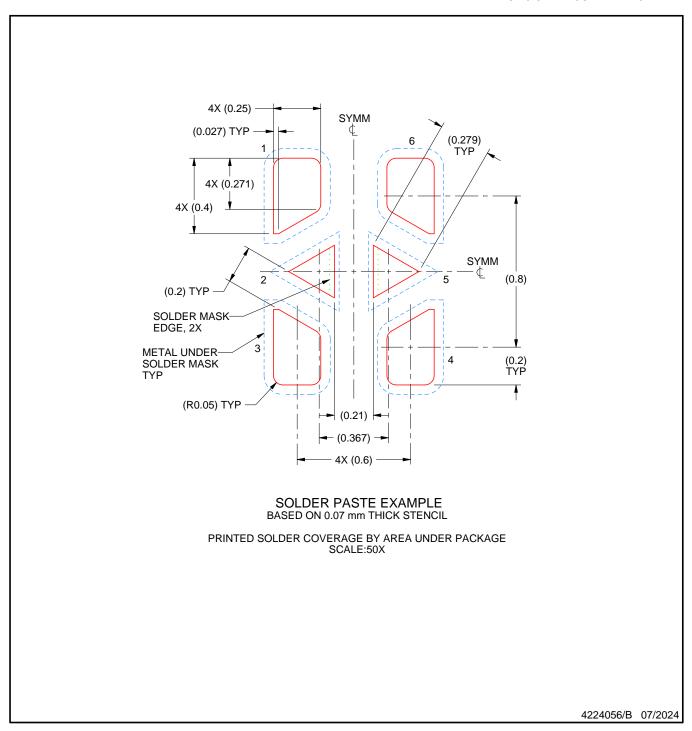


NOTES: (continued)



^{6.} This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

^{7.} Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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