# SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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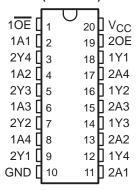
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## description/ordering information

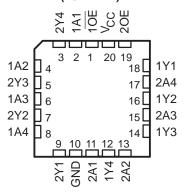
These octal buffers/drivers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH241 devices are organized as two 4-bit line drivers with separate output-enable  $(1\overline{OE}, 2OE)$  inputs. When  $1\overline{OE}$  is low or 2OE is high, the devices pass noninverted data from the A inputs to the Y outputs. When  $1\overline{OE}$  is high or 2OE is low, the outputs are in the high-impedance state.

SN54LVTH241 . . . J OR W PACKAGE SN74LVTH241 . . . DB, DW, NS, OR PW PACKAGE (TOP VIEW)



SN54LVTH241 . . . FK PACKAGE (TOP VIEW)



Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

#### ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	0010 011	Tube	SN74LVTH241DW	IV/TU044		
–40°C to 85°C	SOIC - DW	Tape and reel	SN74LVTH241DWR	LVTH241		
	SOP - NS	Tape and reel	SN74LVTH241NSR	LVTH241		
	SSOP – DB	Tape and reel	SN74LVTH241DBR	LXH241		
		Tube	SN74LVTH241PW	1.7/1/0.44		
	TSSOP – PW	Tape and reel	SN74LVTH241PWR	LXH241		
	CDIP – J	Tube	SNJ54LVTH241J	SNJ54LVTH241J		
−55°C to 125°C	CFP – W	Tube	SNJ54LVTH241W	SNJ54LVTH241W		
	LCCC – FK	Tube	SNJ54LVTH241FK	SNJ54LVTH241FK		

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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## description/ordering information (continued)

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

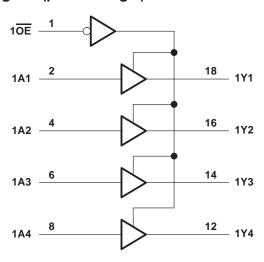
These devices are fully specified for hot-insertion applications using I<sub>off</sub> and power-up 3-state. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

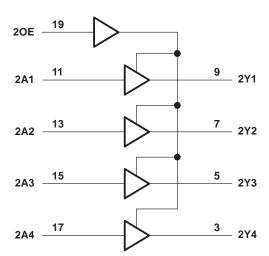
#### **FUNCTION TABLES**

INPU	JTS	OUTPUT
10E	1A	1Y
L	Н	Н
L	L	L
Н	Χ	Z

INP	UTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	X	Z

## logic diagram (positive logic)







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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	
or power-off state, V <sub>O</sub> (see Note 1)	7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) –0.5 V to $V_{CC}$ + 0.5	
Current into any output in the low state, IO: SN54LVTH241	mΑ
SN74LVTH241 128 m	mΑ
Current into any output in the high state, IO (see Note 2): SN54LVTH241	mΑ
SN74LVTH241 64 m	mΑ
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	mΑ
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	mΑ
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DB package	:/W
DW package 58°C/	
NS package 60°C/	
PW package 83°C/	
Storage temperature range, T <sub>stg</sub> 65°C to 150°	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			SN54LV	ГН241	SN74LV	TH241	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	2	2		V
V <sub>IL</sub>	Low-level input voltage			0.8		8.0	V
VI	Input voltage					5.5	V
loн	High-level output current		1	-24		-32	mA
loL	Low-level output current		2	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	20/	10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			ALDITIONS.	SN	54LVTH	241	SN.	74LVTH2	241		
PA	RAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	MIN	TYP†	MAX	UNIT	
٧ıK		$V_{CC} = 2.7 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0	.2		V <sub>CC</sub> -0	.2			
V		$V_{CC} = 2.7 \text{ V},$	$I_{OH} = -8 \text{ mA}$	2.4			2.4			V	
VOH		V 2.V	$I_{OH} = -24 \text{ mA}$	2						V	
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = -32 mA				2				
		V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 μA			0.2			0.2		
		vCC = 2.7 v	$I_{OL} = 24 \text{ mA}$			0.5			0.5		
V			$I_{OL} = 16 \text{ mA}$			0.4			0.4	V	
$V_{OL}$		V <sub>CC</sub> = 3 V	$I_{OL} = 32 \text{ mA}$			0.5			0.5	V	
		ACC = 2 A	$I_{OL} = 48 \text{ mA}$			0.55					
			$I_{OL} = 64 \text{ mA}$						0.55		
		$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	V <sub>I</sub> = 5.5 V			10			10	ı	
1.	Control inputs	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND			<u>&amp;</u> ±1			±1		
l <sub>l</sub>	Data inputs	V <sub>CC</sub> = 3.6 V	VI = VCC		3	1			1	μΑ	
	Data inputs	ACC = 3.9 A	V <sub>I</sub> = 0		4	<b>–</b> 5			-5		
I <sub>off</sub>		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5 $V$		Z.				±100	μΑ	
		V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V	75	5		75				
I <sub>I(hold)</sub>	Data inputs		V <sub>I</sub> = 2 V	-75	9		-75			μΑ	
·i(noid)	Data inputo	V <sub>CC</sub> = 3.6 V <sup>‡</sup> ,	V <sub>I</sub> = 0 to 3.6 V	2	,		500 -750			μ	
lozh		$V_{CC} = 3.6 \text{ V},$	V <sub>O</sub> = 3 V			5			5	μΑ	
l <sub>OZL</sub>		$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$			-5			-5	μΑ	
lozpu		$\frac{V_{CC}}{OE/OE} = 0$ to 1.5 V, $V_{O} = \frac{V_{CC}}{OE/OE} = 0$	0.5 V to 3 V,			±100*			±100	μΑ	
lozpd		$\frac{\text{VCC}}{\text{OE/OE}} = 1.5 \text{ V to 0, V}_{\text{O}} = \frac{\text{VCC}}{\text{OE/OE}} = \frac{\text{VCC}}{\text{OE/OE}} = \frac{\text{VCC}}{\text{OE/OE}} = \frac{\text{VCC}}{\text{VCC}} = \frac{\text{VCC}}$	0.5 V to 3 V,			±100*			±100	μΑ	
		V <sub>CC</sub> = 3.6 V,	Outputs high			0.19			0.19		
ICC		$I_{O} = 0$ ,	Outputs low			5			5	mA	
	$V_I = V_{CC}$ or GND		Outputs disabled			0.19			0.19		
ΔI <sub>CC</sub> §		$V_{CC} = 3 \text{ V to } 3.6 \text{ V, On}$ Other inputs at $V_{CC}$ or	e input at V <sub>CC</sub> – 0.6 V, GND			0.2		_	0.2	mA	
Ci		V <sub>I</sub> = 3 V or 0			3			3		pF	
Со		V <sub>O</sub> = 3 V or 0			7			7		pF	

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup>This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than VCC or GND.

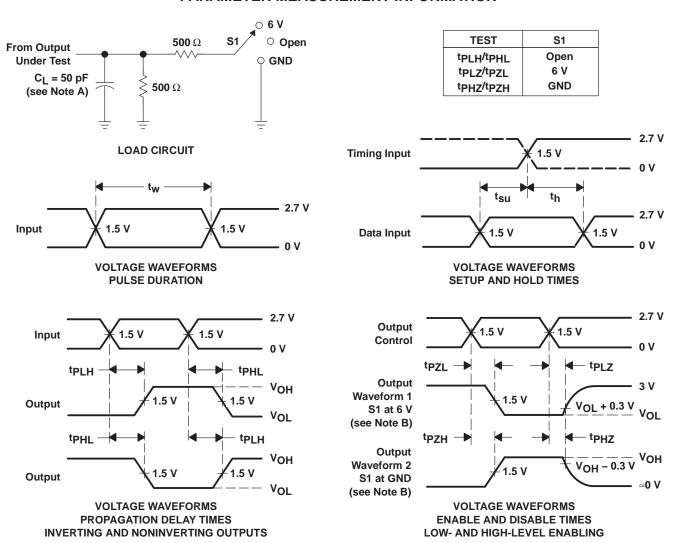
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)		SN54LVTH241				SN74LVTH241					
PARAMETER	FROM (INPUT)		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
<sup>t</sup> PLH	А		1	3.7	4	4	1.1	2.3	3.5		3.9	20	
t <sub>PHL</sub>		Y	1.2	3.5	3/4	3.7	1.3	2.2	3.4		3.6	ns	
<sup>t</sup> PZH	OE or OE	V	1	4.6	9	5.5	1.1	2.7	4.5		5.4	20	
t <sub>PZL</sub>	OE or OE	Y	1.3	4.6		5.1	1.4	2.9	4.4		5	ns	
t <sub>PHZ</sub>	OE or OE	V	1.5	4.7		5.5	1.6	2.8	4.5		5.3		
tPLZ	OE OF OE	Υ	1.7	5		5.5	1.8	3	4.7		5.2	ns	

 $<sup>^{\</sup>dagger}$  All typical values are at VCC = 3.3 V, TA = 25°C.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LVTH241DBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241
SN74LVTH241DBR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241
SN74LVTH241DW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH241
SN74LVTH241DW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH241
SN74LVTH241DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH241
SN74LVTH241DWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH241
SN74LVTH241DWRG4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH241
SN74LVTH241PW	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241
SN74LVTH241PW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241
SN74LVTH241PWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241
SN74LVTH241PWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241
SN74LVTH241PWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241
SN74LVTH241PWRG4.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH241

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH241DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTH241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVTH241PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVTH241PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



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## \*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH241DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVTH241DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVTH241PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVTH241PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0

## **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVTH241DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVTH241DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVTH241PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVTH241PW.B	PW	TSSOP	20	70	530	10.2	3600	3.5



SOIC



## NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







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  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

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- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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