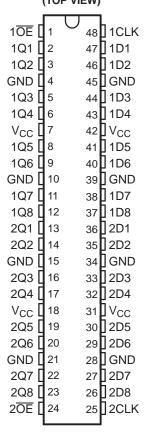


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FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS
 Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH16374... WD PACKAGE SN74LVTH16374... DGG OR DL PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'LVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

T _A	T _A PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	FBGA – GRD		SN74LVTH16374GRDR	11074
	FBGA – ZRD (Pb-free)	Reel of 1000	SN74LVTH16374ZRDR	LL374
		T., b = =4.05	SN74LVTH16374DL	
SSOP – DL	Tube of 25	74LVTH16374DLG4	1.)/TU40074	
400C to 050C	550P - DL	Deal of 4000	SN74LVTH16374DLR	LVTH16374
–40°C to 85°C		Reel of 1000	74LVTH16374DLRG4	
	TSSOP – DGG	David of 2000	SN74LVTH16374DGGR	1.)/TU40074
	1880P – DGG	Reel of 2000	74LVTH16374DGGRG4	LVTH16374
	VFBGA – GQL	Reel of 1000	SN74LVTH16374KR	11074
	VFBGA – ZQL (Pb-free)		SN74LVTH16374ZQLR	LL374
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16374WD	SNJ54LVTH16374WD

⁽¹⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

⁽²⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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GQL OR ZQL PACKAGE (TOP VIEW)

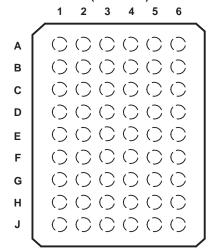
		1	2	3	4	5	6	
Α) (()	()	()	()	1
В	() ()	()	()	()	()	
С	() ()	()	()	()	()	
D	() ()	()	()	()	()	
Е	() ()			()	()	
F	() ()			()	()	
G	() ()	()	()	()	()	
н	() ()	()	()	()	()	
J	() (()	()	()	()	()	
K	() (()	()	()	()	()	J

TERMINAL ASSIGNMENTS⁽¹⁾ (56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
Α	1 OE	NC	NC	NC	NC	1CLK
В	1Q2	1Q1	GND GND		1D1	1D2
С	1Q4	1Q3	V _{CC}	V _{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
Н	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 OE	NC	NC	NC	NC	2CLK

(1) NC - No internal connection

GRD OR ZRD PACKAGE (TOP VIEW)



TERMINAL ASSIGNMENTS⁽¹⁾ (54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
Α	1Q1	NC	1 OE	1CLK	NC	1D1
В	1Q3	1Q2	NC	NC	1D2	1D3
С	1Q5	1Q4	V_{CC}	V _{CC}	1D4	1D5
D	1Q7	1Q6	GND	GND	1D6	1D7
E	2Q1	1Q8	GND	GND	1D8	2D1
F	2Q3	2Q2	GND	GND	2D2	2D3
G	2Q5	2Q4	V_{CC}	V _{CC}	2D4	2D5
Н	2Q7	2Q6	NC	NC	2D6	2D7
J	2Q8	NC	2 OE	2CLK	NC	2D8

(1) NC - No internal connection

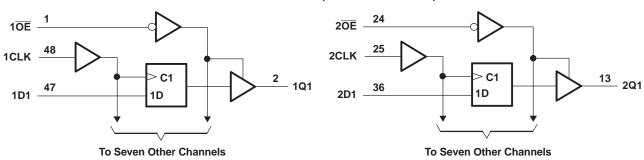
FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q_0
Н	Χ	Χ	Z

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LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range (2)		-0.5	7	V
Vo	Voltage range applied to any output in the high-in	npedance or power-off state ⁽²⁾	-0.5	7	V
Vo	Voltage range applied to any output in the high st	ate ⁽²⁾	-0.5	V _{CC} + 0.5	V
	Owner of Safety and another than the characters	SN54LVTH16374		96	1
I _O	Current into any output in the low state	SN74LVTH16374		128	mA
	Comment into any automatic the binds atom (3)	SN54LVTH16374		48	A
I _O	Current into any output in the high state (3)	SN74LVTH16374		64	mA
I _{IK}	Input clamp current	V _I < 0		- 50	mA
I _{OK}	Output clamp current	V _O < 0		- 50	mA
		DGG package		70	
0	Package thermal impedance (4)	DL package		63	°C/W
θ_{JA}	rackage thermal impedance.	GQL/ZQL package		42	C/VV
		GRD/ZRD package		36	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽³⁾ This current flows only when the output is in the high state and $V_O > V_{CC}$.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



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Recommended Operating Conditions⁽¹⁾

			SN54LVTH	116374	SN74LVTH	16374	LINUT
			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
I _{OH}	High-level output current			-24		-32	mA
I _{OL}	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T _A	Operating free-air temperature		-55	125	-40	85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.





Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	DAMETED	TEST CO	NDITIONS	SN54	LVTH16374	4	SN74	LVTH163	74	LINUT
PA	RAMETER	IESI CO	NDITIONS	MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 2.7 V,$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I _{OH} = -100 μA	V _{CC} - 0.2			V _{CC} - 0.2			
V _{OH}		$V_{CC} = 2.7 \text{ V},$	$I_{OH} = -8 \text{ mA}$	2.4			2.4			V
0		V _{CC} = 3 V	$I_{OH} = -24 \text{ mA}$	2						
		v _{CC} = 3 v	$I_{OH} = -32 \text{ mA}$				2			
		V _{CC} = 2.7 V	$I_{OL} = 100 \mu A$			0.2			0.2	
		VCC = 2.7 V	$I_{OL} = 24 \text{ mA}$			0.5			0.5	
V _{OL}			$I_{OL} = 16 \text{ mA}$			0.4			0.4	V
VOL		V _{CC} = 3 V	I _{OL} = 32 mA			0.5			0.5	V
		vCC = 3 v	$I_{OL} = 48 \text{ mA}$			0.55				
			$I_{OL} = 64 \text{ mA}$						0.55	
		$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	$V_1 = 5.5 \text{ V}$			10			10	
I _I	Control inputs	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND			±1			±1	μΑ
	Data inputs	V _{CC} = 3.6 V	$V_I = V_{CC}$			1			1	
	Data Inputs	V _{CC} = 3.0 V	$V_I = 0$			– 5			– 5	
I _{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V						±100	μΑ
		V _{CC} = 3 V	$V_1 = 0.8 \ V$	75			75			
I _{I(hold)}	Data inputs	VCC = 3 V	V _I = 2 V	-75			– 75			μΑ
I(IIOIG)	, , , ,	$V_{CC} = 3.6 \text{ V},^{(2)}$	$V_1 = 0 \text{ to } 3.6 \text{ V}$						500 -750	·
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V			5			5	μA
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V			- 5			- 5	μA
I _{OZPU}		$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,		:	±100 ⁽³⁾			±100	μΑ
I _{OZPD}		$\frac{V_{CC}}{OE}$ = 1.5 V to 0, V _O = $\frac{V_{CC}}{OE}$ = don't care	= 0.5 V to 3 V,		:	±100 ⁽³⁾			±100	μΑ
		V _{CC} = 3.6 V,	Outputs high			0.19			0.19	
I_{CC}		$I_{O} = 0$	Outputs low			5			5	mA
		$V_I = V_{CC}$ or GND	Outputs disabled			0.19			0.19	
ΔI _{CC} ⁽⁴⁾		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ One input at $V_{CC} = 0$ Other inputs at V_{CC} or	.6 V, r GND			0.2			0.2	mA
C _I		V _I = 3 V or 0			3			3		pF
Co		$V_O = 3 \text{ V or } 0$			9			9		pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

⁽²⁾ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

⁽³⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.

⁽⁴⁾ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			S	N54LVT	H16374		S	N74LV	ГН16374		
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			160		160		160		160	MHz
t _w	Pulse duration, CLK high or low		3		3		3		3		ns
t _{su}	Setup time, data before CLK↑	High or low	2.9		3.3		1.8		2		ns
t _h	Hold time, data after CLK↑	High or low	0.8		0.2		0.8		0.1		ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

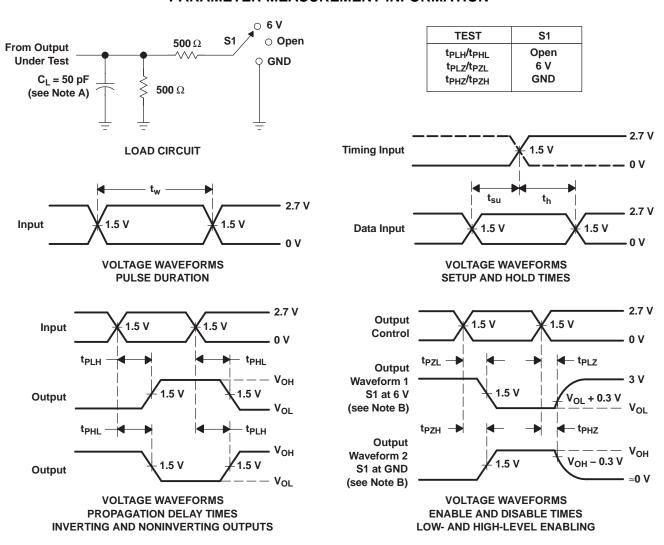
			SN	54LVT	H16374			SN74	LVTH1	6374		
PARAMETER FROM (INPUT)		TO (OUTPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP ⁽¹⁾	MAX	MIN	MAX	
f _{max}			160		160		160			160		MHz
t _{PLH}	CLK	Q	1.4	5.6		6.2	1.9	3	4.5		5.2	no
t _{PHL}	CLN	Q	1.7	4.8		5	2.1	2.9	4		4.2	ns
t _{PZH}	ŌĒ	0	1	5.6		6.4	1.5	2.8	4.5		5.4	
t _{PZL}	OE	Q	1.4	5.5		6.2	1.5	2.8	4.4		5	ns
t _{PHZ}	ŌĒ	0	1	6.4		6.9	2.4	3.5	5		5.4	
t _{PLZ}	OE .	Q	1.7	5		5.2	2	3.2	4.6		4.8	ns
t _{sk(LH)}									0.5			20
t _{sk(HL)}									0.5			ns

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
74LVTH16374DGGR1G4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
74LVTH16374DGGR1G4.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DL.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DLR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DLRG4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DLRG4.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVTH16374:

● Enhanced Product: SN74LVTH16374-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVTH16374DGGR1G4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVTH16374DLRG4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1



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*All dimensions are nominal

7 III dill'orio di Ciricini di									
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)		
74LVTH16374DGGR1G4	TSSOP	DGG	48	2000	356.0	356.0	45.0		
SN74LVTH16374DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0		
SN74LVTH16374DLR	SSOP	DL	48	1000	356.0	356.0	53.0		
SN74LVTH16374DLRG4	SSOP	DL	48	1000	356.0	356.0	53.0		

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVTH16374DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVTH16374DL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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