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#### **FEATURES**

- Members of the Texas Instruments Widebus™
   Family
- Output Ports Have Equivalent 22- $\Omega$  Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH162374... WD PACKAGE SN74LVTH162374... DGG OR DL PACKAGE (TOP VIEW)

	T	$\mathcal{T}$	-
1 <del>0E</del>	∐1 `	48	1CLK
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	[]4	45	] GND
1Q3	5	44	1D3
1Q4	6	43	] 1D4
$V_{CC}$	7	42	$V_{CC}$
1Q5	8	41	] 1D5
1Q6	9	40	] 1D6
GND	10	39	GND
1Q7	11	38	] 1D7
1Q8	12	37	] 1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	<b>[</b> ] 16	33	2D3
2Q4	17	32	2D4
$V_{CC}$	18	31	$]$ $V_{CC}$
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	] GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2 <mark>OE</mark>	24	25	] 2CLK

## **DESCRIPTION/ORDERING INFORMATION**

# **ORDERING INFORMATION**

T <sub>A</sub>	PACKAGI	<u>=</u> (1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	FBGA – GRD	Davi of 4000	74LVTH162374GRDR	11.0074
	FBGA – ZRD (Pb-free)	Reel of 1000	74LVTH162374ZRDR	LL2374
		Tubo of 25	SN74LVTH162374DL	
	SSOP – DL	Tube of 25	SN74LVTH162374DLG4	L \/TLI400074
–40°C to 85°C	550P – DL	Reel of 1000	74LVTH16374DLRG4	LVTH162374
-40°C 10 65°C		Reel of 1000	SN74LVTH16374DLR	
	TOCOD DOC	Deal of 2000	SN74LVTH162374DGGR	L \/TLI462274
	TSSOP – DGG	Reel of 2000	74LVTH162374DGGRG4	LVTH162374
	VFBGA – GQL	Deal of 1000	SN74LVTH162374GQLR	- LL2374
	VFBGA – ZQL (Pb-free)	Reel of 1000	74LVTH162374ZQLR	LL23/4
-55°C to 125°C		Tube	SNJ54LVTH162374WD	SNJ54LVTH162374WD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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# **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The 'LVTH162374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent  $22-\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

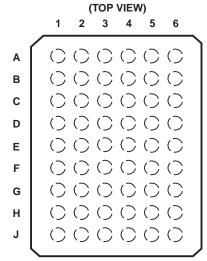
These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

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# GQL OR ZQL PACKAGE (TOP VIEW)

		1	2	3	4	5	6	
Α	$^{\prime}$	()		()	()	()		1
В		()	()	()	()	()	()	ı
С		()	()	()	()	()	()	ı
D		()	()	()	()	()	()	ı
Е		()	()			()	()	ı
F		()	()			()	()	ı
G		()	()	()	()	()	()	ı
Н		()	()	()	()	()	()	ı
J		()	()	()	()	()	()	ı
K		()	()	()	()	()	()	J

# GRD OR ZRD PACKAGE



# TERMINAL ASSIGNMENTS<sup>(1)</sup> (56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
Α	1 <del>OE</del>	NC	NC	NC	NC	1CLK
В	1Q2	1Q1	GND	GND	1D1	1D2
С	1Q4	1Q3	V <sub>CC</sub>	V <sub>CC</sub>	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
Н	2Q5	2Q6	V <sub>CC</sub>	V <sub>CC</sub>	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 <del>OE</del>	NC	NC	NC	NC	2CLK

(1) NC - No internal connection

# TERMINAL ASSIGNMENTS<sup>(1)</sup> (54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
Α	1Q1	NC	1 <del>OE</del>	1CLK	NC	1D1
В	1Q3	1Q2	NC	NC	1D2	1D3
С	1Q5	1Q4	V <sub>CC</sub>	V <sub>CC</sub>	1D4	1D5
D	1Q7	1Q6	GND	GND	1D6	1D7
E	2Q1	1Q8	GND	GND	1D8	2D1
F	2Q3	2Q2	GND	GND	2D2	2D3
G	2Q5	2Q4	V <sub>CC</sub>	V <sub>CC</sub>	2D4	2D5
Н	2Q7	2Q6	NC	NC	2D6	2D7
J	2Q8	NC	2 <del>OE</del>	2CLK	NC	2D8

(1) NC - No internal connection

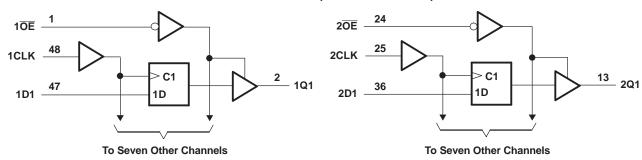
# FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	<b>↑</b>	Н	Н
L	$\uparrow$	L	L
L	H or L	Χ	$Q_0$
Н	X	Χ	Z

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# **LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG, DL, and WD packages.

# Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	4.6	V
VI	Input voltage range (2)		-0.5	7	V
Vo	Voltage range applied to any output in the h	-0.5	7	V	
Vo	Voltage range applied to any output in the h	igh state <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
Io	Current into any output in the low state			30	mA
Io	Current into any output in the high state (3)		30	mA	
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
		DGG package		70	
0	Dealers thereal impacts are (4)	DL package		63	0000
$\theta_{JA}$	Package thermal impedance (4)	GQL/ZQL package		42	°C/W
		GRD/ZRD package		36	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# Recommended Operating Conditions<sup>(1)</sup>

			SN54LVTH	162374	SN74LVTH1	162374	LINUT
			MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	<b>V</b>
I <sub>OH</sub>	High-level output current			-12		-12	mA
I <sub>OL</sub>	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

<sup>(1)</sup> All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

<sup>(2)</sup> The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(3)</sup> This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEGT	CONDITIONS	SN54	4LVTH162	2374	SN74	LVTH16	2374	UNIT
,	PARAMETER	1531	CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	UNII
$V_{IK}$		V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -12 mA	2			2			V
$V_{OL}$		V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 12 mA			0.8			8.0	V
		$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	$V_{I} = 5.5 \text{ V}$			10			10	
	Control inputs	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND			±1			±1	
I <sub>I</sub>	Doto inputo	V <sub>CC</sub> = 3.6 V	$V_I = V_{CC}$			1			1	μΑ
	Data inputs	v <sub>CC</sub> = 3.6 v	$V_I = 0$			-5			-5	
I <sub>off</sub>		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5 V						±100	μΑ
		V 2.V	V <sub>I</sub> = 0.8 V	75			75			
I <sub>I(hold)</sub>	Data inputs	$V_{CC} = 3 V$	V <sub>I</sub> = 2 V	-75			-75			μA
'I(hold)	Data inputs	V <sub>CC</sub> = 3.6 V, <sup>(2)</sup>	V <sub>I</sub> = 0 to 3.6 V						500 -750	μπ
I <sub>OZH</sub>	1	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V			5			5	μΑ
I <sub>OZL</sub>			V <sub>O</sub> = 0.5 V			-5			-5	μΑ
I <sub>OZPU</sub>		$\frac{V_{CC}}{OE}$ = 0 to 1.5 V, $V_{O}$	= 0.5 V to 3 V,		=	±100 <sup>(3)</sup>			±100	μΑ
I <sub>OZPD</sub>		$\frac{V_{CC}}{OE}$ = 1.5 V to 0, $V_{O}$	= 0.5 V to 3 V,		=	±100 <sup>(3)</sup>			±100	μΑ
		V <sub>CC</sub> = 3.6 V,	Outputs high			0.19			0.19	
$I_{CC}$		$I_{O} = 0$ ,	Outputs low			5			5	mA
		$V_I = V_{CC}$ or GND	Outputs disabled			0.19			0.19	
ΔI <sub>CC</sub> <sup>(4)</sup>		$V_{CC} = 3 \text{ V to } 3.6 \text{ V, C}$ Other inputs at $V_{CC}$ o	One input at V <sub>CC</sub> – 0.6 V, or GND			0.2			0.2	mA
Ci		V <sub>I</sub> = 3 V or 0			3			3		pF
Co		$V_0 = 3 \text{ V or } 0$			9			9		pF

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# **Timing Requirements**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN	SN54LVTH162374				N54LVT	H162374		
			V <sub>CC</sub> = 3 ± 0.3	3.3 V V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = 3 ± 0.3	3.3 V 3 V	V <sub>CC</sub> = 2	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			160		160		160		160	MHz
t <sub>w</sub>	Pulse duration, CLK high or low		3		3.3		3		3		ns
t <sub>su</sub>	Setup time, data before CLK↑	High or low	2.8		3.2		1.8		2		ns
t <sub>h</sub>	Hold time, data after CLK↑	High or low	1.2		0.5		0.8		0.1		ns

<sup>(2)</sup> This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

<sup>(3)</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

<sup>(4)</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.



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# **Switching Characteristics**

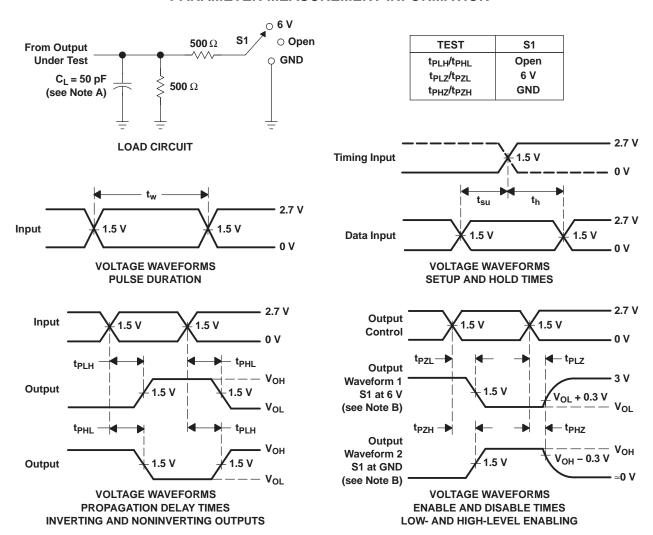
over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

			SN	54LVTH	1162374	4		SN74L	VTH16	2374		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3 ± 0.3	$V_{CC}$ = 3.3 V $\pm$ 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	MAX	
f <sub>max</sub>			160		160		160			160		MHz
t <sub>PLH</sub>	CLK	Q	1.4	6.6		7.4	2	3.4	5.3		6.2	ns
t <sub>PHL</sub>	CLK	Q	1.4	5.8		6	2.2	3.3	4.9		5.1	113
t <sub>PZH</sub>	ŌĒ	0	1	6.6		7.4	1.8	3.5	5.6		6.9	20
t <sub>PZL</sub>	OE	Q	1.4	6		6.8	1.8	3.5	4.9		6	ns
t <sub>PHZ</sub>	ŌĒ	0	1	6.6		7.4	2.4	4.2	5.4		5.7	20
t <sub>PLZ</sub>	OE	Q	1.4	6		6	2	3.8	5		5.1	ns
t <sub>sk(LH)</sub>									0.5			ns
t <sub>sk(HL)</sub>									0.5			115

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_r \leq$  2.5 ns.  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
5962-9854201VXA	Active	Production	CFP (WD)   48	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9854201VX A SNV54LVTH16237 4WD
8W2374DGGRG4	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374
8W2374DGGRG4.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374
SN74LVTH162374DGGR	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374
SN74LVTH162374DGGR.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374
SN74LVTH162374DL	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374
SN74LVTH162374DL.B	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374
SN74LVTH162374DLR	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374
SN74LVTH162374DLR.B	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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# **PACKAGE MATERIALS INFORMATION**

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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
8W2374DGGRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH162374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH162374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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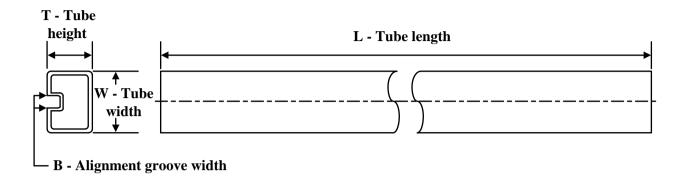
#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
8W2374DGGRG4	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVTH162374DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVTH162374DLR	SSOP	DL	48	1000	356.0	356.0	53.0

# **PACKAGE MATERIALS INFORMATION**

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# **TUBE**



### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVTH162374DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVTH162374DL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87



SMALL OUTLINE PACKAGE



## NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



# DGG (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

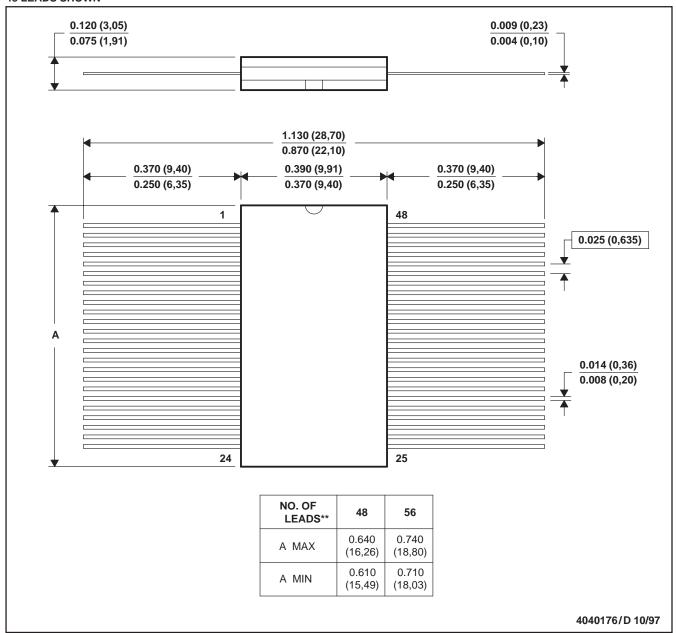
C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

# WD (R-GDFP-F\*\*)

#### **CERAMIC DUAL FLATPACK**

### **48 LEADS SHOWN**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB

# DL (R-PDSO-G48)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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