SCBS746B - JULY 2000 - REVISED OCTOBER 2003

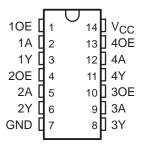
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# description/ordering information

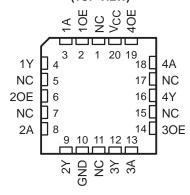
These bus buffers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH126 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (OE) input is low.

SN54LVTH126 . . . J OR W PACKAGE SN74LVTH126 . . . D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



# SN54LVTH126 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

#### **ORDERING INFORMATION**

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	0010 B	Tube	SN74LVTH126D	1)/71/400	
	SOIC - D	Tape and reel	SN74LVTH126DR	LVTH126	
	SOP - NS	Tape and reel	SN74LVTH126NSR	LVTH126	
-40°C to 85°C	SSOP – DB	Tape and reel	SN74LVTH126DBR	LXH126	
	TSSOP – PW	Tube	SN74LVTH126PW	LXH126	
	1550P – PW	Tape and reel	SN74LVTH126PWR	LXH126	
	TVSOP - DGV	Tape and reel	SN74LVTH126DGVR	LXH126	
	CDIP – J	Tube	SNJ54LVTH126J	SNJ54LVTH126J	
–55°C to 125°C	CFP – W	Tube	SNJ54LVTH126W	SNJ54LVTH126W	
	LCCC – FK	Tube	SNJ54LVTH126FK	SNJ54LVTH126FK	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



# **SN54LVTH126, SN74LVTH126** 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

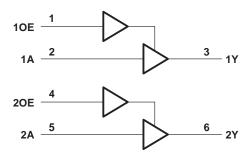
When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

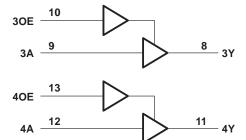
These devices are fully specified for hot-insertion applications using Ioff and power-up 3-state. The Ioff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**FUNCTION TABLE** (each buffer)

INP	JTS	OUTPUT
OE	Α	Υ
Н	Н	Н
Н	L	L
L	Χ	Z

### logic diagram (positive logic)





Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.



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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)		
Voltage range applied to any output in the high-i	impedance	
or power-off state, V <sub>O</sub> (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high s	state, V <sub>O</sub> (see Note 1)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Current into any output in the low state, IO: SNS	54LVTH126	96 mA
SN7	74LVTH126	128 mA
Current into any output in the high state, IO (see	Note 2): SN54LVTH126	48 mA
	SN74LVTH126	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	D package	86°C/W
	DB package	96°C/W
	DGV package	127°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, T <sub>stg</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# recommended operating conditions (see Note 4)

			SN54LV	ГН126	SN74LV	TH126	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	K	2		V
V <sub>IL</sub>	Low-level input voltage			0.8		8.0	V
VI	Input voltage		40	5.5		5.5	V
loн	High-level output current		6	-24		-32	mA
lOL	Low-level output current		20	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	90	10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# SN54LVTH126, SN74LVTH126 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN	54LVTH1	126	SN	74LVTH1	26		
PAI	RAMETER	TEST CO	ONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT	
٧ıK		$V_{CC} = 2.7 \text{ V},$	I <sub>I</sub> = -18 mA			-1.2			-1.2	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	$I_{OH} = -100  \mu A$	VCC-0	.2		VCC-0	.2			
.,		$V_{CC} = 2.7 \text{ V},$	$I_{OH} = -8 \text{ mA}$	2.4			2.4			V	
VOH		Vaa - 2 V	$I_{OH} = -24 \text{ mA}$	2						V	
		VCC = 3 V	$I_{OH} = -32 \text{ mA}$				2				
		Voo - 27V	$I_{OL} = 100  \mu A$			0.2			0.2		
		V <sub>CC</sub> = 2.7 V	$I_{OL} = 24 \text{ mA}$			0.5			0.5		
V			$I_{OL} = 16 \text{ mA}$			0.4			0.4	V	
V <sub>OL</sub>	N 2 V	$I_{OL} = 32 \text{ mA}$			0.5			0.5	V		
	V <sub>CC</sub> = 3 V	$I_{OL} = 48 \text{ mA}$			0.55						
			$I_{OL} = 64 \text{ mA}$			2			0.55		
		$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	V <sub>I</sub> = 5.5 V		4	10			10		
1.	Control inputs	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND		±1				±1	μΑ	
i <sub>I</sub>	Data innuta	V 20V	$V_I = V_{CC}$		1	1		1			
	Data inputs	ACC = 3.9 A	V <sub>I</sub> = 0		2	-5			-5		
l <sub>off</sub>		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5 V	0	Õ,				±100	μΑ	
		W 2 W	V <sub>I</sub> = 0.8 V	75			75				
I <sub>I(hold)</sub>	Data inputs	$V_{CC} = 3.6 \text{ V}$ $V_{CC} = 0,$ $V_{CC} = 3 \text{ V}$ $V_{CC} = 3 \text{ V}$ $V_{CC} = 3.6 \text{ V}^{\ddagger},$ $V_{I}$	V <sub>I</sub> = 2 V	-75			-75			μА	
, ,		$V_{CC} = 3.6 V^{\ddagger}$ ,	$V_{I} = 0 \text{ to } 3.6 \text{ V}$						±500		
lozh		$V_{CC} = 3.6 \text{ V},$	VO = 3 V			5			5	μΑ	
lozL		$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$			-5			-5	μΑ	
lozpu		$V_{CC} = 0$ to 1.5 V, $V_{O} = 0$ OE = don't care	0.5 V to 3 V,			±50*			±50	μΑ	
lozpd		$V_{CC} = 1.5 \text{ V to } 0, V_{O} = 0$ $OE = \text{don't care}$	0.5 V to 3 V,			±50*			±50	μΑ	
		V <sub>CC</sub> = 3.6 V,	Outputs high		0.12	0.19		0.12	0.19		
ICC		$I_{O} = 0$ ,	Outputs low		4.5	7		4.5	7	mA	
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.12	0.19		0.12	0.19		
ΔICC§		V <sub>CC</sub> = 3 V to 3.6 V, One Other inputs at V <sub>CC</sub> or 0				0.3			0.2	mA	
Ci		V <sub>I</sub> = 3 V or 0			4			4		pF	
Со		V <sub>O</sub> = 3 V or 0			6.5			6.5		pF	

On products compliant to MIL-PRF-38535, this parameter is not production tested.



<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>&</sup>lt;sup>‡</sup> This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

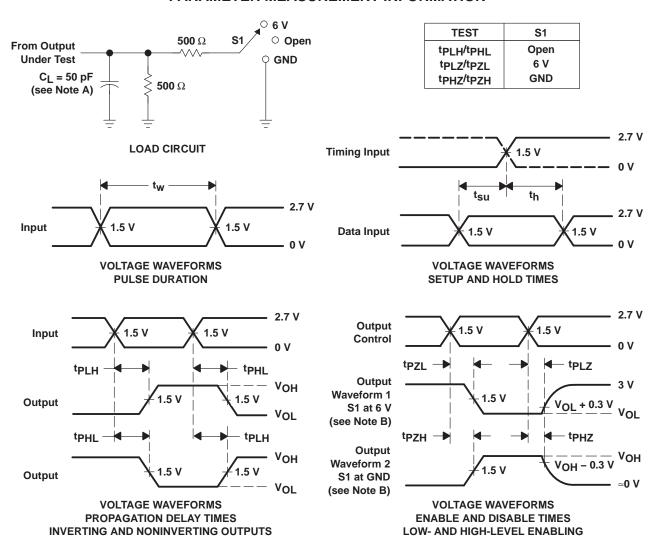
# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

				SN54L\	/TH126			SN7	74LVTH1	26			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX		
t <sub>PLH</sub>	А	~	1	4.8	4	5.5	1	2.3	3.8		4.5	20	
<sup>t</sup> PHL		Y	1	4.9	Y's	5.4	1	2.4	3.9		4.4	ns	
<sup>t</sup> PZH	0.	V	1	6.4	ζ.	7.1	1	3.6	5.4		6.1	20	
t <sub>PZL</sub>	OE	Ť	1.1	6.2		6.8	1.1	3.6	5.2		5.8	ns	
<sup>t</sup> PHZ	OE	0.5	V	1	4.8		5.3	1	2.2	3.8		4.3	20
t <sub>PLZ</sub>		Y	1.3	6.5		7.1	1.3	3.6	5.5		6.1	ns	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50~\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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#### **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LVTH126D	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126D.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126DBR	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DBR.B	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DGVR	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DGVR.B	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DGVRG4	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DGVRG4.B	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126DR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126DRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126DRG4.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126NSR.B	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126NSRG4	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126NSRG4.B	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH126
SN74LVTH126PW	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126PW.B	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126PWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126
SN74LVTH126PWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH126

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.



# **PACKAGE OPTION ADDENDUM**

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVTH126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVTH126DGVRG4	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVTH126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVTH126DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVTH126NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVTH126NSRG4	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVTH126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH126DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVTH126DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVTH126DGVRG4	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVTH126DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVTH126DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVTH126NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVTH126NSRG4	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVTH126PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVTH126D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVTH126D.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVTH126PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVTH126PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5



SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# DGV (R-PDSO-G\*\*)

### 24 PINS SHOWN

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







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- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

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NOTES: (continued)

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