











SN74LVCR2245A

SCAS581N - NOVEMBER 1996-REVISED NOVEMBER 2014

# SN74LVCR2245A Octal Bus Transceiver with 3-State Outputs

#### **Features**

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.3 ns at 3.3 V
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors are Required
- Typical V<sub>OLP</sub> (Output Ground Bounce)  $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)  $> 2 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V<sub>CC</sub>)
- I<sub>off</sub> Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

## 2 Applications

- Wearable Health and Fitness Devices
- **Network Switches**
- Servers
- **Tests and Measurements**

## 3 Description

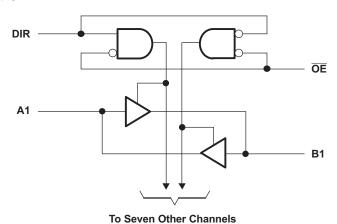
The SN74LVCR2245A device is an octal bus transceiver is designed for 1.65-V to 3.6-V V<sub>CC</sub> operation.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
	SSOP (20)	8.65 mm × 3.90 mm		
	TVSSOP (20)	5.00 mm × 4.40 mm		
SN74LVCR2245A	VQFN (20)	4.50 mm × 3.50 mm		
	SOIC (20)	12.80 mm × 7.50 mm		
	TSSOP (20)	6.50 mm × 4.40 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

# Simplified Schematic





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# 5 Revision History

## Changes from Revision M (March 2005) to Revision N

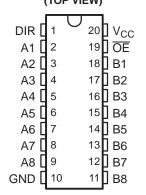
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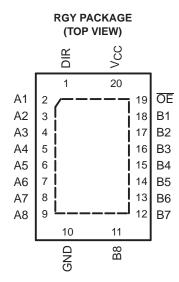
•	Added Applications, Device Information table, Pin Functions table, Handling Ratings table, Thermal Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation	
	Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Deleted Ordering Information table.	1
•	Changed I <sub>off</sub> bullet in <i>Features</i> section.	1
•	Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	6
•	Added –40°C to 125°C temperature range to <i>Electrical Characteristics</i> table	7
•	Changed Switching Characteristics. –40°C to 85°C table.	7



# 6 Pin Configuration and Functions

DB, DBQ, DGV, DW, NS, OR PW PACKAGE (TOP VIEW)





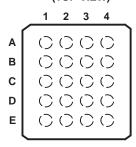
#### **Pin Functions**

	PIN	TVDE	DESCRIPTION			
NO.	NAME	TYPE	DESCRIPTION			
1	DIR	I	Direction Pin			
2	A1	I/O	A1 Input or Output			
3	A2	I/O	A2 Input or Output			
4	A3	I/O	A3 Input or Output			
5	A4	I/O	A4 Input or Output			
6	A5	I/O	A5 Input or Output			
7	A6	I/O	A6 Input or Output			
8	A7	I/O	A7 Input or Output			
9	A8	I/O	A8 Input or Output			
10	GND	_	Ground Pin			
11	B8	I/O	B8 Input or Output			
12	B7	I/O	B7 Input or Output			
13	B6	I/O	B6 Input or Output			
14	B5	I/O	B5 Input or Output			
15	B4	I/O	B4 Input or Output			
16	В3	I/O	B3 Input or Output			
17	B2	I/O	B2 Input or Output			
18	B1	I/O	B1 Input or Output			
19	ŌĒ	I	Output Enable			
20	V <sub>CC</sub>	_	Power Pin			

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# GQN OR ZQN PACKAGE (TOP VIEW)



**Table 1. Pin Assignments** 

	1	2	3	4
Α	A1	DIR	$V_{CC}$	<u>OE</u>
В	А3	B2	A2	B1
С	A5	A4	B4	В3
D	A7	В6	A6	B5
E	GND	A8	B8	B7



## 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
$V_{I}$	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-	-0.5	6.5	V	
Vo	Voltage range applied to any output in the high	or low state (2) (3)	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current		±50	mA	
	Continuous current through V <sub>CC</sub> or GND			±100	mA

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 Handling Ratings

			MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature rang	e	-65	150	ů
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	<b>V</b>
V <sub>(ESD)</sub>		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	0	1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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<sup>2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
.,	Cumply voltage	Operating	1.65	3.6	V
V <sub>CC</sub>	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	
VI	Input voltage		0	5.5	V
\/	Output voltage	High or low state	0	V <sub>CC</sub>	V
Vo		3-state	0	5.5	V
		V <sub>CC</sub> = 1.65 V		-2	
	High lavel autout average	V <sub>CC</sub> = 2.3 V		-4	A
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		-8	mA
		V <sub>CC</sub> = 3 V		-12	
		V <sub>CC</sub> = 1.65 V		2	
	Low lovel output ourrent	V <sub>CC</sub> = 2.3 V		4	A
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		8	mA
		V <sub>CC</sub> = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

<sup>(1)</sup> All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).

## 7.4 Thermal Information

	THERMAL METRIC <sup>(1)</sup>		DBQ	DGV	DB	NS	PW	RGY	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.3	94.7	114.7	94.5	74.7	102.5	41.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	47.9	29.8	56.2	40.5	35.9	47.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	50.9	45.0	56.2	49.7	42.3	53.5	17.1	
ΨЈТ	Junction-to-top characterization parameter	20.0	11.0	0.8	18.1	14.3	2.2	1.4	°C/W
ΨЈВ	Junction-to-board characterization parameter	50.5	44.6	55.5	49.2	41.9	52.9	17.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		_	_	_	_	_	9.8	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).



#### 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMET	TEST COMPITIONS		Т	A = 25°C		-40	)°C to 85°	С	-40	°C to 125	°C	LINIT
ER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	UNIT
	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2			V
	$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			1.2			1.2			
.,	$I_{OH} = -4 \text{ mA}$	2.3 V	1.7			1.7			1.7			
V <sub>OH</sub>	IOH = -4 IIIA	2.7 V	2.2			2.2			2.2			
	$I_{OH} = -6 \text{ mA}$	3 V	2.4			2.4			2.4			
	$I_{OH} = -8 \text{ mA}$	2.7 V	2			2			2			
	$I_{OH} = -12 \text{ mA}$	3 V	2			2			2			
	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2			0.2			0.2	
	$I_{OL} = 2 \text{ mA}$	1.65 V			0.45			0.45			0.45	V
	I <sub>OL</sub> = 4 mA	2.3 V			0.7			0.7			0.7	
V <sub>OL</sub>	I <sub>OL</sub> = 4 IIIA	2.7 V			0.4			0.4			0.4	
	$I_{OL} = 6 \text{ mA}$	3 V			0.55			0.55			0.55	
	$I_{OL} = 8 \text{ mA}$	2.7 V			0.6			0.6			0.6	
	I <sub>OL</sub> = 12 mA	3 V			8.0			0.8			8.0	
I <sub>I</sub> Contr ol inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5			±5			±5	μΑ
I <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$	0			±10			±10			±10	μΑ
I <sub>OZ</sub> <sup>(2)</sup>	$V_0 = 0 \text{ to } 5.5 \text{ V}$	3.6 V			±10			±10			±10	μA
	$V_I = V_{CC}$ or GND	3.6 V			10			10			10	
Icc	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(3)}$ $I_{\text{O}} = 0$	3.0 V			10			10			10	μA
ΔI <sub>CC</sub>	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V			500			500			500	μΑ
C <sub>i</sub> Contr ol inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4								pF
C <sub>io</sub> A or B ports	$V_O = V_{CC}$ or GND	3.3 V		5.5								pF

## 7.6 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> = 2 ± 0.2		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = 3 ± 0.3	3.3 V 3 V	UNIT
	(INPOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A		10.9		7.9	1	7.3	1.5	6.3	ns
t <sub>en</sub>	ŌĒ	A or B		12.6		9.6	1	9.5	1.5	8.2	ns
t <sub>dis</sub>	ŌĒ	A or B		12.1		7.8	1	8.5	1.7	7.8	ns
t <sub>sk(o)</sub>				1		1		1		1	ns

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ . (2) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current. (3) This applies in the disabled state only.



# 7.7 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

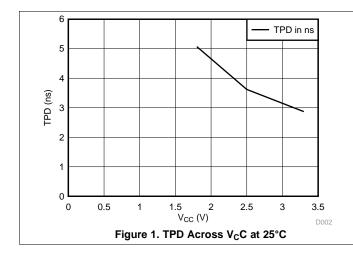
PARAMETER	FROM	TO (OUTPUT)		V <sub>CC</sub> = 1.8 V ± 0.15 V				2.5 V 2 V	V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>pd</sub>	A or B	B or A		12.4		10		8.3	1.5	7.3	ns		
t <sub>en</sub>	ŌĒ	A or B		14.1		11.7		10.5	1.5	9.2	ns		
t <sub>dis</sub>	ŌĒ	A or B		13.6		9.9		9.5	1.7	8.8	ns		
t <sub>sk(o)</sub>				1		1		1		1.5	ns		

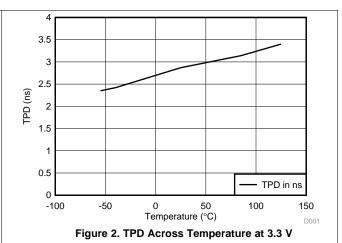
# 7.8 Operating Characteristics

 $T_A = 25^{\circ}C$ 

	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	UNIT	
Power dissipation capacitance		Outputs enabled	f = 10 MHz	43	43	48	nE	
Opd	per transceiver	Outputs disabled	I = IU MIHZ	1	1	4	pF	

# 7.9 Typical Characteristics

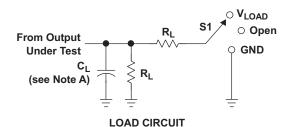




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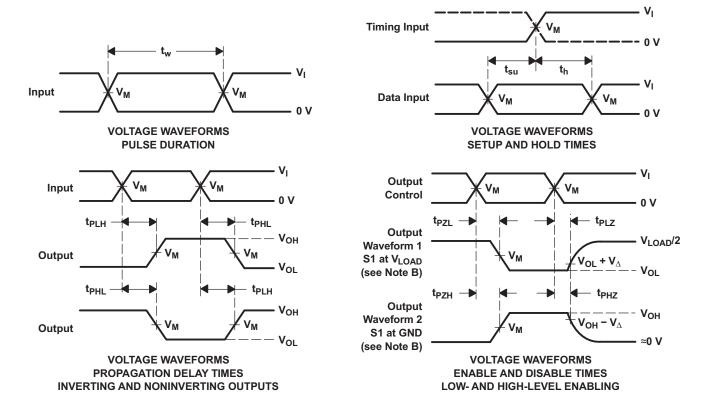


#### 8 Parameter Measurement Information



TEST	<b>S1</b>
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	$V_{LOAD}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

.,	INPUTS		.,	.,		-	.,
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	R <sub>L</sub>	$oldsymbol{V}_{\Delta}$
1.8 V ± 0.15 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	<b>500</b> Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



## 9 Detailed Description

#### 9.1 Overview

This octal bus transceiver is designed for 1.65-V to 3.6-V V<sub>CC</sub> operation.

The SN74LVCR2245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so the buses are effectively isolated.

All outputs, which are designed to sink up to 12 mA, include equivalent 26- $\Omega$  resistors to reduce overshoot and undershoot.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 9.2 Functional Block Diagram

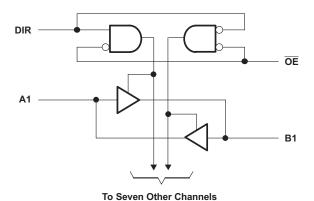


Figure 4. Logic Diagram (Positive Logic)

#### 9.3 Feature Description

- · Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- I<sub>off</sub> feature
  - Allows voltages on the inputs and outputs when V<sub>CC</sub> is 0 V

#### 9.4 Device Functional Modes

**Table 2. Function Table** 

INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	Χ	Isolation				



## 10 Application and Implementation

#### 10.1 Application Information

This 8-bit octal noninverting bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation. This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### 10.2 Typical Application

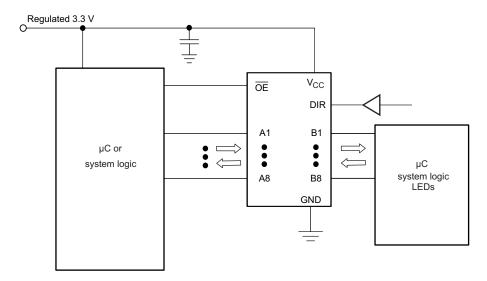


Figure 5. Typical Application Schematic

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

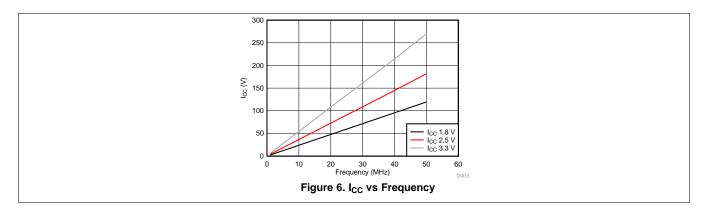
#### 10.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the Recommended Operating Conditions table.
  - For specified High and low levels, see V<sub>IH</sub> and V<sub>IL</sub> in the Recommended Operating Conditions table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V<sub>CC</sub>.
- 2. Recommend Output Conditions
  - Load currents should not exceed 50 mA per output and 100 mA total for the part.
  - Outputs should not be pulled above V<sub>CC</sub>.



## **Typical Application (continued)**

#### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Recommended Operating Conditions table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

#### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

#### 12.2 Layout Example

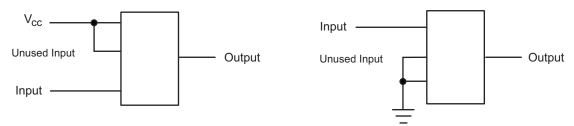


Figure 7. Layout Diagram



## 13 Device and Documentation Support

#### 13.1 Trademarks

All trademarks are the property of their respective owners.

#### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74LVCR2245ARGYRG4	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LER245A
74LVCR2245ARGYRG4.B	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LER245A
SN74LVCR2245ADBQR	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LVCR2245A
SN74LVCR2245ADBQR.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LVCR2245A
SN74LVCR2245ADBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245ADBR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245ADBRG4	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245ADBRG4.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245ADGVR	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245ADGVR.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245ADW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCR2245A
SN74LVCR2245ADW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCR2245A
SN74LVCR2245ADWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCR2245A
SN74LVCR2245ADWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCR2245A
SN74LVCR2245ANSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCR2245A
SN74LVCR2245ANSR.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCR2245A
SN74LVCR2245APW	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245APW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245APWE4	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245APWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245APWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245APWRE4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245APWT	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245APWT.B	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LER245A
SN74LVCR2245ARGYR	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LER245A
SN74LVCR2245ARGYR.B	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LER245A

<sup>(1)</sup> Status: For more details on status, see our product life cycle.



## PACKAGE OPTION ADDENDUM

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- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCR2245ARGYRG4	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74LVCR2245ADBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCR2245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCR2245ADBRG4	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCR2245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCR2245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVCR2245ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVCR2245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCR2245APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCR2245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1



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\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)		
74LVCR2245ARGYRG4	VQFN	RGY	20	3000	353.0	353.0	32.0		
SN74LVCR2245ADBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0		
SN74LVCR2245ADBR	SSOP	DB	20	2000	353.0	353.0	32.0		
SN74LVCR2245ADBRG4	SSOP	DB	20	2000	353.0	353.0	32.0		
SN74LVCR2245ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0		
SN74LVCR2245ADWR	SOIC	DW	20	2000	356.0	356.0	45.0		
SN74LVCR2245ANSR	SOP	NS	20	2000	356.0	356.0	45.0		
SN74LVCR2245APWR	TSSOP	PW	20	2000	353.0	353.0	32.0		
SN74LVCR2245APWT	TSSOP	PW	20	250	353.0	353.0	32.0		
SN74LVCR2245ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0		

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVCR2245ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVCR2245ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVCR2245APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVCR2245APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVCR2245APWE4	PW	TSSOP	20	70	530	10.2	3600	3.5





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DBQ (R-PDSO-G20)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AD.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## DGV (R-PDSO-G\*\*)

## 24 PINS SHOWN

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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