

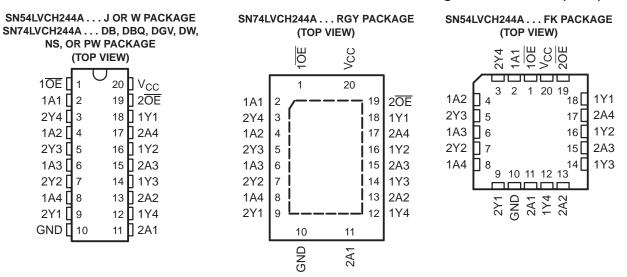
FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Signal Operation on All Ports

(5-V Input/Output Voltage With 3.3-V V_{CC})

 I_{off} Supports Partial-Power-Down Mode Operation

- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

The SN54LVCH244A octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVCH244A octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, these devices pass data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



ORDERING INFORMATION

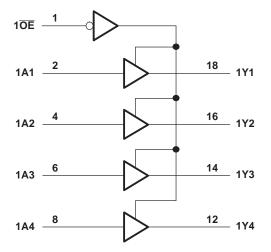
T _A	PACKAGE	(1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Reel of 1000	SN74LVCH244ARGYR	LCH244A
	SOIC - DW	Tube of 25	SN74LVCH244ADW	LVCH244A
	301C - DVV	Reel of 2000	SN74LVCH244ADWR	LVCH244A
	SOP - NS	Reel of 2000	SN74LVCH244ANSR	LVCH244A
–40°C to 85°C	SSOP – DB	Reel of 2000	SN74LVCH244ADBR	LCH244A
-40°C 10 65°C	SSOP (QSOP) – DBQ	Reel of 2500	SN74LVCH244ADBQR	LVCH244A
		Tube of 70	SN74LVCH244APW	
	TSSOP - PW	Reel of 2000	SN74LVCH244APWR	LCH244A
		Reel of 250	SN74LVCH244APWT	
	TVSOP - DGV	Reel of 2000	SN74LVCH244ADGVR	LCH244A
	CDIP – J	Tube of 20	SNJ54LVCH244AJ	SNJ54LVCH244AJ
–55°C to 125°C	CFP – W	Tube of 85	SNJ54LVCH244AW	SNJ54LVCH244AW
	LCCC – FK	Tube of 55	SNJ54LVCH244AFK	SNJ54LVCH244AFK

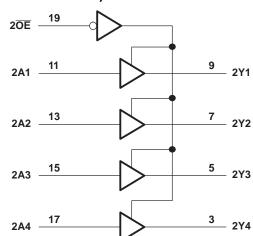
⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH BUFFER)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)





WITH 3-STATE OUTPUTS SCES009O-JULY 1995-REVISED FEBRUARY 2007



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CC}	Supply voltage range		-0.5	6.5	V	
VI	Input voltage range ⁽²⁾		-0.5	6.5	V	
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state ⁽²⁾	-0.5	6.5	V	
Vo	Voltage range applied to any output in the h	nigh or low state (2)(3)	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA	
I _{OK}	Output clamp current					
Io	Continuous output current			±50	mA	
	Continuous current through V _{CC} or GND			±100	mA	
		DB package ⁽⁴⁾		70		
		DBQ package ⁽⁴⁾		68		
		DGV package ⁽⁴⁾		92		
θ_{JA}	Package thermal impedance	DW package ⁽⁴⁾		58		
		NS package ⁽⁴⁾		60		
		PW package ⁽⁴⁾		83		
		RGY package ⁽⁵⁾		37		
T _{stg}	Storage temperature range		-65	150	°C	

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

The value of V_{CC} is provided in the recommended operating conditions table.

The package thermal impedance is calculated in accordance with JESD 51-7.

⁽⁵⁾ The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LVCH244A, SN74LVCH244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS





Recommended Operating Conditions⁽¹⁾

			SN54LVCI	1244A	SN74LV	CH244A	LINUT	
			MIN	MAX	MIN	MAX	UNIT	
V	Cumply voltage	Operating	2	3.6	1.65	3.6	V	
V_{CC}	Supply voltage	Data retention only	1.5		1.5		V	
		V _{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		2			
		V _{CC} = 1.65 V to 1.95 V				$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$				0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		0.8		
V_{I}	Input voltage		0	5.5	0	5.5	V	
V (Output voltage	High or low state	0	V_{CC}	0	V _{CC}	- v	
Vo	Output voltage	3-state	0	5.5	0	5.5		
		V _{CC} = 1.65 V				-4		
	High-level output current	$V_{CC} = 2.3 \text{ V}$				-8	1	
I _{OH}	riigii-ievei output current	$V_{CC} = 2.7 \text{ V}$		-12		-12	mA	
		V _{CC} = 3 V		-24		-24		
		V _{CC} = 1.65 V				4		
1	Low-level output current	$V_{CC} = 2.3 \text{ V}$				8	mA	
I _{OL}	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12		12	ША	
		V _{CC} = 3 V		24		24	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	<u>-</u>		10		10	ns/V	
T_A	Operating free-air temperature		– 55	125	-40	85	°C	

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



TRUMENTS www.ti.com SCES009O-JULY 1995-REVISED FEBRUARY 2007

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	SN54L	VCH244	Α	SN74L	VCH244	Α	UNIT	
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	UNII	
	1001	1.65 V to 3.6 V				V _{CC} - 0.2			-	
	$I_{OH} = -100 \mu A$	2.7 V to 3.6 V	V _{CC} - 0.2							
	$I_{OH} = -4 \text{ mA}$	1.65 V				1.2				
V_{OH}	$I_{OH} = -8 \text{ mA}$	2.3 V				1.7			V	
	I - 12 mA	2.7 V	2.2			2.2				
	$I_{OH} = -12 \text{ mA}$	3 V	2.4			2.4				
	$I_{OH} = -24 \text{ mA}$	3 V	2.2			2.2				
	I _{OL} = 100 μA	1.65 V to 3.6 V						0.2		
	I _{OL} = 100 μA	2.7 V to 3.6 V			0.2					
V	I _{OL} = 4 mA	1.65 V						0.45	V	
V_{OL}	I _{OL} = 8 mA	2.3 V						0.7	V	
	I _{OL} = 12 mA	2.7 V			0.4			0.4		
	I _{OL} = 24 mA	3 V			0.55			0.55		
I _I	V _I = 0 to 5.5 V	3.6 V			±5			±5	μΑ	
I _{off}	V_I or $V_O = 5.5 \text{ V}$	0						±10	μΑ	
	V _I = 0.58 V	1.65 V				(2)				
	V _I = 1.07 V					(2)				
	V _I = 0.7 V	2.3 V				45				
I _{I(hold)}	V _I = 1.7 V	2.3 V				-45			μΑ	
	V _I = 0.8 V	3 V	75			75				
	V _I = 2 V	3 V	-75			-75				
	$V_1 = 0$ to 3.6 $V^{(3)}$	36 V			±500			±500		
l _{OZ}	V _O = 0 to 5.5 V	3.6 V			±15			±10	μΑ	
	$V_I = V_{CC}$ or GND	3.6 V			10			10		
I _{CC}	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(4)}$ $I_{\text{O}} = 0$	3.0 V			10			10	μΑ	
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500			500	μА	
C _i	$V_{I} = V_{CC}$ or GND	3.3 V		4	12		4		pF	
Co	V _O = V _{CC} or GND	3.3 V		5.5	12		5.5		pF	

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. This information was not available at the time of publication.

 ⁽³⁾ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
 (4) This applies in the disabled state only.

SN54LVCH244A, SN74LVCH244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54L\			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.7 \text{ V}$ $V_{CC} = \pm 0.$		3.3 V 3 V	UNIT
			MIN MAX	MIN	MAX	
t _{pd}	A	Y	7.5	1	6.5	ns
t _{en}	ŌĒ	Y	9	1	8	ns
t _{dis}	ŌĒ	Y	8	1	7	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN74LVCH244A							
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V_{CC} = 3.3 V \pm 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Y	(1)	(1)	(1)	(1)		6.9	1.5	5.9	ns
t _{en}	ŌĒ	Y	(1)	(1)	(1)	(1)		8.6	1	7.6	ns
t _{dis}	ŌĒ	Y	(1)	(1)	(1)	(1)		6.8	1.5	5.8	ns

⁽¹⁾ This information was not available at the time of publication.

Operating Characteristics

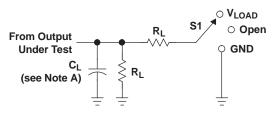
 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
C	Power dissipation capacitance	Outputs enabled	f = 10 MHz	(1)	(1)	47	ρF
Cpd	per buffer/driver	Outputs disabled		(1)	(1)	2	рг

⁽¹⁾ This information was not available at the time of publication.



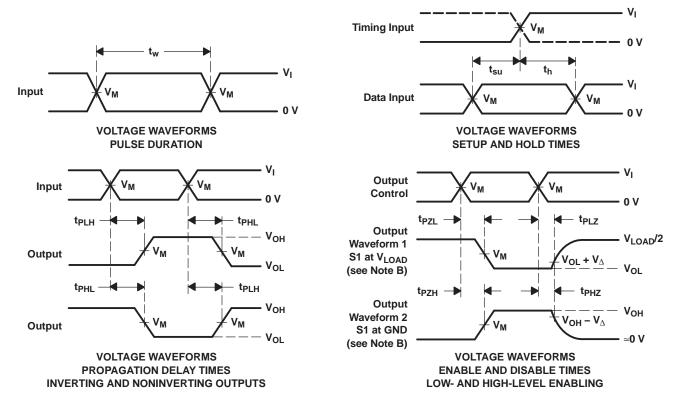
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V	INPUTS		.,	V			V
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD} C _L		R _L	$V_{\!\scriptscriptstyle \Delta}$
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9754201Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9754201Q2A SNJ54LVCH 244AFK
5962-9754201QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754201QR A SNJ54LVCH244AJ
5962-9754201QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754201QS A SNJ54LVCH244AW
5962-9754201V2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9754201V2A SNV54LVCH 244AFK
5962-9754201VSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754201VS A SNV54LVCH244AW
SN74LVCH244ADBQR	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCH244A
SN74LVCH244ADBQR.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCH244A
SN74LVCH244ADBQRG4	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCH244A
SN74LVCH244ADBQRG4.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCH244A
SN74LVCH244ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244ADBR.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244ADGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244ADGVR.B	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244ADGVRG4	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244ADGVRG4.B	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A
SN74LVCH244ADW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A
SN74LVCH244ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A
SN74LVCH244ADWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A
SN74LVCH244ADWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVCH244ADWRG4.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A
SN74LVCH244ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A
SN74LVCH244ANSR.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A
SN74LVCH244APW	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244APW.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244APWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244APWT	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244APWT.B	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A
SN74LVCH244ARGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LCH244A
SN74LVCH244ARGYR.B	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LCH244A
SNJ54LVCH244AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9754201Q2A SNJ54LVCH 244AFK
SNJ54LVCH244AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754201QR A SNJ54LVCH244AJ
SNJ54LVCH244AW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754201QS A SNJ54LVCH244AW

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVCH244A, SN54LVCH244A-SP, SN74LVCH244A:

Catalog: SN74LVCH244A, SN54LVCH244A

Military: SN54LVCH244A

Space: SN54LVCH244A-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH244ADBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCH244ADBQRG4	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCH244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCH244ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH244ADGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVCH244ADWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVCH244ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVCH244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCH244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCH244ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1



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*All dimensions are nominal

All difficultions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH244ADBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0
SN74LVCH244ADBQRG4	SSOP	DBQ	20	2500	353.0	353.0	32.0
SN74LVCH244ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVCH244ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVCH244ADGVRG4	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVCH244ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVCH244ADWRG4	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVCH244ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVCH244APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVCH244APWT	TSSOP	PW	20	250	353.0	353.0	32.0
SN74LVCH244ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

All difficultions are norminal								
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9754201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9754201V2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9754201VSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LVCH244ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVCH244ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVCH244APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVCH244APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54LVCH244AFK	FK	LCCC	20	55	506.98	12.06	2030	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AD.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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