







SN74LVCC3245A SCAS585Q - NOVEMBER 1996 - REVISED DECEMBER 2022

SN74LVCC3245A Octal Bus Transceiver With Adjustable Output Voltage and 3-State Outputs

1 Features

- Bidirectional voltage translator
- 2.3 V to 3.6 V on A port and 3 V to 5.5 V on B port
- Control inputs V_{IH} and V_{IL} levels are referenced to V_{CCA} voltage
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22
 - 2000-V Human Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Level translation
- USB
- Interfacing
- Analog and digital applications

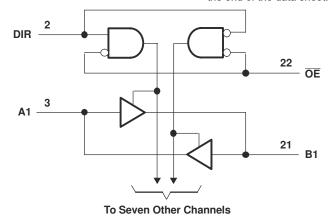
3 Description

SN74LVCC3245A device is noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB}, which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA}, which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

Package Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------|----------------|--------------------|
| | DB (SSOP, 24) | 8.65 mm × 3.90 mm |
| | DW (SOIC, 24) | 15.40 mm × 7.50 mm |
| SN74LVCC3245A | DBQ (SSOP, 24) | 8.20 mm × 5.30 mm |
| | NS (SO, 24) | 15.00 mm × 5.30 mm |
| | PW (TSSOP, 24) | 7.80 mm × 4.40 mm |

For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



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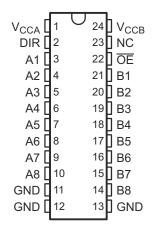
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| С | hanges from Revision P (December 2015) to Revision Q (December 2022) | Page |
|---|--|-----------------------|
| • | Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • | Added thermal information for DB and PW package | |
| | Added inclusive terminology | |
| С | hanges from Revision O (March 2005) to Revision P (December 2015) | Page |
| • | Added Applications section, Device Information table, ESD Ratings table, Feature Description section Functional Modes, Application and Implementation section, Power Supply Recommendations section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Infosection. | i, Layout ormation |
| • | Removed <i>Ordering Information</i> table | |



5 Pin Configuration and Functions



NC – No internal connection See Section 12 for dimensions.

Figure 5-1. DB, DBQ, DW, NS, or PW Package, 24-Pin SSOP, SOIC, SO, or TSSOP (Top View)

Table 5-1. Pin Functions

| P | PIN | TYPE(1) | DESCRIPTION |
|------------------|-----|---------|--------------------------|
| NAME | NO. | ITPE | DESCRIPTION |
| A1 | 3 | I/O | A1 port |
| A2 | 4 | I/O | A2 port |
| A3 | 5 | I/O | A3 port |
| A4 | 6 | I/O | A4 port |
| A5 | 7 | I/O | A5 port |
| A6 | 8 | I/O | A6 port |
| A7 | 9 | I/O | A7 port |
| A8 | 10 | I/O | A8 port |
| B1 | 21 | I/O | B1 port |
| B2 | 20 | I/O | B2 port |
| B3 | 19 | I/O | B3 port |
| B4 | 18 | I/O | B4 port |
| B5 | 17 | I/O | B5 port |
| B6 | 16 | I/O | B6 port |
| B7 | 15 | I/O | B7 port |
| B8 | 14 | I/O | B8 port |
| DIR | 2 | I | Dir input |
| | 11 | | |
| GND | 12 | _ | Ground |
| | 13 | | |
| NC | 23 | _ | Unconnected |
| ŌĒ | 22 | I | Output Enable active low |
| V _{CCA} | 1 | _ | A port power |
| V _{CCB} | 24 | _ | B port power |

(1) I = input, O = output, P = power



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|--------------------------------------|---|---------------------------------|------|------------------------|-----------|
| V _{CCA} V _{CCB} | Supply voltage | | -0.5 | 6 | V |
| | | All A ports ⁽²⁾ | -0.5 | V _{CCA} + 0.5 | |
| VI | Input voltage | All B ports ⁽³⁾ | -0.5 | V _{CCB} + 0.5 | \ \ \ \ \ |
| | | Except I/O ports ⁽²⁾ | -0.5 | V _{CCA} + 0.5 | |
| \/ | Output voltage ⁽³⁾ | All A ports | -0.5 | V _{CCA} + 0.5 | V |
| V _O | Output voltage(**) | All B ports | -0.5 | V _{CCB} + 0.5 |] |
| I _{IK} | Input clamp current | V _I < 0 | | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | | -50 | mA |
| Io | Continuous output current | | | ±50 | mA |
| | Continuous current through V _{CCA} , V _{CCB} , or | GND | | ±100 | mA |
| TJ | Junction temperature | | | 150 | °C |
| _ | lungtion to analyze the annual registers. | DW | | 46 | °C/\\ |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | NS | | 65 | °C/W |
| T _{stg} | Storage temperature | 1 | -65 | 150 | °C |

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | | VALUE | UNIT |
|----------------------------|---|-------|--|-------|------|
| \/ Flactractatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | \/ | | |
| Ľ | V _(FOD) Electrostatic discharge | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 | |

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

| | | V _{CCA} | V _{CCB} | MIN | NOM | MAX | UNIT |
|------------------|---|------------------|------------------|------|-----|-----|------|
| V _{CCA} | Supply voltage | | | 2.3 | 3.3 | 3.6 | V |
| V _{CCB} | Supply voltage | | | 3 | 5 | 5.5 | V |
| ., | | 2.3 V | 3 V | 1.7 | | | |
| | V _{IHA} High-level input voltage | 2.7 V | 3 V | 2 | | | V |
| VIHA | | 3 V | 3.6 V | 2 | | | |
| | | 3.6 V | 5.5 V | 2 | | | |
| | | 2.3 V | 3 V | 2 | | | |
| | High-level input voltage | 2.7 V | 3 V | 2 | | | v |
| V _{IHB} | | 3 V | 3.6 V | 2 | | | v |
| | | 3.6 V | 5.5 V | 3.85 | | | |

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⁽²⁾ This value is limited to 4.6 V maximum.

⁽³⁾ This value is limited to 6 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.3 Recommended Operating Conditions (continued)

| | | V _{CCA} | V _{CCB} | MIN | NOM | MAX | UNIT |
|--|--|------------------|------------------|-----------------|--------------|------------------|------|
| | | 2.3 V | 3 V | | | 0.7 | |
| V | Low level input veltage | 2.7 V | 3 V | | | 0.8 | V |
| VILA | Low-level input voltage | 3 V | 3.6 V | | | 0.8 | V |
| VILA Low-level input voltage 2.3 V 3V 3V 3.6 V 3.0 | 5.5 V | | , | 0.8 | | | |
| VILB Low-level (reference villa linput void villa linput void void void Output void void void void void void void void | | 2.3 V | 3 V | | | 0.8 | |
| ., | Long land bound on the ma | 2.7 V | 3 V | | | 0.8 | ., |
| V _{ILB} | Low-level input voltage | 3 V | 3.6 V | | | 0.8 | V |
| | | 3.6 V | 5.5 V | | | 1.65 | |
| | | 2.3 V | 3 V | 1.7 | , | | |
| ., | High-level input voltage (control terminals) | 2.7 V | 3 V | 2 | | | ., |
| V _{IH} | | 3 V | 3.6 V | 2 | | | V |
| | | 3.6 V | 5.5 V | 2 | | | |
| | | 2.3 V | 3 V | | | 0.7 | |
| | Low-level input voltage (control terminals) | 2.7 V | 3 V | | | 0.8 | |
| V_{IL} | | | 3.6 V | | | 0.8 | V |
| | | 3.6 V | 5.5 V | | , | 0.8 | |
| V _{IA} | Input voltage | | | 0 | | V _{CCA} | V |
| | | | | 0 | | V _{CCB} | V |
| | | | | 0 | | V _{CCA} | V |
| | | | | 0 | | V _{CCB} | V |
| | | 2.3 V | 3 V | | , | -8 | |
| | | 2.7 V | 3 V | | | -12 | |
| I _{OHA} | High-level output current | 3 V | 3 V | | | -24 | mA |
| | | 2.7 V | 4.5 V | | | -24 | |
| | | 2.3 V | 3 V | | | -12 | |
| | | 2.7 V | 3 V | | , | -12 | |
| I _{OHB} | High-level output current | 3 V | 3 V | | | -24 | mA |
| VIL VIA VIB VOA VOB | | 2.7 V | 4.5 V | | | -24 | |
| | | 2.3 V | 3 V | | | 8 | |
| | | 2.7 V | 3 V | | | 12 | |
| I _{OLA} | Low-level output current | 3 V | 3 V | | | 24 | mA |
| | | 2.7 V | 4.5 V | | | 24 | |
| | | 2.3 V | 3 V | | | 12 | |
| | | 2.7 V | 3 V | | , | 12 | |
| I _{OLB} | Low-level output current | 3 V | 3 V | | | 24 | mA |
| | | 2.7 V | 4.5 V | | | 24 | 4 |
| Δt/Δν | Input transition rise or fall rate | | | | | 10 | ns/V |
| T _A | Operating free-air temperature | | | -4 0 | | 85 | °C |



6.4 Thermal Information

| | THERMAL METRIC ^{(1) (4)} | | DBQ (SSOP) | PW (TSSOP) | UNIT |
|-----------------------|--|---------|------------|------------|------|
| | | 24 PINS | 24 PINS | 24 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 90.7 | 61 | 100.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 51.9 | 44.8 | 44.7 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 49.7 | 34.5 | 55.8 | °C/W |
| ΨЈТ | Junction-to-top characterization parameter | 18.8 | 9.5 | 6.8 | °C/W |
| ΨЈВ | Junction-to-board characterization parameter | 49.3 | 37.2 | 55.4 | °C/W |

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| P | ARAMETER | TEST CONDITIONS | V _{CCA} | V _{CCB} | MIN | TYP | MAX | UNIT | |
|---------------------|--------------------------|---|-----------------------|------------------|-----|------|-----|------|--|
| | | I _{OH} = -100 μA | 3 V | 3 V | 2.9 | 3 | | | |
| | | I _{OH} = -8 mA | 2.3 V | 3 V | 2 | | | | |
| Volla | I _{OH} = -12 mA | 2.7 V | 3 V | 2.2 | 2.5 | | V | | |
| VOHA | | 10H12 IIIA | 3 V | 3 V | 2.4 | 2.8 | | V | |
| | | - 24 mA | 3 V | 3 V | 2.2 | 2.6 | | | |
| | | I _{OH} = –24 mA | 2.7 V | 4.5 V | 2 | 2.3 | | | |
| | | I _{OH} = -100 μA | 3 V | 3 V | 2.9 | 3 | | | |
| | | L = 12 mA | 2.3 V | 3 V | 2.4 | | | | |
| V _{OHB} | I _{OH} = –12 mA | | 3 V | 2.4 | 2.8 | | V | | |
| | | L = 24 mA | 3 V | 3 V | 2.2 | 2.6 | | | |
| | | I _{OH} = –24 mA | 2.7 V | 4.5 V | 3.2 | 4.2 | | | |
| | | I _{OL} = 100 μA | 3 V | 3 V | | | 0.1 | | |
| | | I _{OL} = 8 mA | 2.3 V | 3 V | | | 0.6 | | |
| V _{OLA} | | I _{OL} = 12 mA | 2.7 V | 3 V | | 0.1 | 0.5 | V | |
| | | I _{OL} = 24 mA | | 3 V | | 0.2 | 0.5 | | |
| | | | | 4.5 V | | 0.2 | 0.5 | | |
| | | I _{OL} = 100 μA | 3 V | 3 V | | | 0.1 | | |
| ., | | I _{OL} = 12 mA | 2.3 V | 3 V | | | 0.4 | | |
| V _{OLB} | - 24 mA | 3 V | 3 V | | 0.2 | 0.5 | V | | |
| | | I _{OL} = 24 mA | 2.7 V | 4.5 V | | 0.2 | 0.5 | | |
| | O and a big mand a | V V STONE | 0.01/ | 3.6 V | | ±0.1 | ±1 | | |
| 11 | Control inputs | $V_I = V_{CCA}$ or GND | 3.6 V | 5.5 V | | ±0.1 | ±1 | μA | |
| I _{OZ} (1) | A or B ports | $V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or V_I | 1 _{IH} 3.6 V | 3.6 V | | ±0.5 | ±5 | μA | |
| | | A port = V_{CCA} or GND, $I_O = 0$ | 3.6 V | Open | | 5 | 50 | | |
| I _{CCA} | B to A | Drawt - W ar CND I c | 0.01/ | 3.6 V | | 5 | 50 | μΑ | |
| | | B port = V_{CCB} or GND, $I_O = 0$ | 3.6 V | 5.5 V | | 5 | 50 | | |
| | A 4 - B | A most V as OND 1 2 | 221 | 3.6 V | | 5 | 50 | | |
| I _{CCB} | A to B | A port = V_{CCA} or GND, $I_O = 0$ | 3.6 V | 5.5 V | | 8 | 80 | μA | |

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6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PAR | AMETER | TEST CONDITIONS | V _{CCA} | V _{CCB} | MIN | TYP | MAX | UNIT |
|----------------------------------|----------------|---|------------------|------------------|-----|------|-----|------|
| ΔI _{CCA} ⁽²⁾ | A port | V_{I} = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, \overline{OE} at GND and DIR at V_{CCA} | 3.6 V | 3.6 V | | 0.35 | 0.5 | |
| | ŌĒ | V_{I} = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA} | 3.6 V | 3.6 V | | 0.35 | 0.5 | mA |
| | DIR | V_{I} = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, \overline{OE} at GND | 3.6 V | 3.6 V | | 0.35 | 0.5 | |
| ΔI _{CCB} (2) | B port | $V_{I} = V_{CCB} - 2.1 \text{ V}$, Other inputs at V_{CCB} or GND, \overline{OE} at GND and DIR at GND | 3.6 V | 5.5 V | | 1 | 1.5 | mA |
| C _i | Control inputs | V _I = V _{CCA} or GND | Open | Open | | 4 | | pF |
| C _{io} | A or B ports | V _O = V _{CCA/B} or GND | 3.3 V | 5 V | | 18.5 | | pF |

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 through Figure 7-4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CCA,} V _{CCB} | MIN | MAX | UNIT | |
|------------------|----------------------------|---|--|---|------|------|----|
| | | | $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1 | 9.4 | | |
| t _{PHL} | A B V _{CCA} = 2.7 | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 6 | ns | | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 7.1 | | |
| | | | $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 $ | 1 | 9.1 | | |
| t _{PLH} | А | В | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 5.3 | ns | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 7.2 | | |
| | | | $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1 | 11.2 | | |
| t _{PHL} | В | В | Α | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 5.8 | ns |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 6.4 | | |
| | | | $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1 | 9.9 | | |
| t _{PLH} | В А | Α | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 7 | ns | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 7.6 | | |
| | ŌĒ | | $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1 | 14.5 | | |
| t _{PZL} | | Α | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 9.2 | ns | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 9.7 | | |

For I/O ports, the parameter I_{OZ} includes the input leakage current. This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC} .



6.6 Switching Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 through Figure 7-4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | | | | | V _{CCA,} V _{CCB} MIN | | | | MAX | UNIT |
|---------------------|-----------------|---|---|-----|------|----|--|--|--|--|-----|------|
| t _{PZH} ŌĒ | | | V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 | 1 | 12.9 | | | | | | | |
| | ŌĒ | А | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 9.5 | ns | | | | | | |
| | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 9.5 | | | | | | | | |
| | | | V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 | 1 | 13 | | | | | | | |
| t _{PZL} | ŌĒ | В | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V | 1 | 8.1 | ns | | | | | | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 9.2 | | | | | | | |
| t _{PZH} OE | | | V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 | 1 | 12.8 | | | | | | | |
| | ŌĒ | В | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 8.4 | ns | | | | | | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 9.9 | | | | | | | |
| | | | V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 | 1 | 7.1 | ns | | | | | | |
| t _{PLZ} | ŌĒ | A | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 7 | | | | | | | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 6.6 | | | | | | | |
| | | | V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 | 1 | 7.3 | _ | | | | | | |
| t _{PHZ} | ŌĒ | А | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V | 1 | 7.8 | | | | | | | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 6.9 | | | | | | | |
| | | | V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 | 1 | 8.8 | | | | | | | |
| t _{PLZ} | ŌĒ | В | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V | 1 | 7.3 | ns | | | | | | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | | | | | | | | | |
| | | | V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 | 1 | 8.9 | | | | | | | |
| t _{PHZ} | ŌĒ | В | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 | 1 | 7 | ns | | | | | | |
| | | | V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V | 1 | 7.9 | | | | | | | |

6.7 Operating Characteristics

 $V_{CCA} = 3.3 \text{ V}, V_{CCB} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

| JOA | PARAMETER | TEST CO | NDITIONS | TYP | UNIT |
|---|------------------|-------------------|------------|-----|------|
| C _{pd} Power dissipation capacitance per transceiver | Outputs enabled | 0 - 50 f - 40 MH- | | 38 | "F |
| | Outputs disabled | $C_L = 50,$ | f = 10 MHz | 4.5 | p⊦ |



6.8 Typical Characteristics

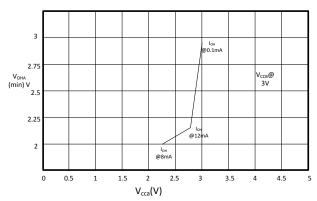
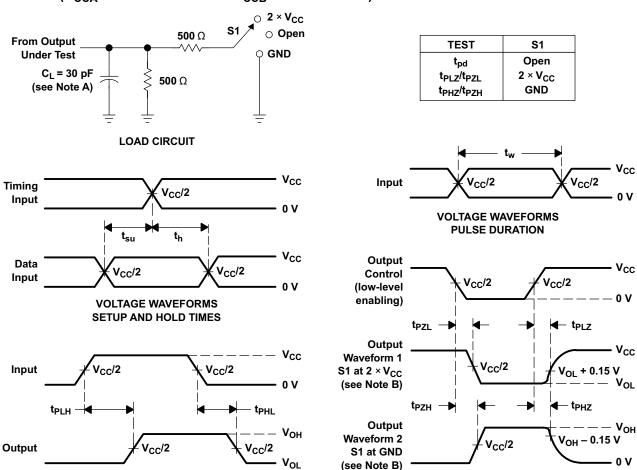


Figure 6-1. $V_{OHA(min)}$ VS V_{CCA}



7 Parameter Measurement Information

7.1 A Port (V_{CCA} = 2.5 V ± 0.2 V and V_{CCB} = 3.3 V ± 0.3 V)



- A. C₁ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH}are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

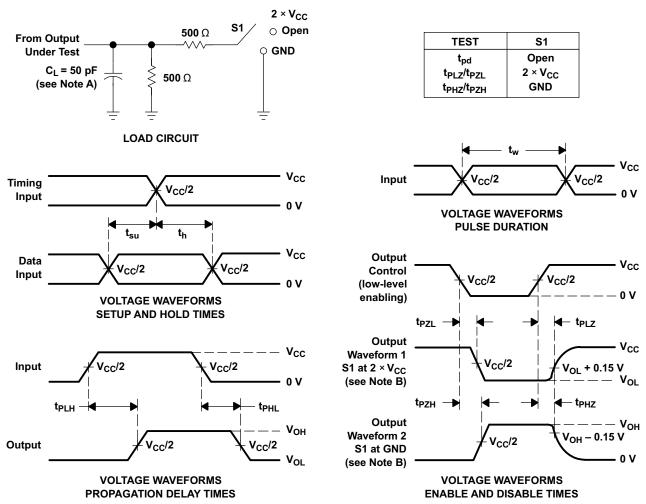
Figure 7-1. Load Circuit and Voltage Waveforms

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES



7.2 B Port (V_{CCA} = 2.5 V ± 0.2 V and V_{CCB} = 3.3 V ± 0.3 V)

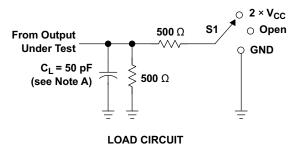


- C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_r ≤ 2 ns
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

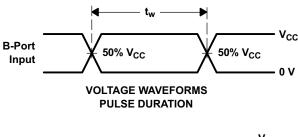
Figure 7-2. Load Circuit and Voltage Waveforms

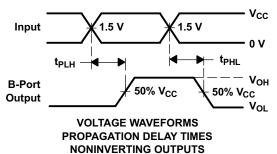


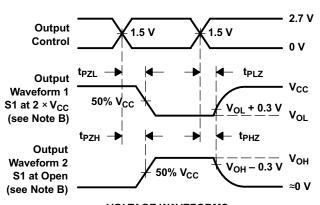
7.3 B Port (V_{CCA} = 3.6 V and V_{CCB} = 5.5 V)



| TEST | S1 |
|------------------------------------|---------------------|
| t _{PLH} /t _{PHL} | Open |
| t _{PLZ} /t _{PZL} | 2 × V _{CC} |
| t _{PHZ} /t _{PZH} | Open |







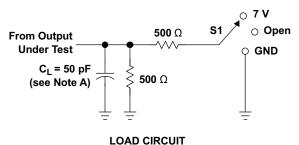
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- 3. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

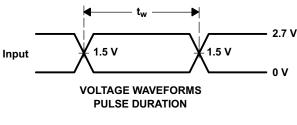
Figure 7-3. Load Circuit and Voltage Waveforms

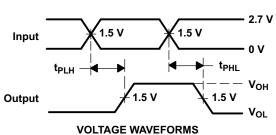


7.4 A and B Port (V_{CCA} and $V_{CCB} = 3.6 \text{ V}$)

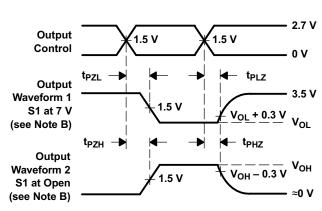


| TEST | S1 |
|------------------------------------|------|
| t _{PLH} /t _{PHL} | Open |
| t _{PLZ} /t _{PZL} | 7 V |
| t _{PHZ} /t _{PZH} | Open |





PROPAGATION DELAY TIMES NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

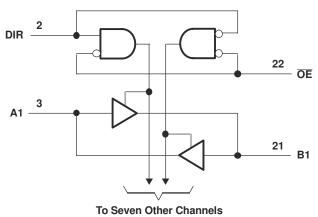
Figure 7-4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVCC3245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, \overline{OE}) is powered by V_{CCA} .

8.2 Functional Block Diagram



8.3 Feature Description

This device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port. The control inputs recommended operating specifications are referenced with respect to V_{CCA} Voltage.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74LVCC3245A.

Table 8-1. Function Table (Each Transceiver)

| INP | UTS | OPERATION |
|-----|-----|-----------------|
| ŌĒ | DIR | OFERATION |
| L | L | B data to A bus |
| L | Н | A data to B bus |
| Н | X | Isolation |

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVCC3245A device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port and designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

9.2 Typical Application

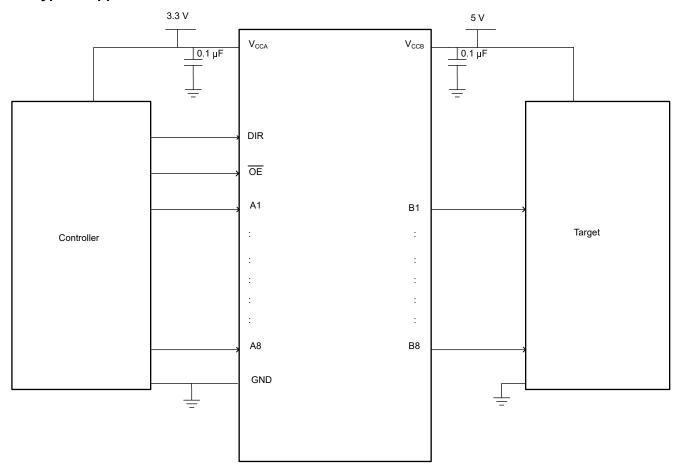


Figure 9-1. Typical Application

9.2.1 Design Requirements

This device can be used as bidirectional level translator depending on the DIR pin. The application describes the level translation of controller with signals at 3.3 V to target operating at 5 V. The \overline{OE} pin is low and DIR pin is 3.3-V high.

9.2.2 Detailed Design Procedure

Use the procedure that follows for the design:

- 1. Recommended Input Conditions
 - Rise time and fall time specs. See (Δt/ΔV) in the Recommended Operating Conditions table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating
 Conditions table at any valid V_{CC}.
- 2. Absolute Maximum Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table.
 - All the voltages on A and B ports should not exceed above V_{CCA} or V_{CCB} to prevent the biasing of Electrostatic discharge (ESD) diodes.

9.2.3 Application Curve

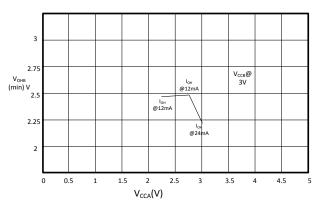


Figure 9-2. V_{OHB(min)} vs V_{CCA}

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} pins then 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.



10 Layout

10.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

10.2 Layout Example



Figure 10-1. Layout Example

10.3 Power-Up Considerations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. To guard against such power-up problems, take these precautions:

- 1. Connect ground before any supply voltage is applied.
- 2. Power up the control side of the device (V_{CCA} for all four of these devices).
- 3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
- 4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

For more information, refer to Voltage-Level-Translation Devices application note.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Implications of Slow or Floating CMOS Inputs
- Texas Instruments, Voltage-Level-Translation Devices

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossarv

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|-----------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|------------------|
| SN74LVCC3245ADBQR | Active | Production | SSOP (DBQ) 24 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADBQR.B | Active | Production | SSOP (DBQ) 24 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADBR | Active | Production | SSOP (DB) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245ADBR.A | Active | Production | SSOP (DB) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245ADBR.B | Active | Production | SSOP (DB) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245ADBRE4 | Active | Production | SSOP (DB) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245ADBRG4 | Active | Production | SSOP (DB) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245ADW | Active | Production | SOIC (DW) 24 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADW.B | Active | Production | SOIC (DW) 24 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADWE4 | Active | Production | SOIC (DW) 24 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADWG4 | Active | Production | SOIC (DW) 24 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADWR | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADWR.B | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADWRG4 | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ADWRG4.B | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ANSR | Active | Production | SOP (NS) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245ANSR.B | Active | Production | SOP (NS) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCC3245A |
| SN74LVCC3245APW | Active | Production | TSSOP (PW) 24 | 60 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APW.B | Active | Production | TSSOP (PW) 24 | 60 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APWR | Active | Production | TSSOP (PW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APWR.A | Active | Production | TSSOP (PW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APWRE4 | Active | Production | TSSOP (PW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APWRG4 | Active | Production | TSSOP (PW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APWT | Active | Production | TSSOP (PW) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APWT.B | Active | Production | TSSOP (PW) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |
| SN74LVCC3245APWTG4 | Active | Production | TSSOP (PW) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH245A |

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVCC3245A:

Enhanced Product: SN74LVCC3245A-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74LVCC3245ADBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVCC3245ADBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVCC3245ADWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVCC3245ADWRG4 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVCC3245ANSR | SOP | NS | 24 | 2000 | 330.0 | 24.4 | 8.3 | 15.4 | 2.6 | 12.0 | 24.0 | Q1 |
| SN74LVCC3245APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVCC3245APWT | TSSOP | PW | 24 | 250 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |



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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVCC3245ADBQR | SSOP | DBQ | 24 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LVCC3245ADBR | SSOP | DB | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVCC3245ADWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74LVCC3245ADWRG4 | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74LVCC3245ANSR | SOP | NS | 24 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVCC3245APWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVCC3245APWT | TSSOP | PW | 24 | 250 | 353.0 | 353.0 | 32.0 |

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVCC3245ADW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LVCC3245ADW.B | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LVCC3245ADWE4 | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LVCC3245ADWG4 | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LVCC3245APW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVCC3245APW.B | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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