

SNx4LVC74A Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear and Preset

1 Features

- Operate from 1.65V to 3.6V
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 5.2ns at 3.3V
- Typical V_{OLP} (output ground bounce) <0.8V at $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) >2V at V_{CC} = 3.3V, T_A = 25°C
- Latch-up performance exceeds 250mA per JESD
- ESD protection exceeds JESD 22
 - 2000V human-body model (A114-A)
 - 1000V charged-device model (C101)

2 Applications

- Servers
- Medical, Healthcare, and Fitness
- Telecom Infrastructures
- TVs, Set-Top Boxes, and Audio
- Test and Measurement
- **Industrial Transport**
- Wireless Infrastructure
- **Enterprise Switching**
- **Motor Drives**
- **Factory Automation and Control**

3 Description

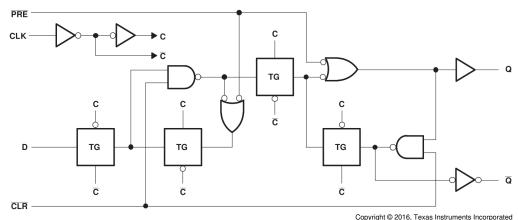
The SNx4LVC74A devices integrate two positive-edge triggered D-type flip-flops in one convenient device.

The SN54LVC74A is designed for 2.7V to 3.6V V_{CC} operation, and the SN74LVC74A is designed for 1.65V to 3.6V V_{CC} operation.

Device Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)	BODY SIZE(3)
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm x 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm x 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm x 7.8mm	10.20mm × 5.30mm
SNx4LVC74A	PW (TSSOP, 14)	5mm x 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm	3.50mm × 3.50mm
	J (CDIP, 14)	19.55mm x 7.9mm	19.56 mm × 6.67 mm
	W (CFP, 14)	9.21mm x 9 mm	9.21 mm × 5.97 mm
	FK (LCCC, 20)	8.9mm x 8.9mm	8.89 mm × 8.89 mm

- For more information, see Mechanical, Packaging, and Orderable Information.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Flip-Flop (Positive Logic)



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4 Pin Configuration and Functions

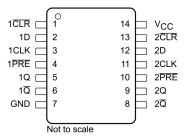


Figure 4-1. D, DB, J, PW, NS, or W Package 14-Pin SOIC, SSOP, CDIP, TSSOP, SO, or CFP (Top View)

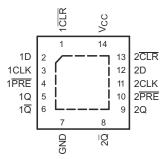


Figure 4-2. BQA or RGY Package 14-Pin WQFN or **VQFN With Exposed Thermal Pad (Top View)**

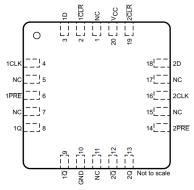


Figure 4-3. FK Package 20-Pin LCCC (Top View)

Table 4-1. Pin Functions

PIN				
NAME	CDIP, CFP, PDIP, SO, SOIC, SSOP, TSSOP, VQFN	LCCC	I/O	DESCRIPTION
1CLK	3	4	I	Channel 1 clock input
1 CLR	1	2	I	Channel 1 clear input. Pull low to set Q output low.
1D	2	3	I	Channel 1 data input
1 PRE	4	6	I	Channel 1 preset input. Pull low to set Q output high.
1Q	5	8	0	Channel 1 output
1 Q	6	9	0	Channel 1 inverted output
2CLK	11	16	I	Channel 2 clock input
2 CLR	13	19	I	Channel 2 clear input. Pull low to set Q output low.
2D	12	18	I	Channel 2 data input
2 PRE	10	14	I	Channel 2 preset input. Pull low to set Q output high.
2Q	9	13	0	Channel 2 output
2 Q	8	12	0	Channel 2 Inverted output
GND	7	10	_	Ground
NC	_	1, 5, 7, 11, 15, 17	_	No connect
V _{CC}	14	20	_	Supply



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V _{CC}		-0.5	6.5	V	
Input voltage, V _I ⁽²⁾			-0.5	6.5	V
Output voltage, V _O ^{(2) (3)}		-0.5	V _{CC} + 0.5	V	
Input clamp current, I _{IK}	V _I < 0			-50	mA
Output clamp current, I _{OK}	V _O < 0			-50	mA
Continuous output current, I _O	·			±50	mA
Continuous current through V _{CC} or GND				±100	mA
Storage temperature, T _{stg}			-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in *Recommended Operating Conditions* .

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	\/	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	\ \ \ \ \ \

- 1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

see(1)

				MIN	MAX	UNIT
		Operating	SN54LVC74A	2	3.6	
V_{CC}	Supply voltage	Operating	SN74LVC74A	1.65	3.6	V
		Data retention only		1.5		
		V _{CC} = 1.65 V to 1.95 V	SN74LVC74A	0.65 × V _{CC}		
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	SN74LVC74A	1.7		V
		V _{CC} = 2.7 V to 3.6 V		2		
		V _{CC} = 1.65 V to 1.95 V	SN74LVC74A		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V	SN74LVC74A		0.7	V
		V _{CC} = 2.7 V to 3.6 V			0.8	
VI	Input voltage	·		0	5.5	V
Vo	Output voltage			0	V _{CC}	V
		V _{CC} = 1.65 V	SN74LVC74A		-4	
	High lovel output ourrent	V _{CC} = 2.3 V	SN74LVC74A		-8	A
I _{OH}	High-level output current	V _{CC} = 2.7 V			-12	mA
		V _{CC} = 3 V			-24	
		V _{CC} = 1.65 V	SN74LVC74A		4	
	Laurelaurelauren errenak	V _{CC} = 2.3 V	SN74LVC74A		8	A
I _{OL}	Low-level output current	V _{CC} = 2.7 V			12	mA
		V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate	·			10	ns/V

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5.3 Recommended Operating Conditions (continued)

see(1)

			MIN	MAX	UNIT
т.	Operating free air temperature	SN54LVC74A	– 55	125	°C
I A	Operating free-air temperature	SN74LVC74A	-40	125	C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).

5.4 Thermal Information: SN74LVC74A

		SN74LVC74A						
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3	127.8	140.4	123.8	150.8	92.1	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	96.8	54.8	59.2	48.1	50.3	52.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	70.9	48	54.6	49.1	63.4	30.8	°C/W
ΨЈТ	Junction-to-top characterization parameter	16.6	20.3	24.1	17.9	6.2	2.4	°C/W
ΨЈВ	Junction-to-board characterization parameter	70.9	47.7	54.1	48.8	62.8	30.9	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	50.1	_	_	_	_	12.5	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP MAX	UNIT		
		I - 100	I _{OH} = -100 μA	V _{CC} = 1.65 V to 3.6 V and T _A = -55°C to 125°C (SN54LVC74A only)	V _{CC} - 0.2			
		ΙΟΗ – – ΙΟΟ μΑ	V_{CC} = 2.7 V to 3.6 V and T_A = -40°C to 125°C (SN74LVC74A only)	V _{CC} - 0.2				
V _{OH}	High-level output voltage	$I_{OH} = -4 \text{ mA}, V_{CC} = (SN74LVC74A \text{ only})$	= 1.65 V, and T _A = -40°C to 125°C /)	1.2				
On	- 1.13	I _{OH} = -8 mA, V _{CC} = (SN74LVC74A only	= 2.3 V, and T _A = -40°C to 125°C /)	1.7				
		L = 12 mΛ	V _{CC} = 2.7 V	2.2				
		I _{OH} = -12 mA	V _{CC} = 3 V	2.4				
		$I_{OH} = -24 \text{ mA}, V_{CC} = 3 \text{ V}$		2.2				
		I _{OL} = 100 μA	L = 100 uA	I = 100 uA	V_{CC} = 1.65 V to 3.6 V, and T_A = -40°C to 125°C (SN74LVC74A only)		0.2	
			V_{CC} = 2.7 V to 3.6 V and T_A = -55°C to 125°C (SN54LVC74A only)		0.2			
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, V _{CC} = (SN74LVC74A only	1.65 V, and T _A = -40°C to 125°C /)		0.45	V		
		I _{OL} = 8 mA, V _{CC} = 2 (SN74LVC74A only	2.3 V, and T _A = –40°C to 125°C /)		0.7			
		I_{OL} = 12 mA, V_{CC} =	2.7 V		0.4			
		I _{OL} = 24 mA, V _{CC} = 3 V			0.55			
I _I	Input current	$V_I = 5.5 \text{ V or GND},$	V _{CC} = 3.6 V		±5	μA		
I _{CC}	Supply current	$V_I = V_{CC}$ or GND, I	_O = 0, V _{CC} = 3.6 V		10	μA		
ΔI _{CC}	Change in supply current	One input at V_{CC} - V_{CC} = 2.7 V to 3.6	- 0.6 V, other inputs at V_{CC} or GND, and V		500	μА		

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5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
С	i Input capacitance	$V_I = V_{CC}$ or GND, $V_{CC} = 3.3$ V, $T_A = 25$ °C		5		pF

5.6 Timing Requirements: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

				MIN	MAX	UNIT	
f	Clock frequency	V _{CC} = 2.7 V			83	MHz	
f _{clock}	Clock frequency	V _{CC} = 3.3 V ± 0.3 V			100		
	Pulse duration	PRE or CLR low		3.3		no	
t _w	Pulse duration	CLK high or low		3.3		ns	
	Setup time before CLK↑		Data	V _{CC} = 2.7 V	3.4		
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3		ns	
t _{su}		PRE or CLR inactive	V _{CC} = 2.7 V	2.2			
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		2			
t _h	t _h Hold time, data after CLK↑			1		ns	

5.7 Timing Requirements: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

				MIN	MAX	UNIT	
f _{clock}	Clock frequency	V _{CC} = 1.8 V or 2.5 V			83	MHz	
		PRE or CLR low	V _{CC} = 1.8 V ± 0.15 V	4.1			
t _w Pul	Pulse duration	PRE OF CER IOW	$V_{CC} = 2.5 V \pm 0.2 V$	3.3		ns	
	ruise duration	CLK high or low	V _{CC} = 1.8 V ± 0.15 V	4.1			
			V _{CC} = 2.5 V ± 0.2 V	3.3			
		Data	V _{CC} = 1.8 V ± 0.15 V	3.6			
	Catus time before CLIVA	Data	V _{CC} = 2.5 V ± 0.2 V	2.3			
t _{su}	Setup time before CLK↑	PRE or CLR inactive	V _{CC} = 1.8 V ± 0.15 V	2.7		ns	
		PRE OF CER Mactive	V _{CC} = 2.5 V ± 0.2 V	1.9			
t _h	Hold time, data after CLK↑	V _{CC} = 1.8 V or 2.5 V		1		ns	

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5.8 Timing Requirements: SN74LVC74A, -40°C to 125°C and -40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

					MIN	MAX	UNIT	
		$T_A = -40^{\circ}C$ to	V _{CC} = 2.7 V		83			
f _{clock}	Clock frequency	125°C	V _{CC} = 3.3 V ± 0.3 V			100	MHz	
	$T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	and $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			150			
	Pulse duration	PRE or CLR low	V _{CC} = 2.7 V or 3.3 V		3.3		ne	
t _w F	ruise duration	CLK high or low	V _{CC} = 2.7 V or 3.3 V	3.3		ns		
		Data	T _A = -40°C to 125°C	V _{CC} = 2.7 V	3.4			
				$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3			
	Setup time before CLK↑		$T_A = -40$ °C to 85°C and	3		ns		
t _{su}	Setup time before CLN		T = 40°C to 125°C	V _{CC} = 2.7 V	2.2		115	
		PRE or CLR inactive	$T_A = -40^{\circ}C \text{ to } 125^{\circ}C$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2			
			$T_A = -40$ °C to 85°C and	2				
t _h	Hold time, data after CLK↑	V _{CC} = 2.7 V or 3.3 \	; = 2.7 V or 3.3 V				ns	

5.9 Switching Characteristics: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT	
t	Maximum clock			V _{CC} = 2.7 V	83		MHz	
	frequency	_	_	V _{CC} = 3.3 V ± 0.3 V	100		IVIT1Z	
		CLK	O or O	V _{CC} = 2.7 V		6	ns	
	Propagation (delay)			V _{CC} = 2.7 V	1	5.2		
τ _{pd}	time	PRE or CLR		V _{CC} = 3.3 V ± 0.3 V		6.4		
				V _{CC} = 3.3 V ± 0.3 V	1	5.4		

5.10 Switching Characteristics: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f _{max}	Maximum clock frequency	_	_		83		MHz
		CLK PRE		V _{CC} = 1.8 V ± 0.15 V	1	7.1	ns
	Propagation (delay)		⊣ QorQ	V _{CC} = 2.5 V ± 0.2 V	1	4.4	
^L pd	time			V _{CC} = 1.8 V ± 0.15 V	1	6.9	
				V _{CC} = 2.5 V ± 0.2 V	1	4.6	



5.11 Switching Characteristics: SN74LVC74A, -40°C to 125°C and -40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

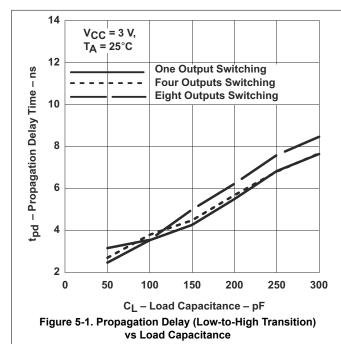
	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CO	NDITIONS	MIN	MAX	UNIT
	NA do		_	T _Δ = –40°C to 125°C	V _{CC} = 2.7 V	83		
f _{max}	Maximum clock frequency	_		1 _A = -40 0 to 125 0	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100		MHz
				$T_A = -40$ °C to 85°C and	V_{CC} = 3.3 V ± 0.3 V	150		
		CLK	- Q or Q	T _A = -40°C to 125°C	V _{CC} = 2.7 V	1	6	
					$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		5.2	
	Propagation (delay)			$T_A = -40$ °C to 85°C and $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	5.2	
t _{pd}	time			$T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C}$	V _{CC} = 2.7 V	1	6.4	ns
		PRE or CLR			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		5.4	
				$T_A = -40$ °C to 85°C and $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	5.4	
t _{sk(o)}	Skew (time), output	_	_	$T_A = -40$ °C to 85°C and	V _{CC} = 3.3 V ± 0.3 V		1	ns

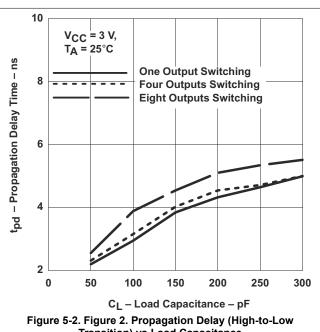
5.12 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST C	CONDITIONS	TYP	UNIT
			V _{CC} = 1.8 V	24	
C _{pd}	Power dissipation capacitance per flip-flop	f = 10 MHz	V _{CC} = 2.5 V	24	pF
			V _{CC} = 3.3 V	26	

5.13 Typical Characteristics





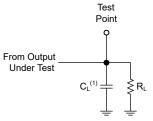
Transition) vs Load Capacitance

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_t \leq$ 2.5ns.

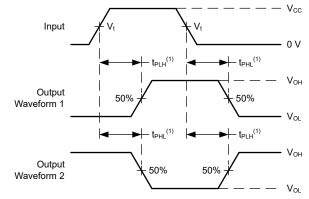
The outputs are measured individually with one input transition per measurement.

V _{cc}	V _t	R _L	CL	ΔV
1.8V ± 0.15V	V _{CC} /2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V _{CC} /2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



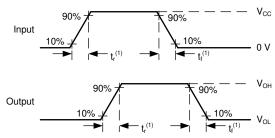
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

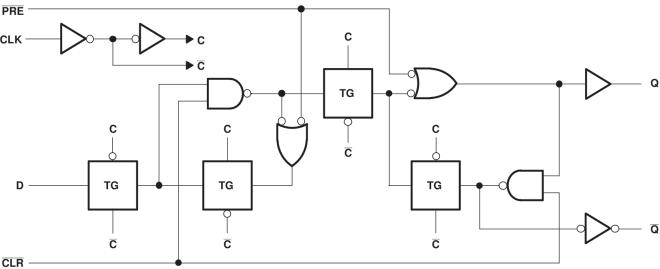
The SNx4LVC74A devices feature two independent positive-edge triggered D flip-flops. Integrated preset (PRE) and clear (CLR) functions allow for easy setup and control during operation.

The SN54LVC74A device is specified from -55°C to 125°C, and the SN74LVC74A device is specified from -40°C to 125°C.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of these devices for down-translation in a mixed-voltage environment.

7.2 Functional Block Diagram



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7.3 Feature Description

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

7.4 Device Functional Modes

Table 7-1 describes the SNx4LVC74A functionality and interactions between the PRE, CLR, CLK, and D inputs.

Table 7-1. Function Table **INPUTS OUTPUTS** PRE **CLR CLK** D Q $\overline{\mathbf{Q}}$ L Н Χ Х Н L Н L Χ Χ L Н L L Х Х $H^{(1)}$ $H^{(1)}$ Н Н Н Н L 1

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Table 7-1. Function	Table (d	continued)
INDUITO		OUTDU

	INP	OUTPUTS			
PRE	CLR	CLK	D	Q	Q
Н	Н	1	L	L	Н
Н	Н	L	Х	Q_0	\overline{Q}_{0}

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A common application for the SN74LVC74A is a frequency divider. By connecting the $\overline{\mathbb{Q}}$ output to the D input, the Q output toggles states on each positive edge of the incoming clock signal. Because it takes two positive edges, or two clock pulses, to complete one complete pulse on the output (one pulse to toggle from low to high, another to toggle from high to low), the incoming clock frequency is effectively divided by two.

8.2 Typical Application

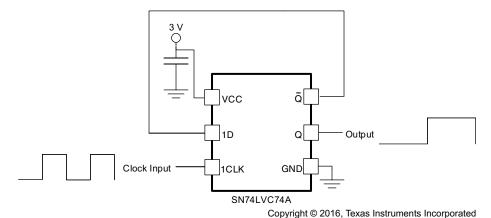


Figure 8-1. Frequency Divider

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

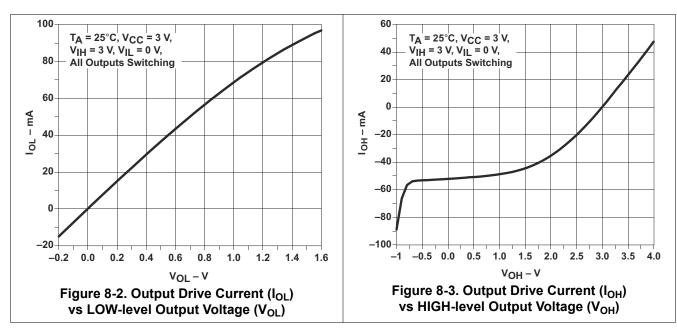
8.2.2 Detailed Design Procedure

- 1. Recommended input conditions:
 - For rise time and fall time specification, see (Δt/ΔV) in *Recommended Operating Conditions*.
 - For specified high and low levels, see (V_{IH} and V_{IL}) in Recommended Operating Conditions.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in Recommended Operating
 Conditions at any valid V_{CC}.
- 2. Recommended maximum output conditions:



- Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
- Outputs must not be pulled above V_{CC}.

8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply may be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01- μ F or 0.022- μ F capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

8.4 Layout

8.4.1 Layout Guidelines

Inputs must not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-4 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} , whichever makes more sense or is more convenient.



8.4.2 Layout Example

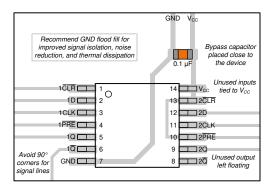


Figure 8-4. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision V (May 2024) to Revision W (December 2024)

Page

Changes from Revision U (January 2017) to Revision V (May 2024)

Page

- Added package size to Device Information table......1



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9761601Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9761601Q2A SNJ54LVC 74AFK
5962-9761601QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601QC A SNJ54LVC74AJ
5962-9761601QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601QD A SNJ54LVC74AW
5962-9761601VDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601VD A SNV54LVC74AW
SN74LVC74ABQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ABQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74AD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74AD.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADBR.B	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADBRG4	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADRE4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADT	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADT.B	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR1G4	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC74ANSR1G4.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR1G4.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74APW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWG4	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWRE4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWT	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWT.B	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWTG4	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYRG4.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYRG4.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SNJ54LVC74AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9761601Q2A SNJ54LVC 74AFK
SNJ54LVC74AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601Q A SNJ54LVC74A
SNJ54LVC74AW	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601QI A SNJ54LVC74AV

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC74A, SN54LVC74A-SP, SN74LVC74A:

Catalog: SN74LVC74A, SN54LVC74A

Automotive: SN74LVC74A-Q1, SN74LVC74A-Q1

Enhanced Product: SN74LVC74A-EP, SN74LVC74A-EP

Military: SN54LVC74A

Space : SN54LVC74A-SP

NOTE: Qualified Version Definitions:



PACKAGE OPTION ADDENDUM

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- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC74ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC74ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC74ANSR1G4	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVC74ARGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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*All dimensions are nominal

7 til dillionolono are nominal								
Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
SN74LVC74ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0	
SN74LVC74ADBR	SSOP	DB	14	2000	353.0	353.0	32.0	
SN74LVC74ADR	SOIC	D	14	2500	333.2	345.9	28.6	
SN74LVC74ADT	SOIC	D	14	250	213.0	191.0	35.0	
SN74LVC74ANSR	SOP	NS	14	2000	353.0	353.0	32.0	
SN74LVC74ANSR1G4	SOP	NS	14	2000	353.0	353.0	32.0	
SN74LVC74APWR	TSSOP	PW	14	2000	353.0	353.0	32.0	
SN74LVC74APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0	
SN74LVC74APWT	TSSOP	PW	14	250	353.0	353.0	32.0	
SN74LVC74ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0	
SN74LVC74ARGYRG4	VQFN	RGY	14	3000	353.0	353.0	32.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9761601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9761601VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC74AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC74AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC74APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC74APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC74APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC74AFK	FK	LCCC	20	55	506.98	12.06	2030	NA

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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