

SN74LVC2G74 Single Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset

1 Features

- Available in the Texas Instruments NanoFree™ package
- Supports 5 V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Maximum t_{pd} of 5.9 ns at 3.3 V
- Low power consumption, 10 μA maximum I_{CC}
- ± 24 mA output drive at 3.3 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA Per JESD 78, class II
- ESD protection exceeds JESD 22
 - 2000 V human-body model
 - 200 V machine model
 - 1000 V charged-device model

2 Applications

- Servers
- LED displays
- Network switch
- Telecom infrastructure
- Motor drivers
- I/O expanders

3 Description

This single positive-edge-triggered D-type flip-flop is designed for 1.65 V to 5.5 V V_{CC} operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

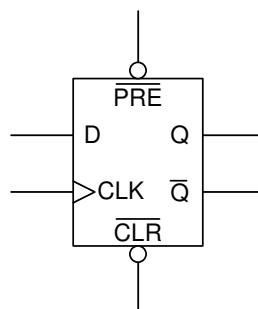
A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC2G74	SM8 (8)	2.95 mm × 2.80 mm
	VSSOP (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

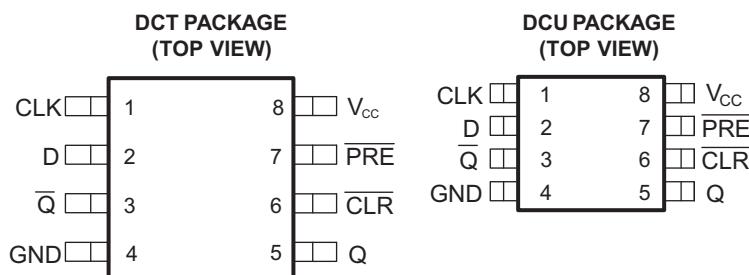
Changes from Revision P (July 2016) to Revision Q (September 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the <i>Application and Information</i> section.....	10
• Updated the <i>Device Power Button Circuit</i> figure in the <i>Typical Power Button Circuit</i> section.....	10

Changes from Revision O (January 2015) to Revision P (July 2016)	Page
• Changed SSOP to SM8 in <i>Device Information</i> table.....	1
• Updated pinout images to new format.....	3
• Added pin number for DSBGA package in <i>Pin Functions</i> table.....	3
• Changed 6 PINS to 8 PINS in <i>Thermal Information</i> table.....	5
• Changed 23 to 2.3 for t_{su} data in <i>Timing Requirements, -40°C to $+125^{\circ}\text{C}$</i>	6

Changes from Revision N (July 2013) to Revision O (January 2015)	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1

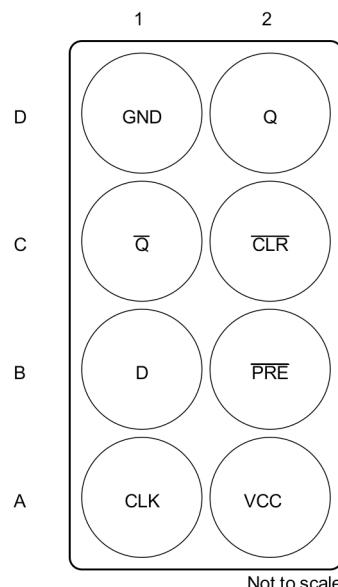
Changes from Revision M (February 2007) to Revision N (July 2013)	Page
• Changed I_{off} description in <i>Features</i>	1
• Added parameter values for -40 to $+125^{\circ}\text{C}$ temperature ratings in <i>Electrical Characteristics</i> table.....	6
• Changed <i>Timing Requirements, -40°C to $+85^{\circ}\text{C}$</i> table.....	6
• Added <i>Timing Requirements, -40°C to $+125^{\circ}\text{C}$</i> table.....	6
• Changed <i>Switching Characteristics, -40°C to $+85^{\circ}\text{C}$</i> table.....	7
• Added <i>Switching Characteristics, -40°C to $+125^{\circ}\text{C}$</i> table.....	7

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

Figure 5-1. DCT 8-Pin SM8 and DCU 8-Pin VSSOP Package Top View



See mecahnical drawings for dimensions.

Figure 5-2. YZP Package 8-Pin DSBGA Bottom View

Table 5-1. Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	VSSOP, SM8	DSBGA		
CLK	1	A1	I	Clock input
CLR	6	C2	I	Clear input – Pull low to set Q output low
D	2	B1	I	Input
GND	4	D1	—	Ground
PRE	7	B2	I	Preset input – Pull low to set Q output high
Q	5	D2	O	Output
Q-bar	3	C1	O	Inverted output
V _{cc}	8	A2	—	Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	6.5
V_I	Input voltage ⁽²⁾		-0.5	6.5
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	6.5
V_O	Voltage range applied to any output in the high or low state ^{(2) (3)}	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current $V_I < 0$			-50
I_{OK}	Output clamp current $V_O < 0$			-50
I_O	Continuous output current			± 50
	Continuous current through V_{CC} or GND			± 100
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The value of V_{CC} is provided in [Section 6.3](#) table.

6.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-4		mA
		V _{CC} = 2.3 V	-8		
		V _{CC} = 3 V	-16		
		V _{CC} = 4.5 V	-24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 3 V	16		
		V _{CC} = 4.5 V	24		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V _{CC} = 3.3 V ± 0.3 V	10		
		V _{CC} = 5 V ± 0.5 V	5		
T _A	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC2G74			UNIT	
	DCT	DCU	YZP		
	8 PINS				
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-40°C to +85°C			-40°C to +125°C			UNIT	
			Recommended			-40°C to +125°C				
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP	MAX		
V _{OH}	I _{OH} = -100 µA	1.65 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V	
	I _{OH} = -4 mA	1.65 V	1.2			1.2				
	I _{OH} = -8 mA	2.3 V	1.9			1.85				
	I _{OH} = -16 mA	3 V	2.4			2.4				
	I _{OH} = -24 mA		2.3			2.3				
	I _{OH} = -32 mA	4.5 V	3.8			3.8				
V _{OL}	I _{OL} = 100 µA	1.65 V to 5.5 V	0.1			0.1			V	
	I _{OL} = 4 mA	1.65 V	0.45			0.45				
	I _{OL} = 8 mA	2.3 V	0.3			0.3				
	I _{OL} = 16 mA	3 V	0.4			0.4				
	I _{OL} = 24 mA		0.55			0.55				
	I _{OL} = 32 mA	4.5 V	0.55			0.55				
I _I	Data or control inputs	V _I = 5.5 V or GND	0 to 5.5 V			±5			µA	
I _{off}	V _I or V _O = 5.5 V	0	±10			±10			µA	
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10			10			µA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500			500			µA	
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements, -40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM	TO	-40°C to +85°C						UNIT	
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V			
			MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}			80		175		175		200	MHz
t _w	CLK		6.2		2.7		2.7		2	ns
	PRE or CLR low		6.2		2.7		2.7		2	
t _{su}	Data		2.9		1.7		1.3		1.1	ns
	PRE or CLR inactive		1.9		1.4		1.2		1	
t _h			0		0.3		1.2		0.5	ns

6.7 Timing Requirements, -40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM	TO	-40°C to +125°C						UNIT	
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V			
			MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}			80		120		120		140	MHz
t _w	CLK		6.2		3.5		3.5		3.3	ns
	PRE or CLR low		6.2		3.5		3.5		3.3	
t _{su}	Data		2.9		2.3		1.9		1.7	ns
	PRE or CLR inactive		1.9		2		1.8		1.6	
t _h			0		0.3		0.5		0.5	ns

6.8 Switching Characteristics, -40°C to $+85^{\circ}\text{C}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM	TO	-40°C to $+85^{\circ}\text{C}$								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{max}			80		175		175		200		MHz	
t_{pd}	CLK	Q	4.8	13.4	2.2	7.1	2.2	5.9	1.4	4.1	ns	
		\bar{Q}	6	14.4	3	7.7	2.6	6.2	1.6	4.4		
	PRE or CLR low	Q or \bar{Q}	4.4	12.9	2.3	7	1.7	5.9	1.6	4.1		

6.9 Switching Characteristics, -40°C to $+125^{\circ}\text{C}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

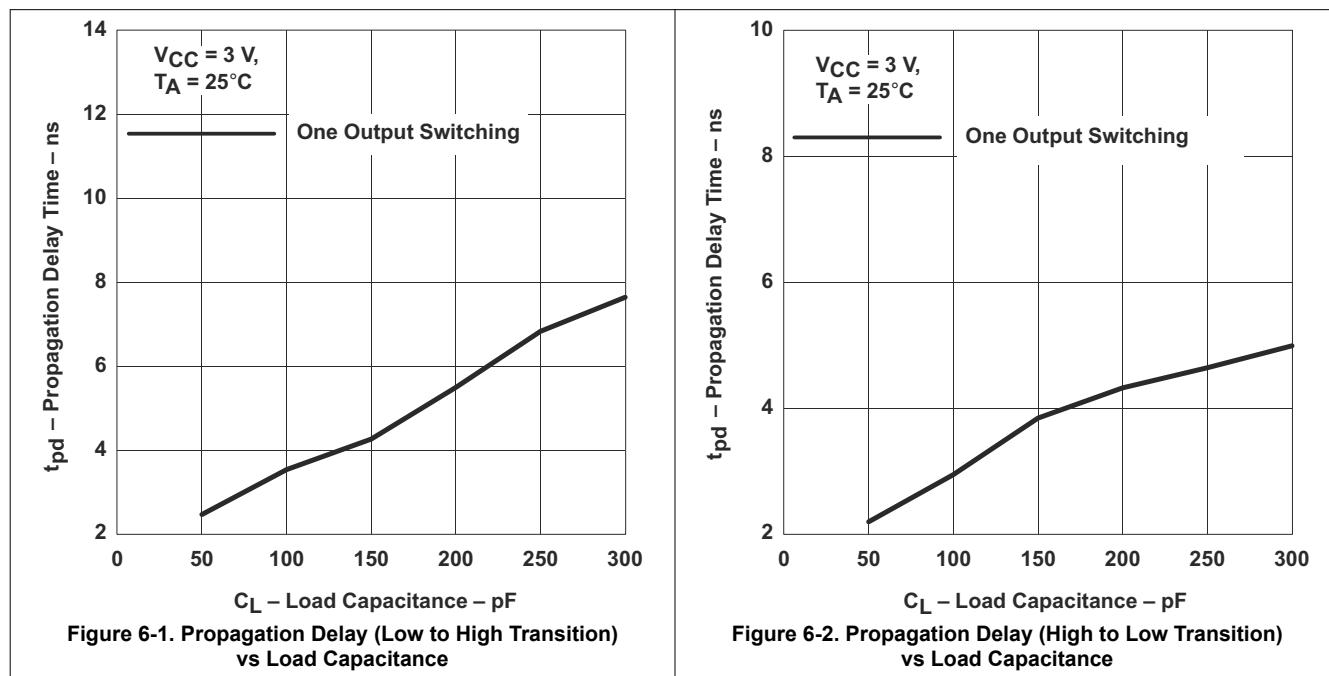
PARAMETER	FROM	TO	-40°C to $+125^{\circ}\text{C}$								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{max}			80		120		120		140		MHz	
t_{pd}	CLK	Q	4.8	14.4	2.2	8.1	2.2	6.9	1.4	5.1	ns	
		\bar{Q}	6	16	3	9.7	2.6	7.2	1.6	5.4		
	PRE or CLR low	Q or \bar{Q}	4.4	14.9	2.3	9.5	1.7	7.9	1.6	6.1		

6.10 Operating Characteristics

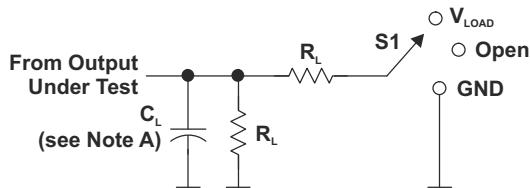
$T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 \text{ V}$	UNIT	
		TYP	TYP	TYP	TYP		
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF

6.11 Typical Characteristics



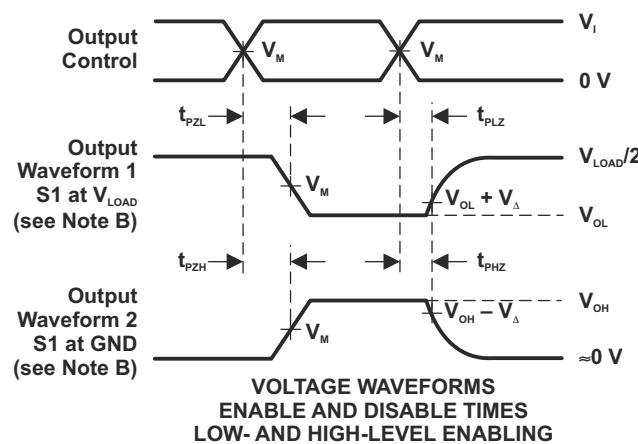
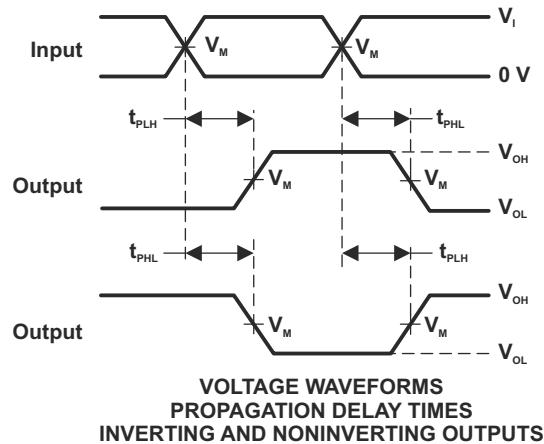
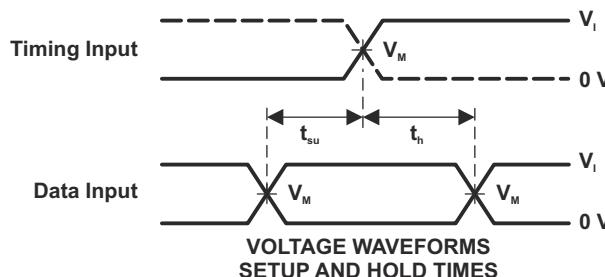
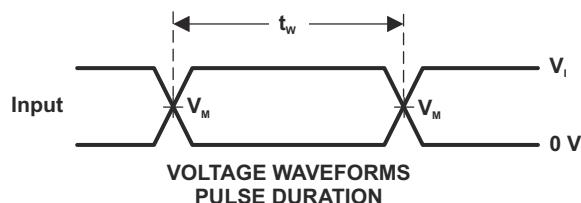
7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	V_{CC}	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices.

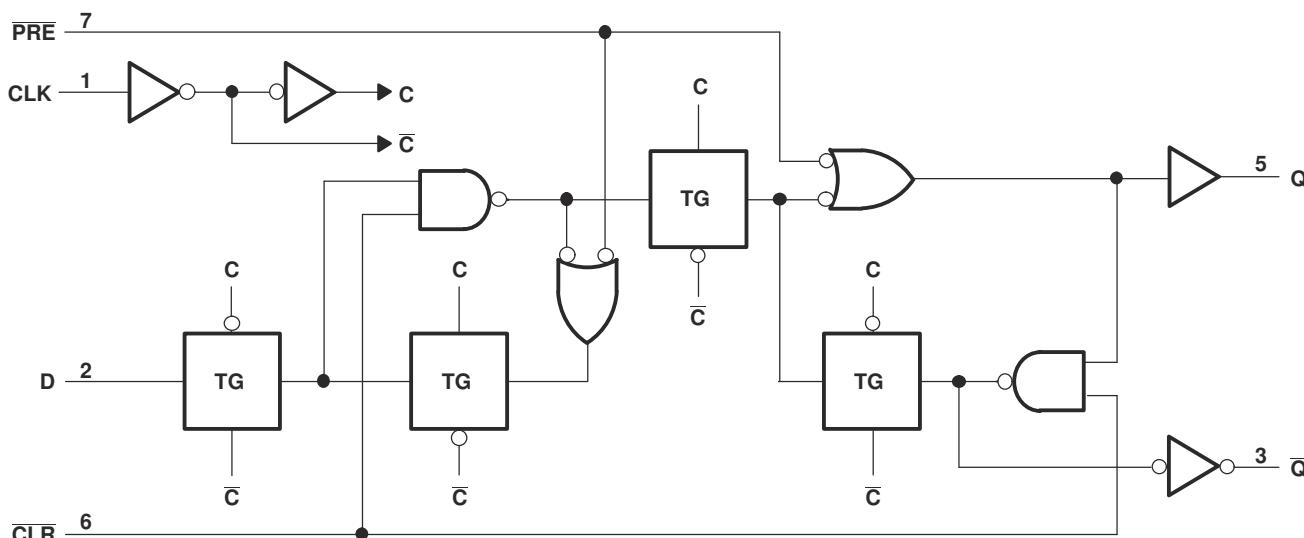
Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

- Allows down voltage translation
 - 5 V to 3.3 V
 - 5 V or 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V
- I_{off} Feature
 - Can prevent backflow current that can damage device when powered down.

8.4 Device Functional Modes

Table 8-1 shows the functional modes of SN74LVC2G74.

Table 8-1. Function Table

Inputs				Outputs	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0

(1) This configuration is non-stable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The $330\ \Omega$ resistor and $22\ \text{pF}$ capacitor shown in [Figure 9-1](#) produce enough delay to meet the hold time requirement of the D input. To calculate the delay for a particular RC combination, use [Equation 1](#). The delay with this RC combination is 5.03 ns

$$t_{\text{delay}} = -RC \ln(0.5) \approx 0.693 RC \quad (1)$$

To ensure proper operation, check that the transition time of the RC circuit meets the transition time requirements of the device inputs listed in the Recommended Operating Conditions table. Transition time for an RC can be approximated with [Equation 2](#).

$$t \approx 2.2 RC \quad (2)$$

In this case, transition time is 18.15 ns, which equates to a 4.54 ns / V input transition rate at $V_{CC} = 5\ \text{V}$, and is below the 5 ns / V maximum requirement for recommended operation.

9.2 Typical Power Button Circuit

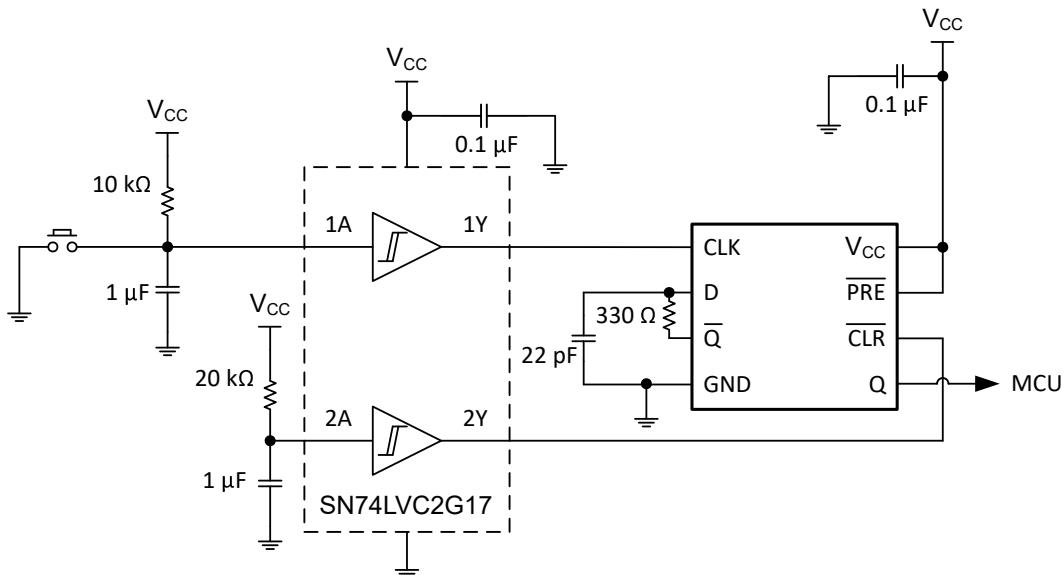


Figure 9-1. Device Power Button Circuit

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

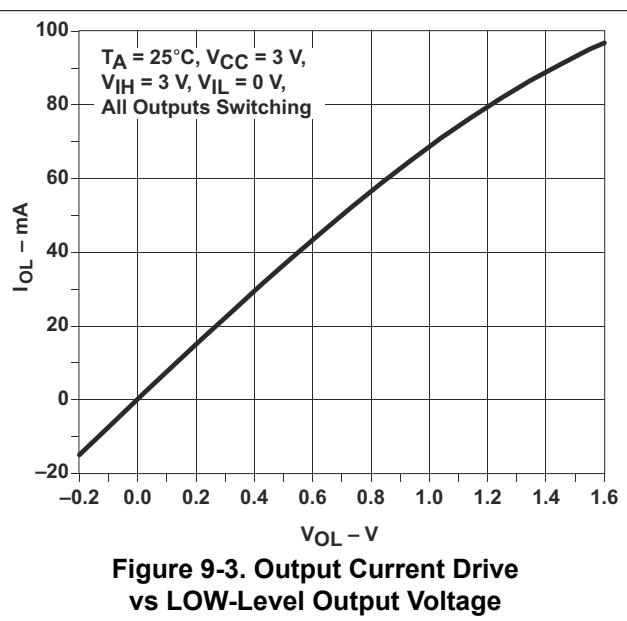
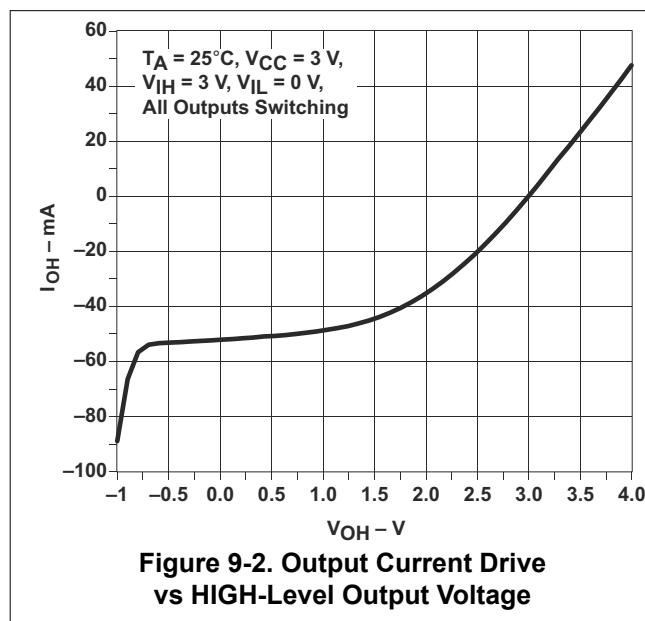
1. Recommended Input Conditions:

- For rise time and fall time specifications, see ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
- For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}

2. Recommend Output Conditions:

- Load currents should not exceed 50 mA per output and 100 mA total for the part.
- Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} terminals then .01- μ F or .022- μ F capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 11-1](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

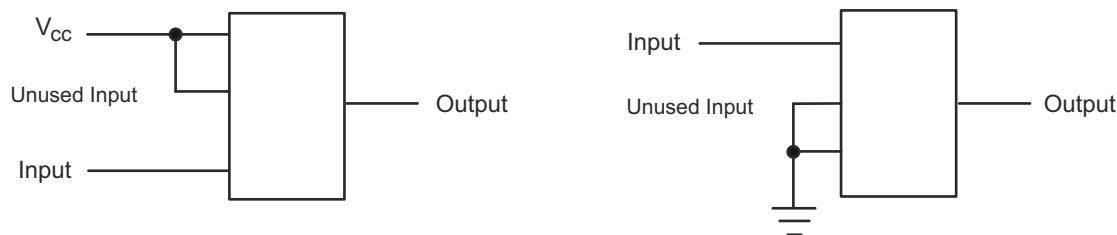


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

NanoFree™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

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12.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC2G74DCT3	Obsolete	Production	SSOP (DCT) 8	-	-	Call TI	Call TI	-40 to 125	C74Z
SN74LVC2G74DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2WS5, C74)Z
SN74LVC2G74DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2WS5, C74)Z
SN74LVC2G74DCTRE4	Active	Production	SSOP (DCT) 8	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74Z
SN74LVC2G74DCTRE4.B	Active	Production	SSOP (DCT) 8	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74Z
SN74LVC2G74DCTRE6	Obsolete	Production	SSOP (DCT) 8	-	-	Call TI	Call TI	-40 to 125	C74Z
SN74LVC2G74DCTRG4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74Z
SN74LVC2G74DCTRG4.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74Z
SN74LVC2G74DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(74, C74J, C74Q, C74R)CZ
SN74LVC2G74DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(74, C74J, C74Q, C74R)CZ
SN74LVC2G74DCURE4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R
SN74LVC2G74DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R
SN74LVC2G74DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R
SN74LVC2G74DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C74J, C74Q, C74R)
SN74LVC2G74DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C74J, C74Q, C74R)
SN74LVC2G74DCUTE4	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R
SN74LVC2G74DCUTG4	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R
SN74LVC2G74DCUTG4.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R
SN74LVC2G74YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CPN

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC2G74YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CPN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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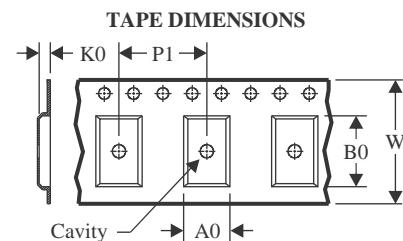
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2G74 :

- Automotive : [SN74LVC2G74-Q1](#)
- Enhanced Product : [SN74LVC2G74-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

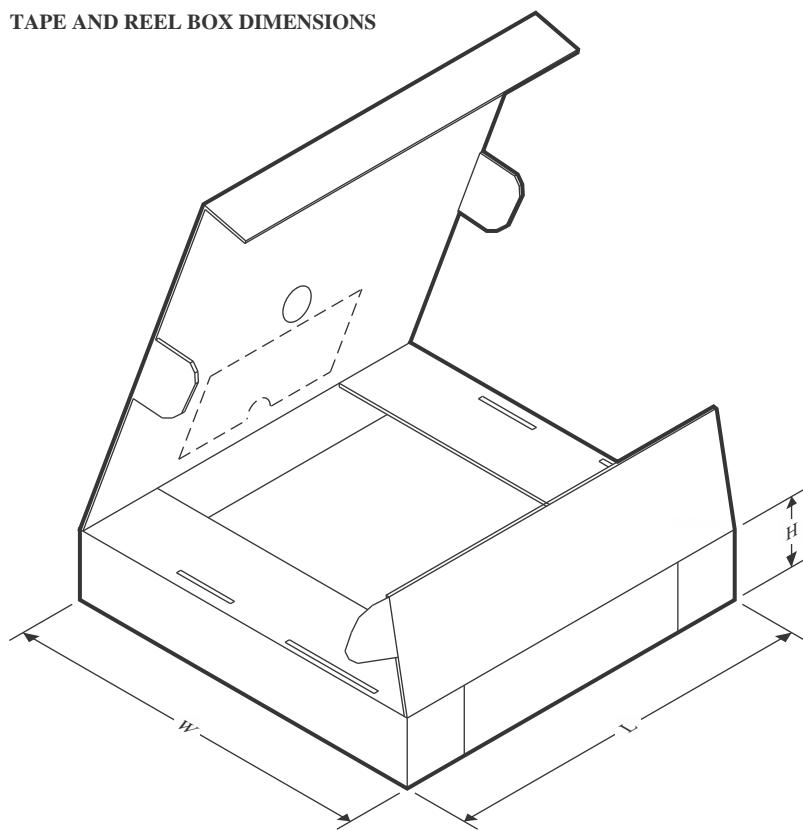
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G74DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC2G74DCTRG4	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

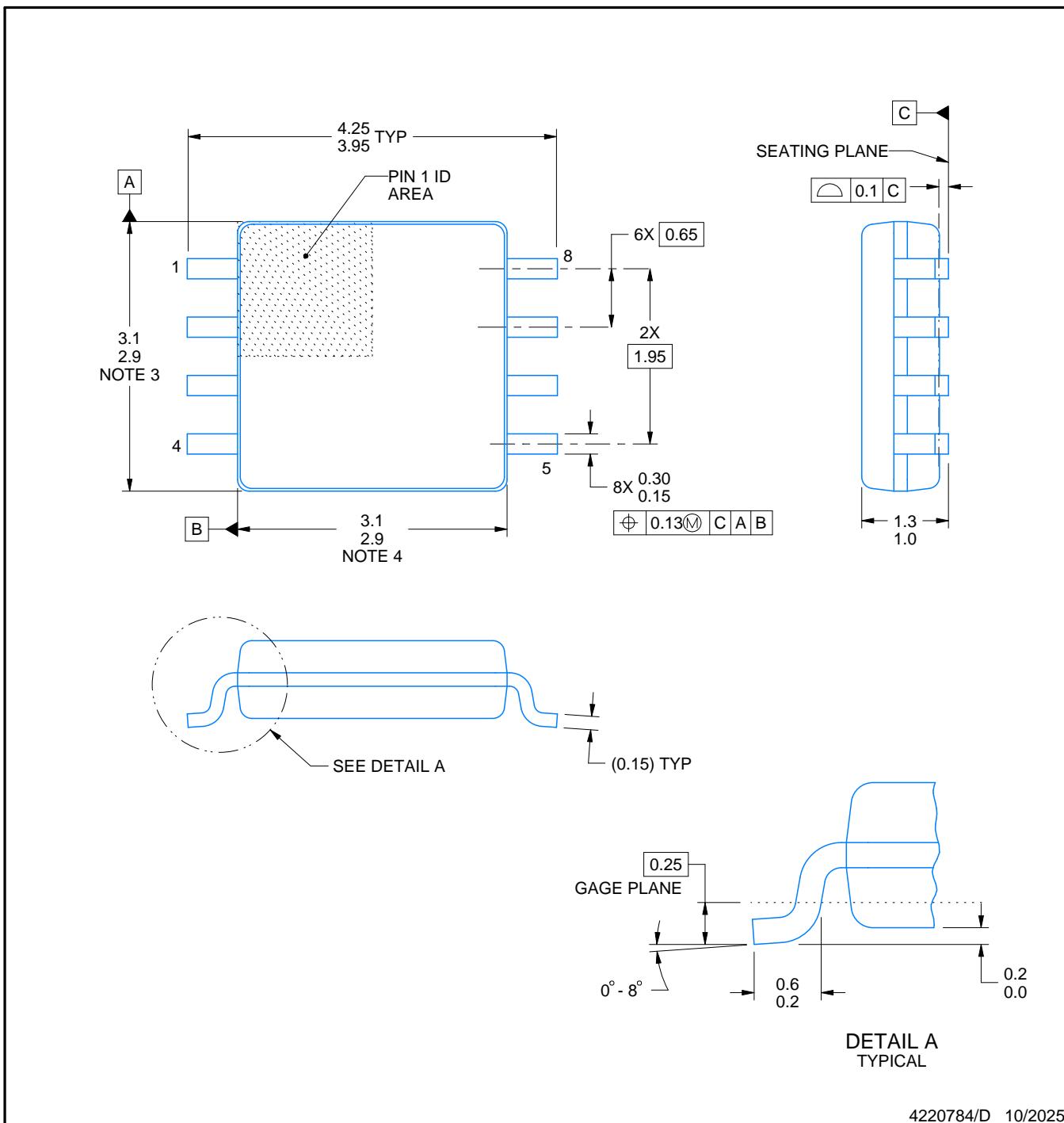
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G74DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC2G74DCTRG4	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G74DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G74DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G74DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



PACKAGE OUTLINE

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



NOTES:

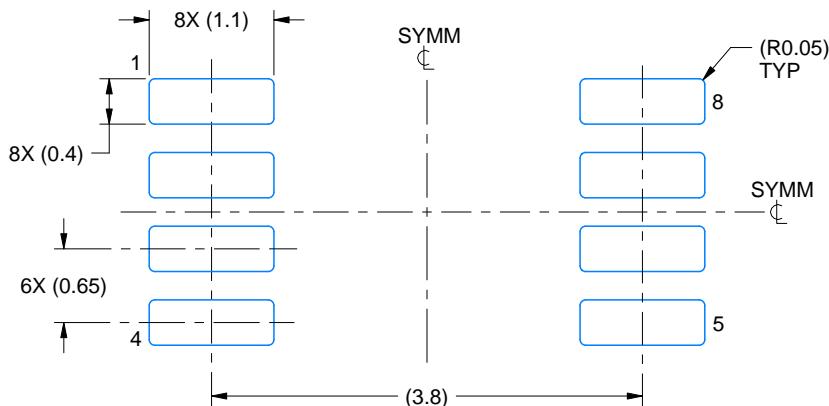
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

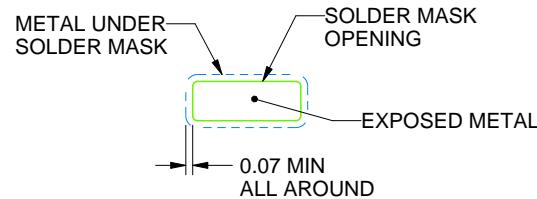
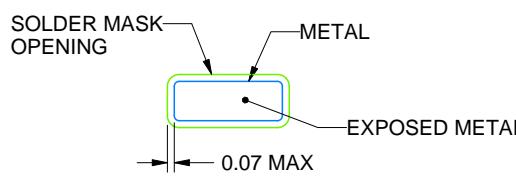
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

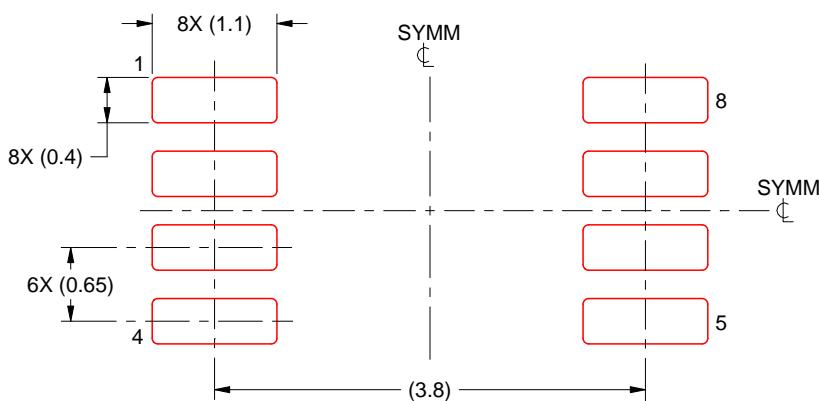
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

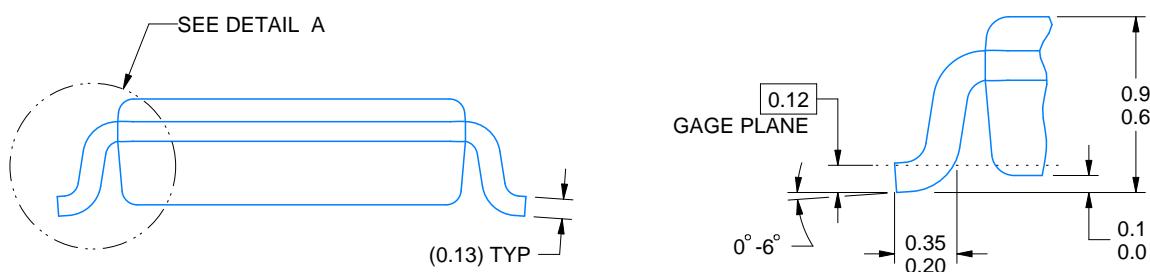
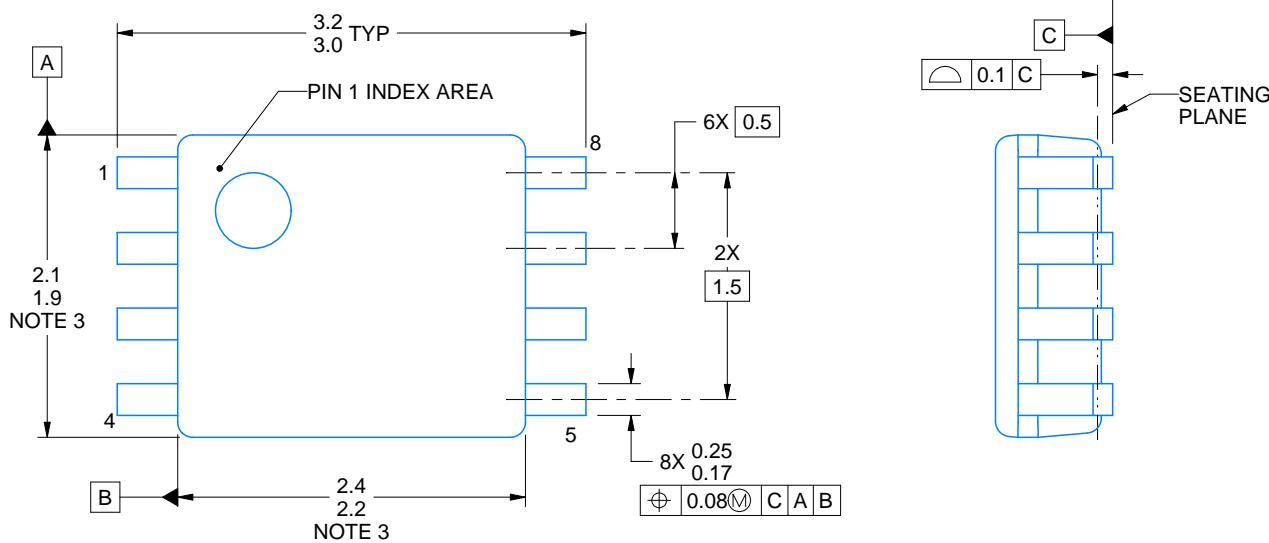
PACKAGE OUTLINE

DCU0008A



VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



DETAIL A TYPICAL

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

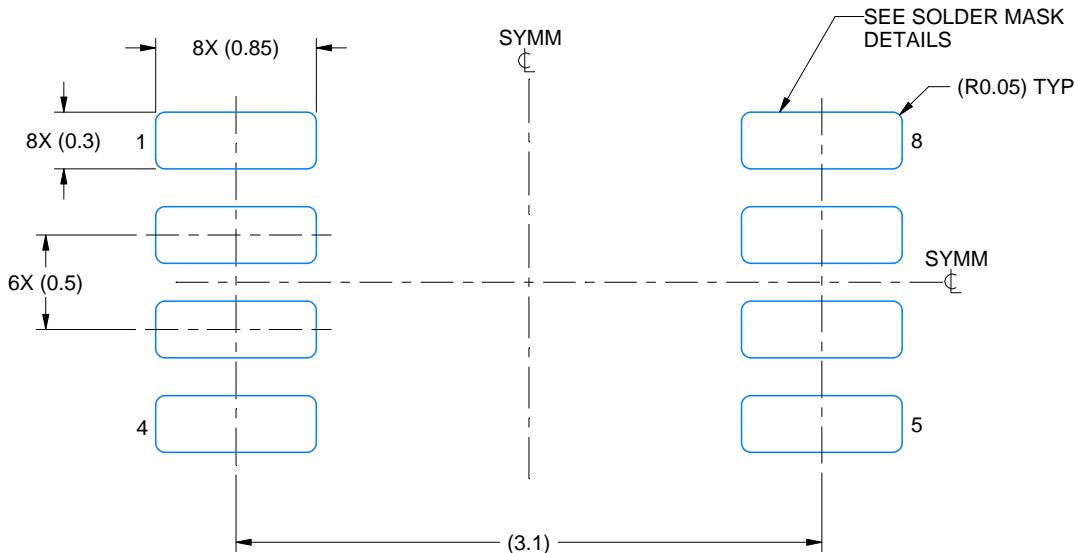
4225266/A 09/2014

EXAMPLE BOARD LAYOUT

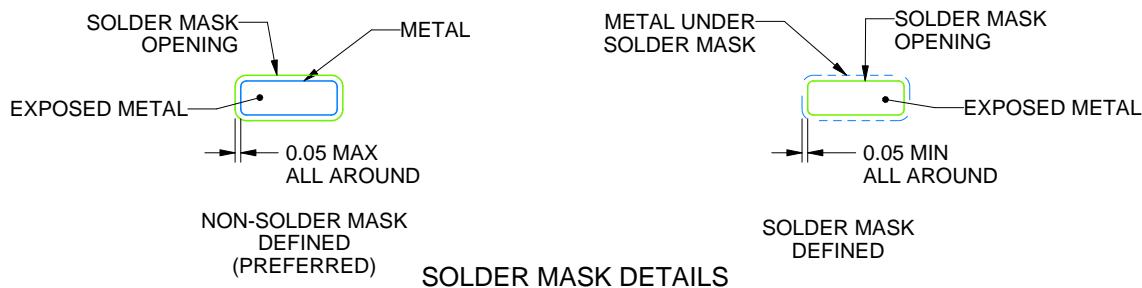
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

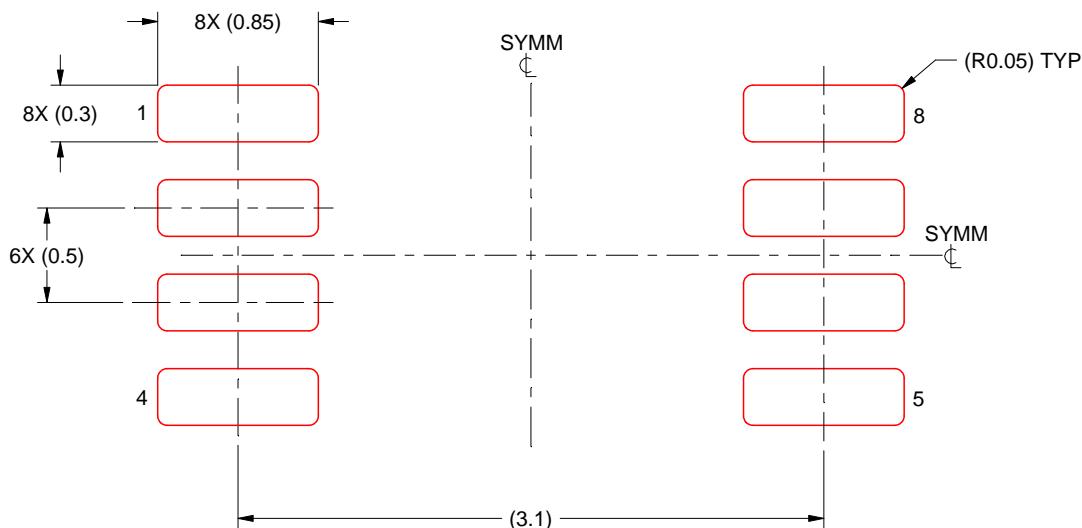
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

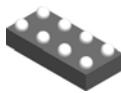


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

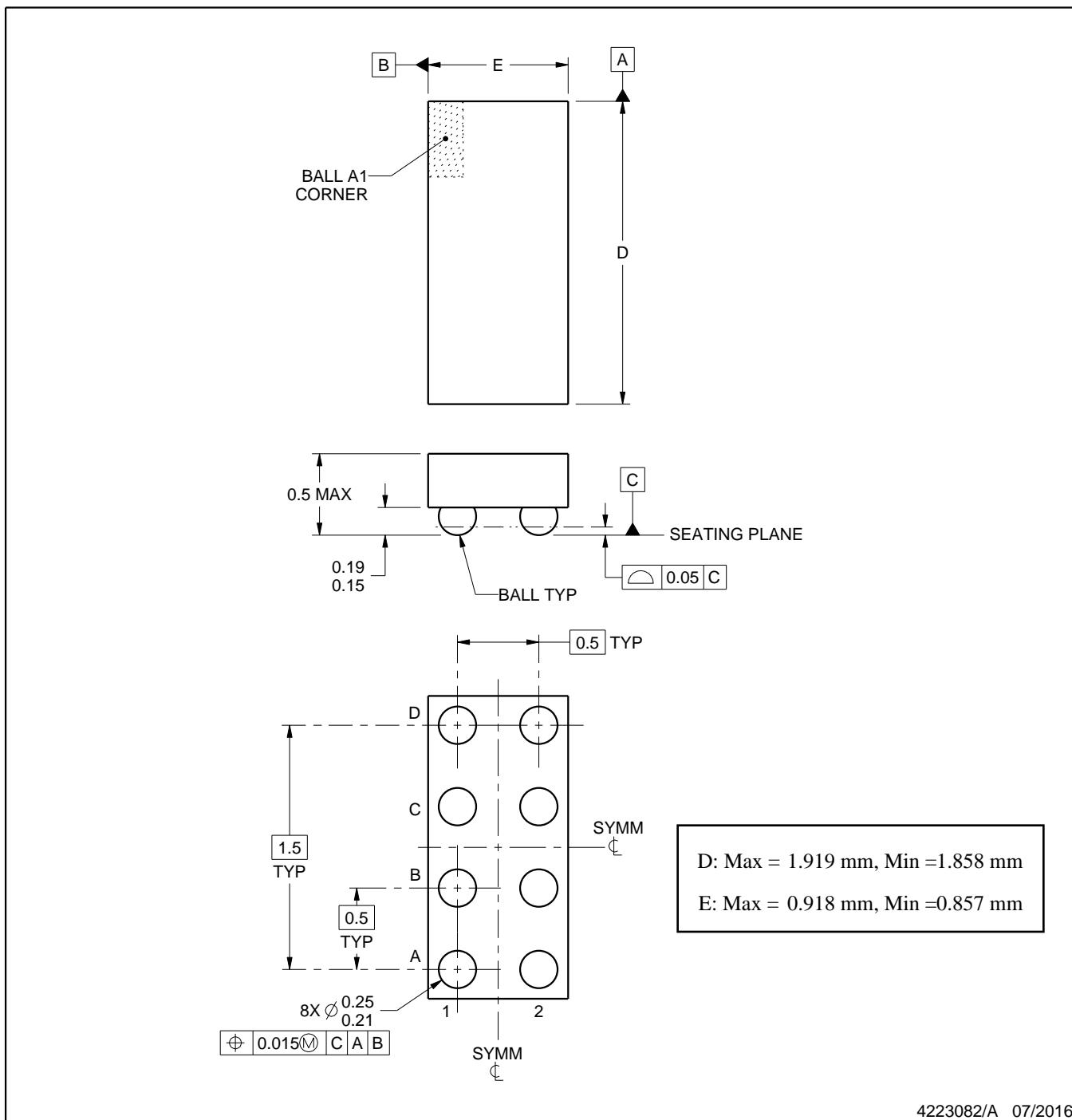


PACKAGE OUTLINE

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

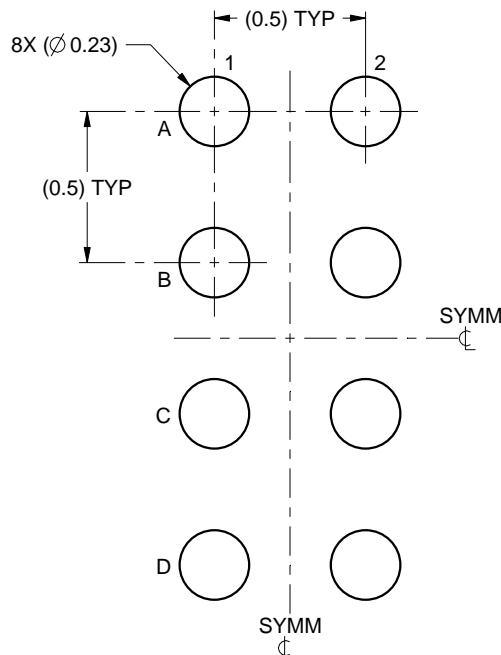
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

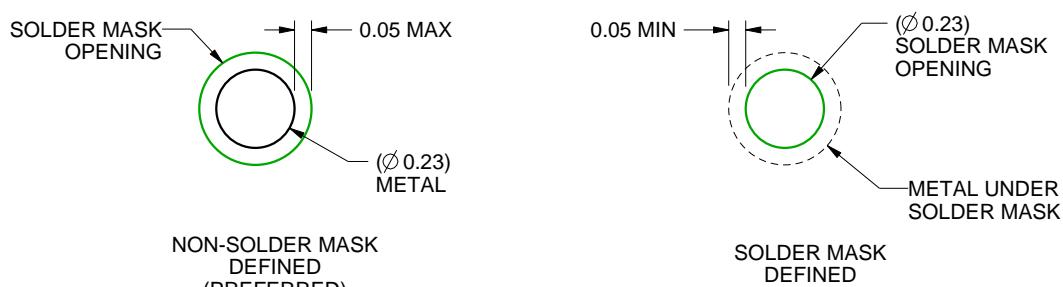
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

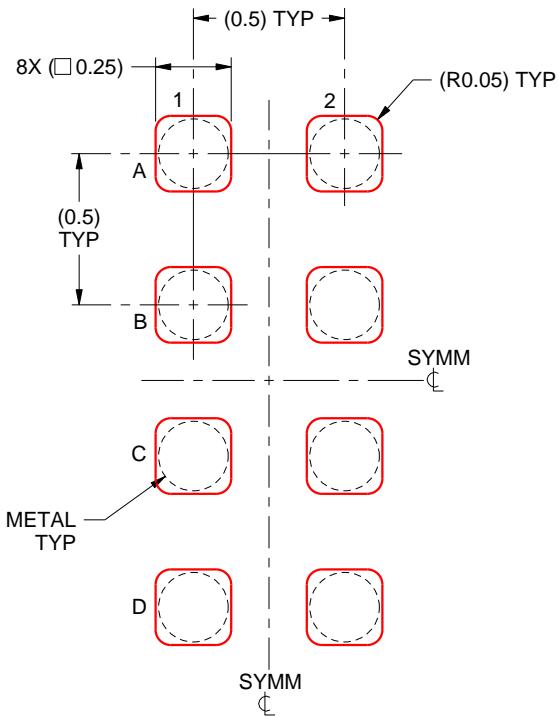
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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