











SN74LVC2G53

SCES324Q - JULY 2001 - REVISED JANUARY 2019

# SN74LVC2G53 Single-Pole Double-Throw (SPDT) Analog Switch 2:1 Analog Multiplexer/Demultiplexer

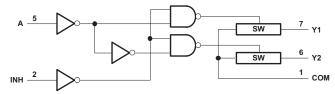
### **Features**

- Available in the Texas Instruments NanoFree™ Package
- 1.65-V to 5.5-V V<sub>CC</sub> Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns ( $V_{CC} = 3 \text{ V}$ ,  $C_1 = 50 \text{ pF}$
- Low ON-State Resistance, Typically 6.5 Ω  $(V_{CC} = 4.5 \text{ V})$
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

# **Applications**

- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

#### **Logic Diagram**



NOTE: For simplicity, the test conditions shown in Figure 1 through Figure 4 and Figure 6 through Figure 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

# 3 Description

This single 2:1 analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoFree package technology is maior breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G53DCT	SM8 (8)	2.95 mm × 2.80 mm
SN74LVC2G53DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74LVC2G53YZP	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram, Each Switch (SW)

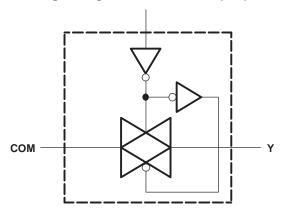




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# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

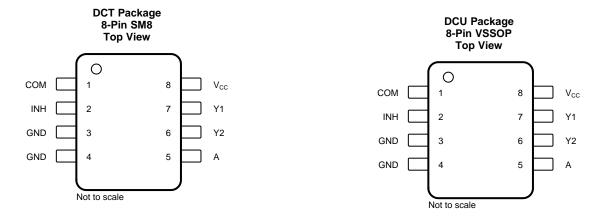
Changes from Revision P (October 2016) to Revision Q	Page
Changed the Thermal Information table	5
Changes from Revision O (December 2015) to Revision P	Page
Added DSBGA package in <i>Pin Functions</i> table	3
Added Receiving Notification of Documentation Updates section	
Changes from Revision N (January 2014) to Revision O	Page
<ul> <li>Added Applications section, Device Information table, ESD Ratings table, Thermal Inform Description section, Device Functional Modes, Application and Implementation section, F Recommendations section, Layout section, Device and Documentation Support section, a Packaging, and Orderable Information section.</li> </ul>	ower Supply and Mechanical,
Moved T <sub>sta</sub> to Absolute Maximum Ratings table	4

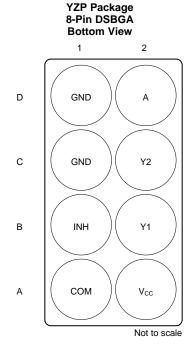
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# 5 Pin Configuration and Functions





See Mechanical, Packaging, and Orderable Information for dimensions.

### **Pin Functions**

	PIN		1/0	DESCRIPTION
NAME	SM8, VSSOP	DSBGA	1/0	DESCRIPTION
Α	5	D2	1	Controls the switch
COM	1	A1	I/O	Bidirectional signal to be switched
GND	3	C1	_	Ground pin
GND	4	D1	_	Ground pin
INH	2	B1	I	Enables or disables the switch
$V_{CC}$	8	A2	_	Power pin
Y2	6	C2	I/O	Bidirectional signal to be switched
Y1	7	B2	I/O	Bidirectional signal to be switched



## 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage (2)		-0.5	6.5	V
VI	Input voltage (2)(3)		-0.5	6.5	V
V <sub>I/O</sub>	Switch I/O voltage <sup>(2)(3)(4)</sup>		-0.5	$V_{CC} + 0.5$	V
I <sub>IK</sub>	Control input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>I/OK</sub>	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		±50	mA
I <sub>T</sub>	ON-state switch current	$V_{I/O} = 0$ to $V_{CC}$		±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
$T_{J}$	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	\/	
	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

See note(1).

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		1.65	5.5	V
V <sub>I/O</sub>	I/O port voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	$V_{CC} \times 0.65$		
V <sub>IH</sub>	Lligh level input voltage control input	$V_{CC}$ = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		V
	High-level input voltage, control input	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	$V_{CC} \times 0.7$		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		
	Low-level input voltage, control input	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$V_{CC} \times 0.35$	V
\/		$V_{CC}$ = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
VIL		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		$V_{CC} \times 0.3$	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$	
$V_{I}$	Control input voltage		0	5.5	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		20	
A + / A > ,	Innut transition via and fall time	$V_{CC}$ = 2.3 V to 2.7 V		20	20/1
Δt/Δv	Input transition rise and fall time	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		10	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		10	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

<sup>(2)</sup> All voltages are with respect to ground, unless otherwise specified.

<sup>(3)</sup> The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(4)</sup> This value is limited to 5.5 V maximum.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



### 6.4 Thermal Information

	THERMAL METRIC <sup>(1)</sup>	DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	185.9	288.9	98.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	116.3	99.6	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.4	207.3	27.6	°C/W
ΨЈΤ	Junction-to-top characterization parameter	41.6	22.4	0.6	°C/W
ΨЈВ	Junction-to-board characterization parameter	97.3	205.7	27.4	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	V <sub>cc</sub>	MIN TYP(1)	MAX	UNIT	
			V – V – or CND	I <sub>S</sub> = 4 mA	1.65 V	13	30		
_	ON-state switch resistance		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$	$I_S = 8 \text{ mA}$	2.3 V	10	20	Ω	
r <sub>on</sub>	OIN-State Switch resistance		(see Figure 2	$I_S = 24 \text{ mA}$	3 V	8.5	17	12	
			and Figure 1)	$I_S = 32 \text{ mA}$	4.5 V	6.5	13		
			$V_I = V_{CC}$ to GND,	$I_S = 4 \text{ mA}$	1.65 V	86.5	120		
_	Peak ON-state resistance		$V_{INH} = V_{IL}$	$I_S = 8 \text{ mA}$	2.3 V	23	30	Ω	
r <sub>on(p)</sub>	reak OIN-State resistance	(se	(see Figure 2	$I_S = 24 \text{ mA}$	3 V	13	20	12	
			and Figure 1)	$I_S = 32 \text{ mA}$	4.5 V	8	15		
			$V_{I} = V_{CC}$ to GND,	$I_S = 4 \text{ mA}$	1.65 V		7		
۸۰	Difference of ON-state resistance	tance	$V_C = V_{CC}$ to GND, $V_C = V_{IH}$	$I_S = 8 \text{ mA}$	2.3 V		5	Ω	
$\Delta r_{on}$	between switches	switches	(see Figure 2	$I_S = 24 \text{ mA}$	3 V		3		
	and Figure 1	and Figure 1)	$I_S = 32 \text{ mA}$	4.5 V		2			
			$V_I = V_{CC}$ and $V_O = GND$		5.5 V		±1		
I <sub>S(off)</sub>	OFF-state switch leakage co	urrent	$V_I = GND$ and $V_O = V_{CO}$ $V_{INH} = V_{IH}$ (see Figure 3				±0.1 <sup>(1)</sup>	μА	
	ON state quitab la diseas au		$V_I = V_{CC}$ or GND, $V_{INH}$	= V <sub>II</sub> ,	F F V		±1		
I <sub>S(on)</sub>	ON-state switch leakage cu	rrent	V <sub>O</sub> = Open (see Figure	4)	5.5 V		±0.1 <sup>(1)</sup>	μΑ	
	Control inner to account		V V ~ CND		5.5.4		±1	۸	
l <sub>l</sub>	Control input current		$V_C = V_{CC}$ or GND		5.5 V		±0.1 <sup>(1)</sup>	μА	
I <sub>CC</sub>	Supply current		$V_C = V_{CC}$ or GND		5.5 V		1	μΑ	
$\Delta I_{CC}$	Supply-current change		$V_{C} = V_{CC} - 0.6 \text{ V}$		5.5 V		500	μΑ	
C <sub>ic</sub>	Control input capacitance				5 V	3.5		pF	
0	Switch input/output	Υ			5.V	6.5			
C <sub>io(off)</sub>	capacitance	COM			5 V	10		pF	
C <sub>io(on)</sub>	Switch input/output capacita	ince			5 V	19.5		pF	

(1)  $T_A = 25^{\circ}C$ 

<sup>(2)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>cc</sub>	MIN	MAX	UNIT
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		2	
<b>.</b> (1)	COM or V	V or COM	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		1.2	
t <sub>pd</sub> <sup>(1)</sup>	COM or Y	Y or COM	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		0.8	ns
			$V_{CC} = 5 V \pm 0.5 V$		0.6	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	3.3	9	
t <sub>en</sub> <sup>(2)</sup>	INH	COMerv	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	2.5	6.1	
en (=)	IINIT	COM or Y	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2.2	5.4	ns
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1.8	4.5	
	INH	COM or Y	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	3.2	10.9	ns
t <sub>dis</sub> (3)			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	2.3	8.3	
ldis (°)			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2.3	8.1	
			$V_{CC} = 5 V \pm 0.5 V$	1.6	8	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	2.9	10.3	
t <sub>en</sub> <sup>(2)</sup>	^	COMerv	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	2.1	7.2	ns
len` ′	Α	COM or Y	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.9	5.8	
			$V_{CC} = 5 V \pm 0.5 V$	1.3	5.4	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	2.1	2.1	ns
(3)	^	COMery	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.4	7.9	
t <sub>dis</sub> (3)	Α	COM or Y	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.1	7.2	
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1	5	

<sup>(1)</sup> t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

# 6.7 Analog Switch Characteristics

 $T_A = 25$ °C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>cc</sub>	ТҮР	UNIT
				1.65 V	35	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	120	
			f <sub>in</sub> = sine wave (see Figure 6)	3 V	190	
Frequency response	COMerV	V or COM		4.5 V	215	NAL I-
(switch on)	COM or Y	Y or COM		1.65 V	>300	MHz
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$ $f_{in} = \text{sine wave}$ (see Figure 6)	2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
			$C_L$ = 50 pF, $R_L$ = 600 $\Omega$ , $f_{in}$ = 1 MHz (sine wave) (see Figure 7)	1.65 V	-58	dB
				2.3 V	-58	
				3 V	-58	
Crosstalk <sup>(1)</sup>	COM an V	V == COM		4.5 V	-58	
(between switches)	COM or Y	Y or COM		1.65 V	-42	
			$C_L$ = 5 pF, $R_L$ = 50 $\Omega$ , $f_{in}$ = 1 MHz (sine wave) (see Figure 7)	2.3 V	-42	
				3 V	-42	
				4.5 V	-42	

(1) Adjust fin voltage to obtain 0 dBm at input.

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<sup>(2)</sup>  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

<sup>(3)</sup>  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .



# **Analog Switch Characteristics (continued)**

 $T_A = 25^{\circ}C$ 

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>cc</sub>	ТҮР	UNIT
				1.65 V	35	.,
Crosstalk	INH	2014	$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	50	
(control input to signal output)	IINI	COM or Y	f <sub>in</sub> = 1 MHz (square wave) (see Figure 8)	3 V	70	mV
				4.5 V	100	
				1.65 V	-60	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	-60	dB
Feedthrough attenuation (switch off)	COM or Y	Y or COM	f <sub>in</sub> = 1 MHz (sine wave) (see Figure 9)	3 V	-60	
				4.5 V	-60	
				1.65 V	-50	
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	2.3 V	-50	
			f <sub>in</sub> = 1 MHz (sine wave) (see Figure 9)	3 V	-50	
				4.5 V	-50	
				1.65 V	0.1%	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	2.3 V	0.025%	
			f <sub>in</sub> = 1 kHz (sine wave) (see Figure 10)	3 V	0.015%	
Cin a construction distantian	COM an V	V == COM		4.5 V	0.01%	
Sine-wave distortion	COM or Y	Y or COM		1.65 V	0.15%	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	2.3 V	0.025%	
			f <sub>in</sub> = 10 kHz (sine wave) (see Figure 10)	3 V	0.015%	
				4.5 V	0.01%	

# 6.8 Operating Characteristics

 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	TYP	UNIT
			9		
	0 50 5 6 40 1415	V <sub>CC</sub> = 2.5 V	10		
$C_{pd}$	C <sub>pd</sub> Power dissipation capacitance	$C_L = 50 \text{ pF, f} = 10 \text{ MHz}$	V <sub>CC</sub> = 3.3 V	10	pF
			V <sub>CC</sub> = 5 V	12	



# 6.9 Typical Characteristics

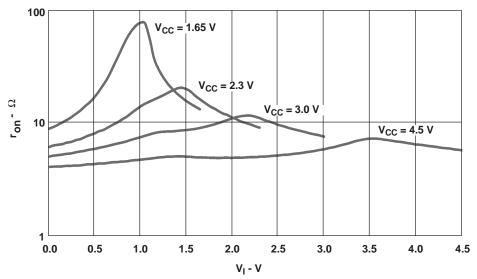


Figure 1. Typical  $r_{on}$  as a Function of Input Voltage (V<sub>I</sub>) for  $V_{I}$  = 0 to  $V_{CC}$ 



# 7 Parameter Measurement Information

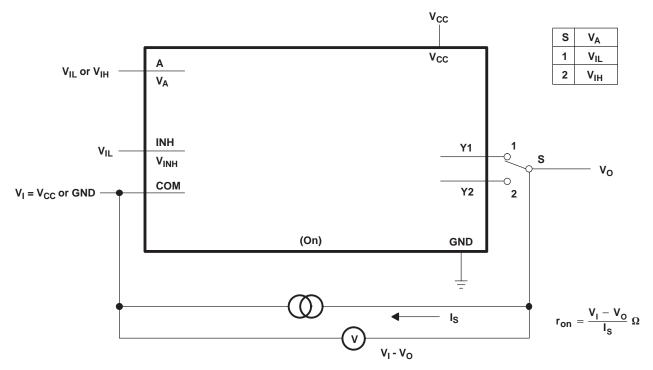


Figure 2. ON-State Resistance Test Circuit

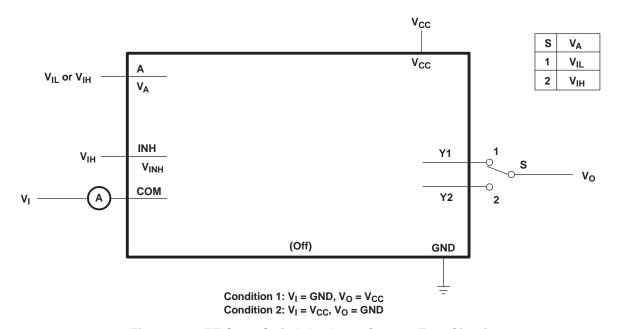


Figure 3. OFF-State Switch Leakage-Current Test Circuit

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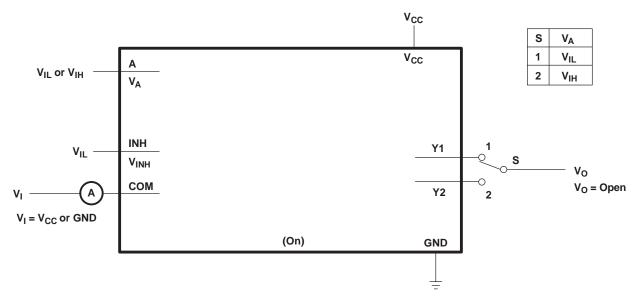
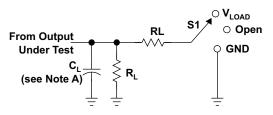


Figure 4. ON-State Switch Leakage-Current Test Circuit

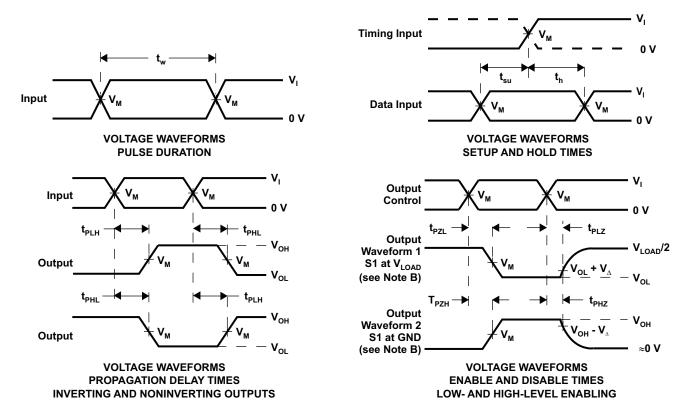




TEST	<b>S1</b>
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

**LOAD CIRCUIT** 

.,	INPUTS		.,	.,	_		.,
V <sub>cc</sub>	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	R <sub>L</sub>	$oldsymbol{V}_{\!\scriptscriptstyle\Delta}$
1.8 V $\pm$ 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	V <sub>cc</sub>	≤ <b>2</b> ns	V <sub>cc</sub> /2	$2 \times \mathbf{V_{cc}}$	30 pF	<b>500</b> Ω	0.15 V
3.3 V $\pm$ 0.3 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>CC</sub>	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>CC</sub>	50 pF	<b>500</b> Ω	0.3 V



NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 Mhz,  $Z_O = 50~\Omega$
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\rm PLZ}$  and  $t_{\rm PHZ}$  are the same as  $t_{\rm dis}$ .
- F.  $t_{\rm PZL}$  and  $t_{\rm PZH}$  are the same as  $t_{\rm en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

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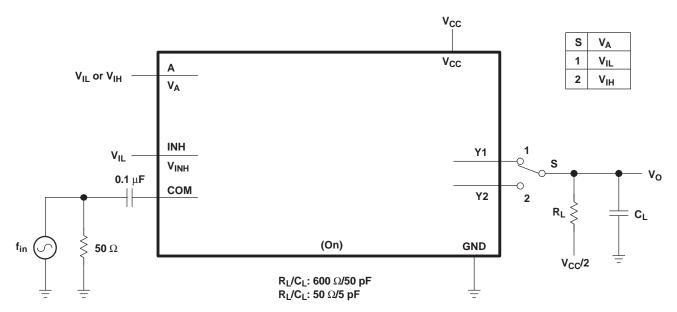


Figure 6. Frequency Response (Switch On)

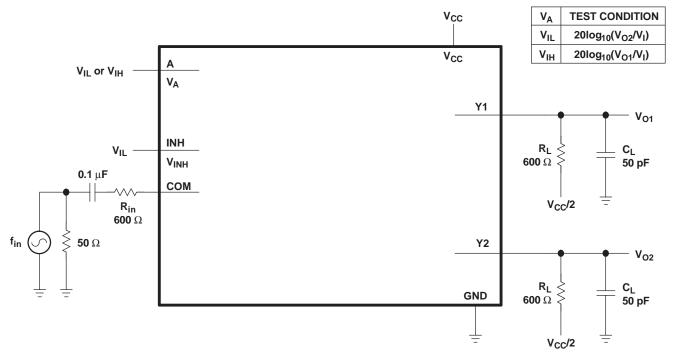


Figure 7. Crosstalk (Between Switches)

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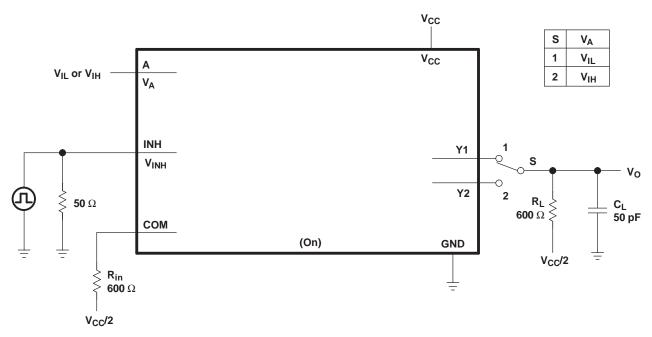


Figure 8. Crosstalk (Control Input, Switch Output)

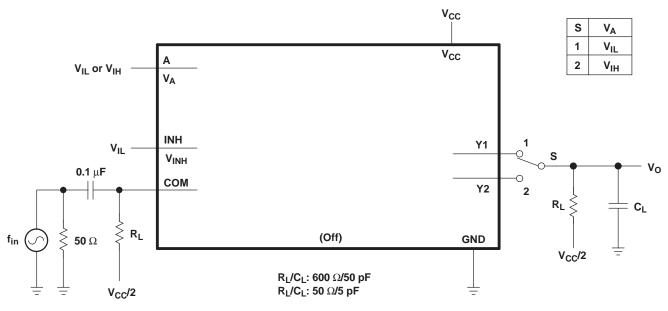


Figure 9. Feedthrough (Switch Off)



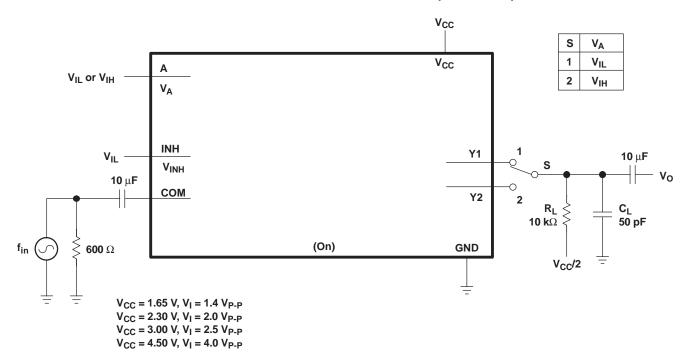


Figure 10. Sine-Wave Distortion



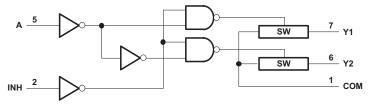
# 8 Detailed Description

#### 8.1 Overview

This dual analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

### 8.2 Functional Block Diagram



NOTE: For simplicity, the test conditions shown in Figure 1 through Figure 4 and Figure 6 through Figure 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

Figure 11. Logic Diagram

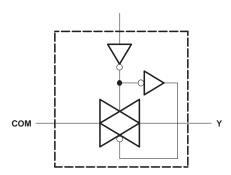


Figure 12. Logic Diagram, Each Switch (SW)

### 8.3 Feature Description

A high-level voltage applied to INH disables the switches. When INH is low, signals can pass from A to Y or Y to A. Low ON-resistance of 6.5  $\Omega$  at 4.5-V V<sub>CC</sub> is ideal for analog signal conditioning systems. The control signals can accept voltages up to 5.5 V without V<sub>CC</sub> connected in the system. Combination of lower t<sub>pd</sub> of 0.8 ns at 3.3 V and low enable and disable time make this part suitable for high-speed signal switching applications.

#### 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G53.

**Table 1. Function Table** 

	TROL UTS	ON CHANNEL
INH	Α	CHANNEL
L	L	Y1
L	Н	Y2
Н	Х	None



## 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC2G53 can be used in any situation where an SPDT switch is required in an application. This switch helps to select one of two signals of which signals can be either digital or analog.

## 9.2 Typical Application

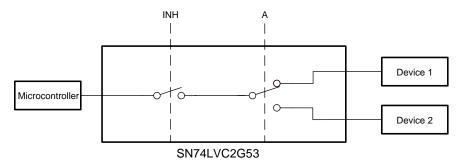


Figure 13. Typical Application Schematic

#### 9.2.1 Design Requirements

The SN74LVC2G53 allows on/off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and  $V_{CC}$  for optimal operation.

#### 9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta v$  in the Recommended Operating Conditions table.
  - For specified high and low levels, see V<sub>IH</sub> and V<sub>IL</sub> in the Recommended Operating Conditions table.
  - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V<sub>CC</sub>.
- 2. Recommended Output Conditions:
  - Load currents should not exceed ±50 mA.
- 3. Frequency Selection Criterion:
  - Maximum frequency tested is 150 MHz.
  - Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

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## **Typical Application (continued)**

#### 9.2.3 Application Curve

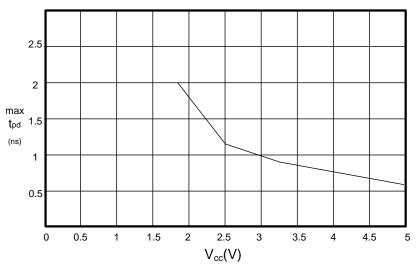


Figure 14. t<sub>pd</sub> vs V<sub>CC</sub>

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* .

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu F$  bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a 0.01- $\mu F$  or 0.022- $\mu F$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu F$  bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu F$  and 1- $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.



# 11 Layout

# 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection.

#### **NOTE**

Not all PCB traces can be straight, and so they will have to turn corners. Figure 15 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

## 11.2 Layout Example

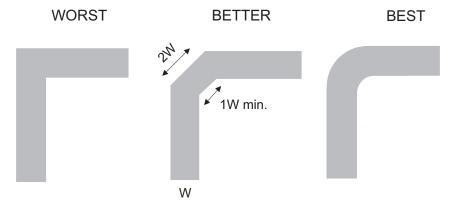


Figure 15. Trace Example

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# 12 Device and Documentation Support

## 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7-Oct-2025

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### **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LVC2G53DCT3	Obsolete	Production	SSOP (DCT)   8	-	-	Call TI	Call TI	-40 to 85	C53 Z
SN74LVC2G53DCTR	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53 Z
SN74LVC2G53DCTR.A	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53 Z
SN74LVC2G53DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53 Z
SN74LVC2G53DCUR	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(53, C53Q, C53R) CZ
SN74LVC2G53DCUR.A	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(53, C53Q, C53R) CZ
SN74LVC2G53DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(53, C53Q, C53R) CZ
SN74LVC2G53DCURG4	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53R
SN74LVC2G53DCURG4.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53R
SN74LVC2G53DCUT	Obsolete	Production	VSSOP (DCU)   8	-	-	Call TI	Call TI	-40 to 85	(53, C53Q, C53R) CZ
SN74LVC2G53DCUTG4	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	C53R
SN74LVC2G53DCUTG4.B	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53R
SN74LVC2G53YZPR	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C4N
SN74LVC2G53YZPR.B	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C4N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.



# **PACKAGE OPTION ADDENDUM**

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G53DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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#### \*All dimensions are nominal

7 til dillionoro dio momina							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G53DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G53DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G53DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G53YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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