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SCES559C - MARCH 2004 - REVISED MARCH 2011

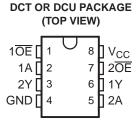
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Check for Samples: SN74LVC2G125-Q1

FEATURES

- Qualified for Automotive Applications
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.3 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation

 Latch-Up Performance Exceeds 100 mA Per JESD 78. Class II



DESCRIPTION/ORDERING INFORMATION

The SN74LVC2G125-Q1 is a dual bus buffer gate designed for 1.65-V to 5.5-V V_{CC} operation. This device features dual line drivers with 3-state outputs. The outputs are disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING (3)
40°C +- 05°C	SSOP - DCT	Tape and reel	CLVC2G125IDCTRQ1	C25
–40°C to 85°C	VSSOP - DCU	Tape and reel	CLVC2G125IDCURQ1	CCW_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE (EACH BUFFER)

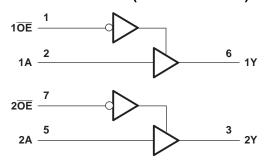
INP	JTS	OUTPUT				
ŌĒ	Α	Y				
L	Н	Н				
L	L	L				
Н	X	Z				



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LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CC}	Supply voltage range		-0.5	6.5	V	
V_{I}	Input voltage range (2)		-0.5	6.5	V	
Vo	Voltage range applied to any output in the high-impedance	-0.5	6.5	V		
Vo	Voltage range applied to any output in the high or low state	-0.5	V _{CC} + 0.5	V		
I_{IK}	Input clamp current	V _I < 0		-50	mA	
I _{OK}	Output clamp current	V _O < 0		- 50	mA	
Io	Continuous output current			±50	mA	
	Continuous current through V _{CC} or GND			±100	mA	
0	Package thermal impedance (4)	DCT package		220	90044	
θ_{JA}	Package thermal impedance 7	DCU package		227	°C/W	
T _{stg}	Storage temperature range	– 65	150	°C		

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

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⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
\/	Supply voltage	Operating	1.65	5.5	V	
V _{CC}	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
.,	High lavel input valtage	V_{CC} = 2.3 V to 2.7 V	1.7		V	
V _{IH}	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$				
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
. ,	Law Israel Sancturality as	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	.,	
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}		
V _I	Input voltage		0	5.5	V	
,	Output walks as	High or low state	0	V _{CC}		
V _O	Output voltage	3-state		5.5	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
l _{он}	High-level output current	V 2.V		-16	mA	
		$V_{CC} = 3 V$		-24		
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V		8		
loL	Low-level output current	V 2 V		16	mA	
		$V_{CC} = 3 V$				
		V _{CC} = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		ns/V		
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5		
T _A	Operating free-air temperature		-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

F	PARAMETER	TEST COM	NDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT	
		$I_{OH} = -100 \ \mu A$		1.65 V to 5.5 V	$V_{CC} - 0.1$				
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
\/		$I_{OH} = -8 \text{ mA}$		2.3 V	1.9			V	
VOH	VOH	$I_{OH} = -16 \text{ mA}$		3 V	2.4			V	
	$I_{OH} = -24 \text{ mA}$		3 V	2.3					
	A or OE inputs	$I_{OH} = -32 \text{ mA}$		4.5 V	3.8				
		$I_{OL} = 100 \mu A$		1.65 V to 5.5 V			0.1		
		I _{OL} = 4 mA		1.65 V		0.45			
V	V _{OL}	$I_{OL} = 8 \text{ mA}$		2.3 V			0.3	V	
VOL		I _{OL} = 16 mA		3 V			0.4		
		I _{OL} = 24 mA		3 V			0.55		
		I _{OL} = 32 mA		4.5 V 0.5			0.55		
I	A or OE inputs	V _I = 5.5 V or GND		0 to 5.5 V			±5	μΑ	
I _{off}		V_I or $V_O = 5.5 \text{ V}$		0			±10	μΑ	
I_{OZ}		V _O = 0 to 5.5 V		3.6 V			10	μΑ	
I_{CC}		$V_I = 5.5 \text{ V or GND},$	I _O = 0	1.65 V to 5.5 V			10	μΑ	
ΔI_{CC}		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 5.5 V			500	μΑ	
_	Data inputs	V V or CND	227	3.5		~F			
C _i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		4	pF			
Co		V _O = V _{CC} or GND		3.3 V		6.5		pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.3		V _{CC} = ± 0.5		UNIT
	(INPOT)	(001P01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	3.3	9.1	1.5	4.8	1.4	4.3	1	3.7	ns
t _{en}	ŌĒ	Υ	4	9.9	1.9	5.6	1.2	4.7	1.2	3.8	ns
t _{dis}	ŌĒ	Y	1.5	11.6	1	5.8	1.4	4.6	1	3.4	ns

Operating Characteristics

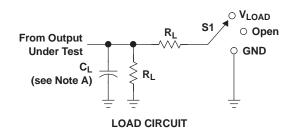
 $T_A = 25^{\circ}$

	PARAMETER			V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	V _{CC} = 5 V TYP	UNIT	
	Power dissipation	Outputs enabled	f 40 MH-	19	19	20	22		
C_{pd}		Outputs disabled	f = 10 MHz	2	2	2	3	pF	

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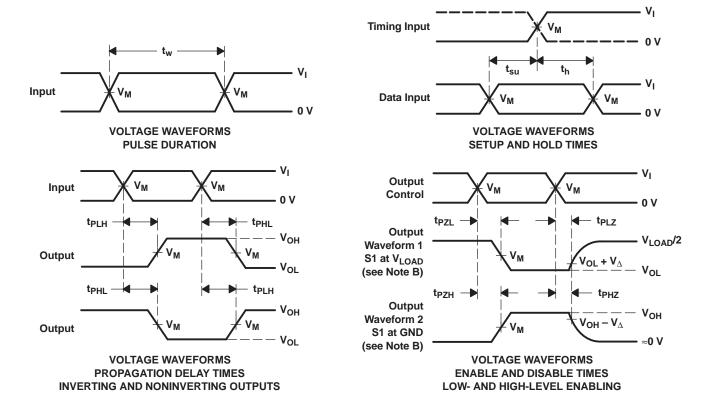


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

V	INF	PUTS	· ·	V	•		
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_{Δ}
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	V_{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
CLVC2G125IDCTRQ1	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C25
			`						Z
CLVC2G125IDCTRQ1.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C25
			(/ / /						Z
CLVC2G125IDCURQ1	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCWR
CLVC2G125IDCURQ1.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCWR

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF SN74LVC2G125-Q1:

● Catalog : SN74LVC2G125

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC2G125IDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC2G125IDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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