

SN74LVC2G08-Q1 Dual 2-Input Positive-AND Gate

1 Features

- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to +125°C Ambient Operating Temperature Range (DCU package)
 - Device Temperature Grade 3: –40°C to +85°C Ambient Operating Temperature Range (DCT package)
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Can be Used as a Down Translator to Translate Input from a Maximum of 5.5 V Down to the V_{CC}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Combine Power Good signals for Muliple Power
- Prevent a Signal from Being Passed Until a Condition is True
- Combine Active-Low Error Signals

3 Description

This dual 2-input positive-AND gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G08-Q1 performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

This device is fully specified for partial-power-down applications using I off. The I off circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G08DCT-Q1	SM8 (8)	2.95 mm × 2.80 mm
SN74LVC2G08DCU-Q1	VSSOP (8)	2.30 mm × 2.00 mm

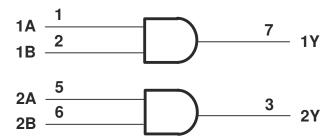


Figure 3-1. Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	nanges from Revision D (March 2010) to Revision E (October 2020)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Removed Typical V_{OLP} (Output Ground Bound) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C from Features section	1
•	Removed Typical V_{OHV} (Output V_{OHV} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C from Features section.	1
•	Removed the Ordering Information table from Description section	1
•	Added a Device Information table to the Description section	1
•	Added the Logic Diagram (Positive Logic) figure to the Description section	1
•	Added the Pin Configuration and Functions section	3
•	Added SN74LVC2G08DCT-Q1 and SN74LVC2G08DCU-Q1 minimum and maximum operating free-air	
	temperature ranges to the Recommended Operating Conditions section	
•	Added the T _A temperature ranges (–40°C to 85°C and –40°C to 125°C) for the t _{pd} parameter to the Switch	
	Characteristics section	
•	Added the Typical Characteristics section	<mark>7</mark>
•	Added the Overview section	9
•	Added the Functional Block Diagram section	9
•	Added the Features Description section	9
•	Added the Device Funcational Modes section	10
•	Added the Application and Implementation section	11
•	Added the Application Information section	11
•	Added the Power Supply Recommendations section	12
•	Added the Layout section	12
•	Added the Layout Guidelines section	12
•	Added the Layout Example section	12
•	Updated the Device and Documentation Support section	13



5 Pin Configuration and Functions

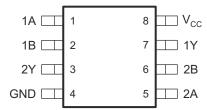


Figure 5-1. DCT Package 8-Pin SM8 Top View

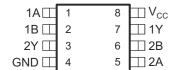


Figure 5-2. DCU Package 8-Pin VSSOP Top View

Pin Functions

PIN		1/0	DESCRIPTION	
NAME	NO.	I/O	DESCRIPTION	
1A	1	I	Channel 1 logic input	
1B	2	I	Channel 1 logic input	
1Y	7	0	Logic level output	
2A	5	I	Channel 2 logic input	
2B	6	I	Channel 2 logic input	
2Y	3	0	Logic level output	
GND	4	_	Ground	
V _{CC}	8	_	Power Supply	



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
VI	Input voltage range ⁽¹⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state ⁽¹⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state ⁽¹⁾ (2)	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current		-50	mA
I _{OK}	Output clamp current		-50	mA
Io	Continuous output current	·	±50	mA
	Continuous current through V _{CC} or GND		±100	mA
TJ	Junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

⁽¹⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
V _(ESD)	discharge	Charged device model (CDM), per AEC Q100-011	±1000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Product Folder Links: SN74LVC2G08-Q1

⁽²⁾ The value of V_{CC} is provided in the *Recommended Operating Conditions* table.



6.3 Recommended Operating Conditions

			MIN	MAX	UNIT		
.,	0	Operating	1.65	5.5			
V_{CC}	Supply voltage	Data retention only	1.5		V		
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}				
.,	Bala Jased Considerable as	V _{CC} = 2.3 V to 2.7 V	1.7		V		
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}				
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}			
	Landard Sound on the ma	V _{CC} = 2.3 V to 2.7 V		0.7	.,		
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V		
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}			
VI	Input voltage		0	5.5	V		
Vo	Output voltage		0	V _{CC}	V		
		V _{CC} = 1.65 V		-4			
		V _{CC} = 2.3 V		-8			
I _{OH}	High-level output current	v		-16	mA		
		$V_{CC} = 3 V$		-24			
		V _{CC} = 4.5 V		-32			
		V _{CC} = 1.65 V		4			
		V _{CC} = 2.3 V		8			
I _{OL}	Low-level output current			16	mA		
		$V_{CC} = 3 V$		24	1		
		V _{CC} = 4.5 V		32			
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20			
Δt/Δν	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		10	ns/V		
		V _{CC} = 5 V ± 0.5 V		5			
_		SN74LVC2G08DCU-Q1	-40	125	00		
T _A	Operating free-air temperature	SN74LVC2G08DCT-Q1	-40	85	°C		

6.4 Thermal Information

		SN74LV		
	THERMAL METRIC(1)	DCT (SM8)	DCU (VSSOP)	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	201.5	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	117.2	91.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100	122.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	42.4	31.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	98.9	122.1	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1			
		I _{OH} = -4 mA	1.65 V	1.2			
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		I _{OH} = -8 mA	2.3 V	1.9			V
V _{OH}		I _{OH} = -16 mA	3 V	2.4			V
		I _{OH} = -24 mA	3 V	2.3			
		I _{OH} = -32 mA	4.5 V	3.8			
		I _{OL} = 100 μA	1.65 V to 5.5 V			0.1	
		I _{OL} = 4 mA	1.65 V			0.45	
,,		I _{OL} = 8 mA	2.3 V			0.3	v
V _{OL}	V _{OL}	I _{OL} = 16 mA	234			0.4	V
		I _{OL} = 24 mA	- 3 V			0.55	
		I _{OL} = 32 mA	4.5 V			0.55	
I _I	A or B inputs	V _I = 5.5 V or GND	0 to 5.5 V			±5	μΑ
I _{off}		V _I or V _O = 5.5 V	0			±10	μΑ
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10	μΑ
ΔI _{CC}		One input at $V_{CC} = 0.6 \text{ V}$, Other inputs at V_{CC} or GND, $T_A = -40^{\circ}\text{C}$ to 85°C	3 V to 5.5 V			500	μΑ
Ci		$V_1 = V_{CC}$ or GND, $T_A = -40^{\circ}$ C to 85°C	3.3 V		5		pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A	V _{cc}	MIN	MAX	UNIT							
				V _{CC} = 1.8 V ± 0.15 V	2.6	9								
			–40°C to 85°C	V _{CC} = 2.5 V ± 0.2 V	1	5.1								
		Υ	Υ	Y	Y		V _{CC} = 3.3 V ± 0.3 V	1	4.7					
	A or B						Υ		V		V _{CC} = 5 V ± 0.5 V	1	3.8	ns
t _{pd}	AOIB								4000 to 40500	V _{CC} = 1.8 V ± 0.15 V	2.6	9.8	115	
										V _{CC} = 2.5 V ± 0.2 V	1	5.8		
			-40 C to 125 C	V _{CC} = 3.3 V ± 0.3 V	1	5.3								
				V _{CC} = 5 V ± 0.5 V	1	4.8								

6.7 Operating Characteristics

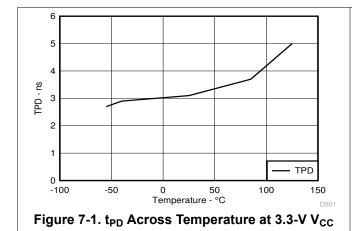
 $T_A = 25^{\circ}C$

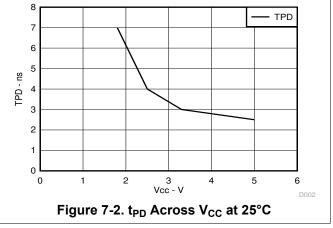
PARAMETER TEST CONDITIONS V _{CC} = 1.8 V V _C		V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT		
	TANAMETER	TEST SONDITIONS	TYP	TYP	TYP	TYP	ONT
C_{pd}	Power dissipation capacitance	f = 10 MHz	17	17	17	20	pF

Product Folder Links: SN74LVC2G08-Q1



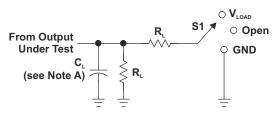
7 Typical Characteristics







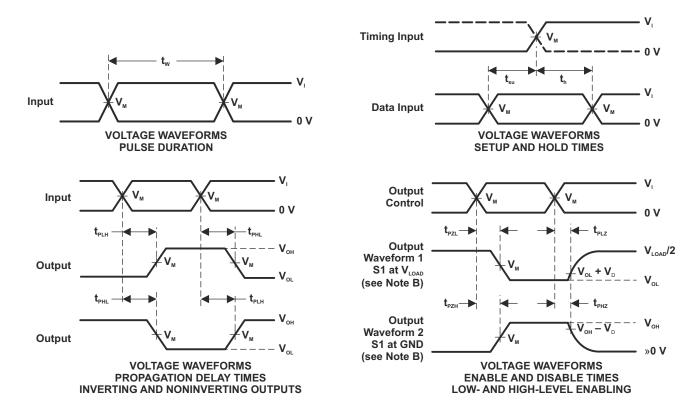
8 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
$\mathbf{t}_{\scriptscriptstyle{\mathrm{PLZ}}}/\mathbf{t}_{\scriptscriptstyle{\mathrm{PZL}}}$	V _{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

.,	INPUTS		.,	.,		_	.,	
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C	R _⊾	V _D	
1.8 V ± 0.15 V	V _{cc}	£2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 kW	0.15 V	
2.5 V ± 0.2 V	V_{cc}	£2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 W	0.15 V	
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V	
5 V ± 0.5 V	V _{cc}	£2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 W	0.3 V	



NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, $Z_0 = 50$ W.
- D. The outputs are measured one at a time, with one transition per measurement.

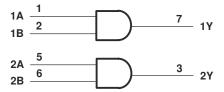
Figure 8-1. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LVC2G08-Q1 device contains two 2-input positive AND gates and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$. This device is fully specified for partial-power-down applications using loff. The loff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

9.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in Implications of Slow or Floating CMOS Inputs.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10-k Ω resistor is recommended and will typically meet all requirements.

9.3.3 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in Figure 9-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



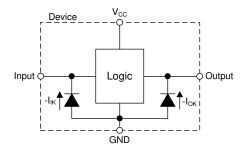


Figure 9-1. Electrical Placement of Clamping Diodes for Each Input and Output

9.3.4 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

9.4 Device Functional Modes

Table 9-1 lists the functional modes of the SN74LVC2G08-Q1.

Table 9-1. Function Table

INP	UTS	OUTPUT
Α	В	Y
Н	Н	Н
L	X	L
X	L	L

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVC2G08-Q1 is a high-drive CMOS device that can be used for implementing AND logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V, making it Ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC} .

10.2 Typical Application

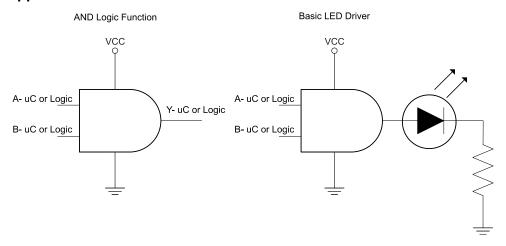


Figure 10-1. Typical Application

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

10.2.1.1 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs. See (Δt/ΔV) in the Recommended Operating Conditions table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I maximum) in the Recommended
 Operating Conditions table at any valid V_{CC}.
- 2. Recommended Output Conditions
 - Load currents must not exceed (I_O maximum) per output and must not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Recommended Operating Conditions* table.
 - Outputs must not be pulled above V_{CC} in normal operating conditions.

11 Application Curves

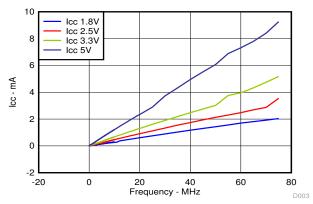


Figure 11-1. I_{CC} vs Frequency

12 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table. Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} pins then 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results

13 Layout

13.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

13.2 Layout Example



Figure 13-1. Layout Example

14 Device and Documentation Support

14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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14.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

14.4 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

14.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LVC2G08IDCTRQ1	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C08 Z
SN74LVC2G08IDCTRQ1.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C08 Z
SN74LVC2G08QDCURQ1	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HLRQ
SN74LVC2G08QDCURQ1.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HLRQ

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF SN74LVC2G08-Q1:

◆ Catalog : SN74LVC2G08

● Enhanced Product : SN74LVC2G08-EP

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 13-Dec-2020

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G08QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74LVC2G08QDCURQ1	VSSOP	DCU	8	3000	183.0	183.0	20.0	





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







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 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

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