

# SNx4LVC257A Quadruple 2-Line to 1-Line Data Selectors and **Multiplexers With 3-State Outputs**

### 1 Features

- Operate from 1.65V to 3.6V
- Inputs accept voltages to 5.5V
- Maximum t<sub>pd</sub> of 4.6ns at 3.3V
- Typical V<sub>OLP</sub> (output ground bounce) <0.8V at  $V_{CC} = 3.3V$ ,  $T_A = 25^{\circ}C$
- Typical V<sub>OHV</sub> (output V<sub>OH</sub> undershoot) >2V at  $V_{CC}$  = 3.3V,  $T_A$  = 25°C
- Latch-up performance exceeds 250mA per JESD
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114-A)
  - 200V machine model (A115-A)
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# 2 Applications

- **Cable Modem Termination Systems**
- Tests and Measurements
- I/O Expanders
- **Motor Drivers**
- **Network Switches**
- Servers
- Telecom Infrastructure

## 3 Description

These quadruple 2-line to 1-line data selectors and multiplexers are designed for 1.65V to 3.6V V<sub>CC</sub> operation.

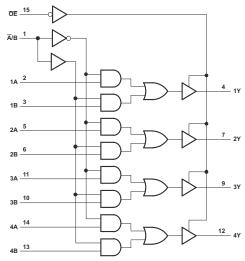
The SNx4LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (  $\overline{OE}$ ) input is at a high logic level.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V or 5V system environment.

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE(2)	BODY SIZE(3)
	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC, 16)	9.90 mm × 6mm	9.90 mm × 3.90 mm
SNx4LVC257A	DB (SSOP, 16)	6.20 mm × 7.8mm	6.20 mm × 5.30 mm
SINAHEVOZSTA	NS (SOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP, 16)	5.00 mm × 6.4mm	5.00 mm × 4.40 mm
	RGY (VQFN, 16)	4mm × 3.5mm	4mm × 3.5mm

- For more information, see Mechanical, Packaging, and Orderable Information.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.

Logic Diagram (Positive Logic)



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# **4 Pin Configuration and Functions**

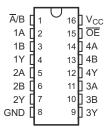


Figure 4-1. D, DB, NS, J, W, or PW Package; 16-Pin SOIC, SSOP, SO, CDIP, CFP, or TSSOP (Top View)

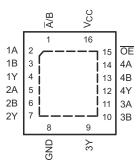


Figure 4-2. BQB or RGY Package; 16-Pin WQFN or VQFN with Exposed Thermal Pad (Top View)

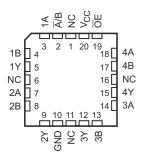


Figure 4-3. FK Package, 20-Pin LCCC Top View

	PIN			
NAME	SOIC, SSOP, SO, CDIP, CFP, TSSOP, WQFN, or VQFN	LCCC	I/O	DESCRIPTION
Ā/B	1	2	I	Select Pin, Low selects A, High selects B
1A	2	3	I/O	Multiplexer Signal Input
1B	3	4	I/O	Multiplexer Signal Input
1Y	4	5	I/O	Multiplexer Output
2A	5	7	I/O	Multiplexer Signal Input
2B	6	8	I/O	Multiplexer Signal Input
2Y	7	9	I/O	Multiplexer Output
3A	11	14	I/O	Multiplexer Signal Input
3B	10	13	I/O	Multiplexer Signal Input
3Y	9	12	I/O	Multiplexer Output
4A	14	18	I/O	Multiplexer Signal Input
4B	13	17	I/O	Multiplexer Signal Input
4Y	12	15	I/O	Multiplexer Output
GND	8	10		Ground
NC <sup>(1)</sup>	_	1, 6, 11, 16		No connect
ŌĒ	15	19	I/O	Active low Output enable
V <sub>CC</sub>	16	20	_	Power pin

(1) NC - no internal connection



## **5 Specifications**

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage			-0.5	6.5	V
VI	Input voltage <sup>(2)</sup>			-0.5	6.5	V
Vo	Output voltage <sup>(2) (3)</sup>			-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> <	< 0		-50	mA
I <sub>OK</sub>	Output clamp current	Vo	< 0		-50	mA
Io	Continuous output current				±50	mA
	Continuous current through V <sub>CC</sub> or C	GND			±100	mA
T <sub>stg</sub>	Storage temperature			-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.

## 5.2 ESD Ratings

			VALUE	UNIT
	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
V <sub>(ESD)</sub>	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)(1)

			SN54LVC	SN54LVC257A SN74LVC257A			
			MIN	MAX	MIN	MAX	UNIT
\/	Cumply voltage	Operating	2	3.6	1.65	3.6	V
$V_{CC}$	Supply voltage	Data retention only	1.5		1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V			0.65 × V <sub>CC</sub>		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V			1.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		2		
		V <sub>CC</sub> = 1.65 V to 1.95 V				0.35 × V <sub>CC</sub>	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V				0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		0.8	
VI	Input voltage		0	5.5	0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V				-4	
	High-level output current	V <sub>CC</sub> = 2.3 V				-8	mA
I <sub>OH</sub>	riigri-ievei output current	V <sub>CC</sub> = 2.7 V		-12		-12	ША
		V <sub>CC</sub> = 3 V		-24		-24	
		V <sub>CC</sub> = 1.65 V				4	
	I I I I I I I I	V <sub>CC</sub> = 2.3 V				8	mΛ
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		12		12	mA
ı		V <sub>CC</sub> = 3 V		24		24	

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over operating free-air temperature range (unless otherwise noted)(1)

		SN54LVC257A SN74LVC257A		UNIT			
		MIN	MAX			ONII	
Δt/Δν	Input transition rise or fall rate		10		10	ns/V	
T <sub>A</sub>	Operating free-air temperature	<b>–</b> 55	125	-40	85	°C	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

#### 5.4 Thermal Information

	SN74LVC257A							
THERMAL METRIC(1)		BQB (WQFN)         D (SOIC)         DB (SSOP)         NS (SO)         PW (TSSOP)				RGY (VQFN)	UNIT	
		16 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.8	118.1	82	64	141.8	87.1	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

#### 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	.,	SN54	LVC257	A	SN74	LVC257	١	LINIT
PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	UNIT
	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V				V <sub>CC</sub> - 0.2			
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	2.7 V to 3.6 V	V <sub>CC</sub> - 0.2						
	$I_{OH} = -4 \text{ mA}$	1.65 V				1.2			
	$I_{OH} = -8 \text{ mA}$	2.3 V				1.7			V
	I = 10 mA	2.7 V	2.2			2.2			
	I <sub>OH</sub> = -12 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = -24 mA	3 V	2.2			2.2			
	1 - 100	1.65 V to 3.6 V						0.2	
	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V			0.2				
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	I <sub>OL</sub> = 4 mA	1.65 V						0.45	V
V <sub>OL</sub>	I <sub>OL</sub> = 8 mA	2.3 V						0.7	
	I <sub>OL</sub> = 12 mA	2.7 V			0.4			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5			±5	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±15			±10	μA
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			10			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500			500	μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		5			5		pF
Co	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5			5		pF

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.



# 5.6 Switching Characteristics, SN54LVC257A

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			;				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2	2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
4	A or B	· ·		5.4	1	4.6	
t <sub>pd</sub>	d Ā/B	1		7.5	1	6.4	ns
t <sub>en</sub>	ŌĒ	Y		6.7	1	5.6	ns
t <sub>dis</sub>	ŌĒ	Y		4.7	0.5	4.3	ns
t <sub>sk(o)</sub>						1	ns

# 5.7 Switching Characteristics, SN74LVC257A

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

					;	SN74LV	/C257A				
PARAMETER	AMETER FROM TO (OUTPUT)		V <sub>CC</sub> = 1.8 V V <sub>CC</sub> = 2.5 V ± 0.15 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
4	A or B	Y	1	13.5	1	7.4	1	5.4	1	4.6	
t <sub>pd</sub>	Ā/B	1	1	15.6	1	9.5	1	7.5	1	6.4	ns
t <sub>en</sub>	ŌĒ	Y	1	14.6	1	8.7	1	6.7	1	5.6	ns
t <sub>dis</sub>	ŌĒ	Y	1	15.4	1	6.7	1	4.7	1	4.3	ns
t <sub>sk(o)</sub>										1	ns

# **5.8 Operating Characteristics**

 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT	
	17110111121211	1201 001121110110	TYP	TYP	TYP	Oitii	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	13.5	14.5	15.5	pF	



# **5.9 Typical Characteristics**

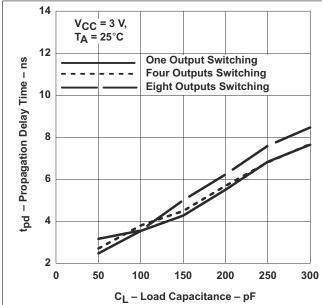


Figure 5-1. Propagation Delay (Low to High Transition)
vs Load Capacitance

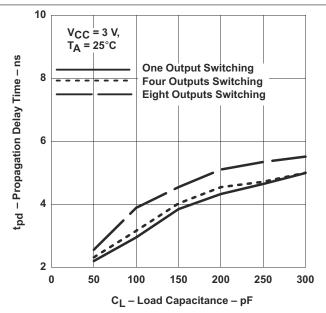
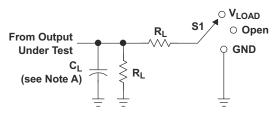


Figure 5-2. Propagation Delay (High to Low Transition)
vs Load Capacitance



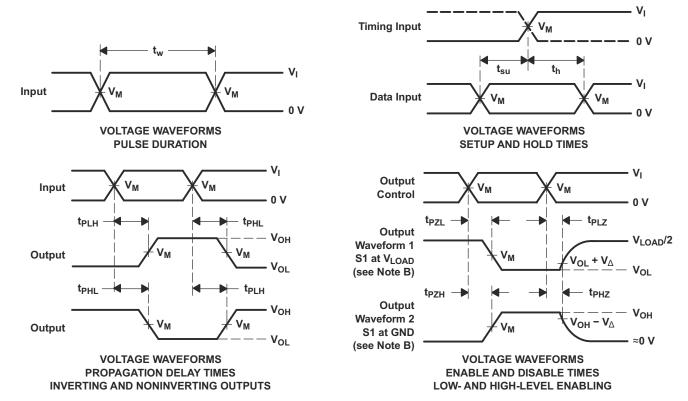
### **6 Parameter Measurement Information**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

	AD	$\sim$ 1	п	$\sim$	ш	T
LU	ΆU	u	ĸ	U	U	ш

.,	INF	PUTS	.,	V			V	
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	$R_L$	$V_{\triangle}$	
1.8 V±0.15 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V	
2.5 V±0.2 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	<b>500</b> Ω	0.15 V	
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V	
3.3 V±0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V	



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristcs: PRR ≤10 MHz, Z <sub>O</sub> = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measuremert.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>od</sub>.
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms



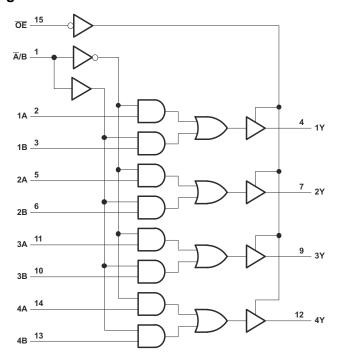
# 7 Detailed Description

### 7.1 Overview

These quadruple 2-line to 1-line data selectors and multiplexers are designed for 1.65-V to 3.6-V V<sub>CC</sub> operation.

The SNx4LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ( $\overline{OE}$ ) input is at a high logic level.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V and 5-V system environment. Device features a maximum  $t_{pd}$  of 4.6 ns allowing the device to be used in high-speed applications as well.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### 7.4 Device Functional Modes

Table 7-1 lists the functional modes for the SN54LVC257A and SN74LVC257A devices.

**INPUTS OUTPUT** Υ <u>OE</u> A/B Α В Н Χ Χ Χ Ζ L L Χ L Н Х Н L L Н Х L L L L Н Χ Н Н

**Table 7-1. Function Table** 

# **Application and Implementation**

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## **1 Application Information**

The SNx4LVC257A devices are useful for digital signal data selector or multiplexer applications.

### **2 Typical Application**

The SNx4LVC257A devices use CMOS technology and have balanced output drive. These devices can be used for down level translation and multiplexer function as shown in Figure 8-1.

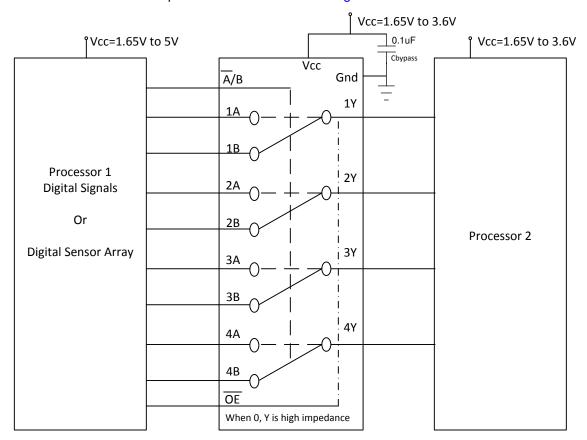


Figure 8-1. SNx4LVC257A Used as Level Translation and as a Multiplexer

## 2.1 Design Requirements

Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

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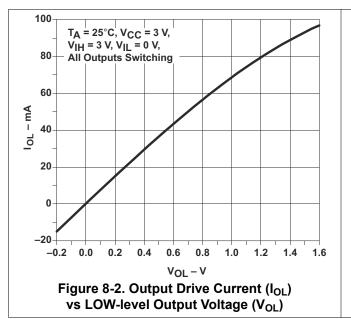
#### 2.2 Detailed Design Procedure

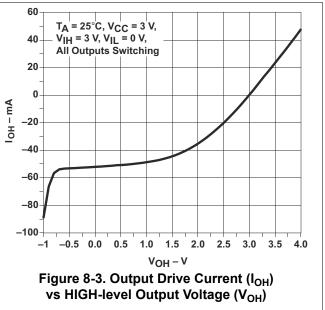
- 1. Recommended Input Conditions
  - For rise time and fall time specification, see ( $\Delta t/\Delta V$ ) in the Section 5.3 table.
  - For specified high and low levels, see (V<sub>IH</sub> and V<sub>IL</sub>) in the Section 5.3 table.
  - Inputs are over voltage tolerant allowing them to go as high as (V<sub>I</sub> max) in the Section 5.3 table at any valid V<sub>CC</sub>.

## 2. Recommend Output Conditions

- Load currents must not exceed (I<sub>O</sub> max) per output and must not exceed (continuous current through V<sub>CC</sub> or GND) total current for the part. These limits are in the Section 5.3 table.
- Outputs must not be pulled above V<sub>CC</sub>.

#### 2.3 Application Curves





#### 3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 5.3 table.

Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01- $\mu$ F or 0.022- $\mu$ F capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

#### 4 Layout

#### 4.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-4 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.



### 4.2 Layout Example

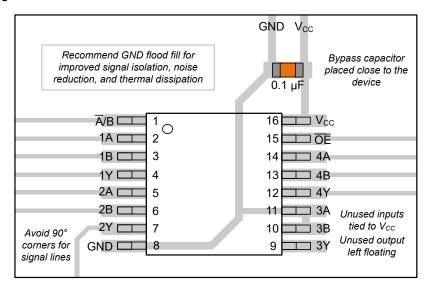


Figure 8-4. Example Layout for the SN74LVC257A



# 8 Device and Documentation Support

## 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

#### 8.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER SAMPLE & B		TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN54LVC257A	Click here	Click here	Click here	Click here	Click here	
SN74LVC257A	Click here	Click here	Click here	Click here	Click here	

#### 8.2 Community Resources

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

# Changes from Revision P (May 2024) to Revision Q (December 2024)

Page

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C	hanges from Revision O (June 2015) to Revision P (May 2024)	Page
•	Added BQA package to Package Information table, Pin Configuration and Functions section, and Th	ermal
	Information table	1
•	Added package size to Device Information table and deleted Device Options table table	1

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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8-Nov-2025

# **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-0050901QFA	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050901QF A SNJ54LVC257AW
SN74LVC257ABQBR	Active	Production	WQFN (BQB)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC257A
SN74LVC257ABQBR.A	Active	Production	WQFN (BQB)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC257A
SN74LVC257AD	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257AD.B	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADBR	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257ADBR.B	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257ADR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADR.B	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADRG4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ANSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ANSR.B	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257APW	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APW.B	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWR	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWR.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWRG4	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWRG4.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWT	Active	Production	TSSOP (PW)   16	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWT.B	Active	Production	TSSOP (PW)   16	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257ARGYR	Active	Production	VQFN (RGY)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A
SN74LVC257ARGYR.A	Active	Production	VQFN (RGY)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A
SN74LVC257ARGYR.B	Active	Production	VQFN (RGY)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A
SNJ54LVC257AW	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050901QF A SNJ54LVC257AW

# PACKAGE OPTION ADDENDUM

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- (1) Status: For more details on status, see our product life cycle.
- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54LVC257A, SN74LVC257A:

Catalog: SN74LVC257A

Automotive: SN74LVC257A-Q1, SN74LVC257A-Q1

Enhanced Product: SN74LVC257A-EP, SN74LVC257A-EP

Military: SN54LVC257A

NOTE: Qualified Version Definitions:



# PACKAGE OPTION ADDENDUM

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- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications



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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC257ABQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74LVC257ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC257ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC257ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC257ABQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74LVC257ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LVC257ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LVC257ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LVC257APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC257APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC257APWT	TSSOP	PW	16	250	353.0	353.0	32.0
SN74LVC257ARGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-0050901QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LVC257AD	D	SOIC	16	40	507	8	3940	4.32
SN74LVC257AD.B	D	SOIC	16	40	507	8	3940	4.32
SN74LVC257APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC257APW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54LVC257AW	W	CFP	16	25	506.98	26.16	6220	NA

# D (R-PDS0-G16)

# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# W (R-GDFP-F16)

# CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



# RGY (R-PVQFN-N16)

## PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



# RGY (R-PVQFN-N16)

# PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.





SOP



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



## NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



#### NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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