











SN74LVC1G86

SCES222Q - APRIL 1999 - REVISED JUNE 2017

# SN74LVC1G86 Single 2-Input Exclusive-OR Gate

### **Features**

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- Qualified from -40°C to +125°C
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Are Over Voltage Tolerant up to 5.5 V
- Supports Down Translation to V<sub>CC</sub>
- Maximum t<sub>pd</sub> of 4 ns at 3.3 V and 15-pF load
- Low Power Consumption, 10-µA Maximum I<sub>CC</sub> At
- ±24-mA Output Drive at 3.3 V
- Ioff Supports Partial-Power-Down Mode, and Back-**Drive Protection**
- Available in the Texas Instruments NanoFree™ Package
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

# **Applications**

- Wireless Headsets
- Motor Drives and Controls
- TVs
- Set-Top Boxes
- Audio

# 3 Description

The SN74LVC1G86 device performs the Boolean function  $Y = \overline{AB} + A\overline{B}$  in positive logic. This single 2input exclusive-OR gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output. This device has low power consumption with maximum t<sub>pd</sub> of 4 ns at 3.3 V and 15-pF capacitive load. The maximum output drive is ±32-mA at 4.5 V and ±24-mA at 3.3 V.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$  . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current back flow through the device when it is powered down.

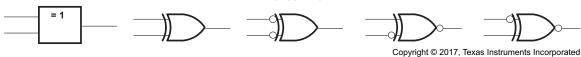
#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)				
SN74LVC1G86DBV	SOT-23 (5)	2.90 mm × 1.60 mm				
SN74LVC1G86DCK	SC70 (5)	2.00 mm × 1.25 mm				
SN74LVC1G86DRL	SOT (5)	1.60 mm × 1.20 mm				
SN74LVC1G86YZP	DSBGA (5)	1.44 mm × 0.94 mm				

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### **Functional Block Diagram**

**EXCLUSIVE OR** 



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.



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# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

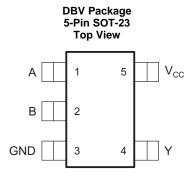
Changes from Revision P (September 2015) to Revision Q	Page
Changed YZP (DSBGA) package pinout diagram and added DSBGA column	3
<ul> <li>Added Balanced High-Drive CMOS Push-Pull Outputs, Standard CMOS Inputs, Clamp Diodes, Partial Powe (I<sub>off</sub>), and Over-voltage Tolerant Inputs sections.</li> </ul>	
Changes from Revision O (December 2013) to Revision P	Page

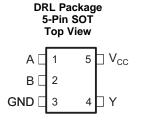
Added Applications section, Device Information table, ESD Ratings table, Thermal Information table, Typical
Characteristics section, Feature Description section, Device Functional Modes, Application and Implementation
section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and
Mechanical, Packaging, and Orderable Information section

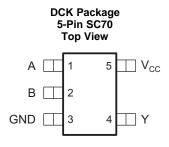
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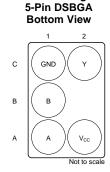
# 5 Pin Configuration and Functions







YZP Package



# Pin Functions<sup>(1)</sup>

	PIN		I/O	DESCRIPTION
NAME	DBV, DRL, DCK	DSBGA	1/0	DESCRIPTION
Α	1	A1	I	Input A
В	2	B1	I	Input B
GND	3	C1	_	Ground
$V_{CC}$	5	A2	_	Positive Supply
Υ	4	C2	0	Output Y

(1) See mechanical drawings for dimensions.



# 6 Specifications

# 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		-0.5	6.5	V
VI	Input voltage (2)	-0.5	6.5	V	
Vo	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V	
Vo	Voltage applied to any output in the high or low state (2)(3)	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

				VALUE	UNIT
,	., Electrostatic	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	
1	V <sub>(ESD)</sub>	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT				
.,	Complement	Operating	1.65	5.5	V				
$V_{CC}$	Supply voltage	Data retention only	1.5		V				
	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>						
١,,		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V <sub>CC</sub> = 2.3 V to 2.7 V 1.7						
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V				
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.7 × V <sub>CC</sub>						
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>					
\/	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	.,,				
$V_{IL}$		V <sub>CC</sub> = 3 V to 3.6 V		0.8	V				
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		0.3 × V <sub>CC</sub>					
VI	Input voltage		0	5.5	V				
Vo	Output voltage		0	V <sub>CC</sub>	V				
		V <sub>CC</sub> = 1.65 V		-4					
		V <sub>CC</sub> = 2.3 V		-8					
$I_{OH}$	High-level output current			-16	mA				
		V <sub>CC</sub> = 3 V		-24					
		V <sub>CC</sub> = 4.5 V		-32					

 All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs, SCBA004.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(3)</sup> The value of  $V_{CC}$  is provided in the Recommended Operating Conditions table.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



# **Recommended Operating Conditions (continued)**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current $V_{CC} = 3 \text{ V}$	V - 3 V		16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	
т	Operating free cir temperature	YZP package	-40	85	9
T <sub>A</sub>	Operating free-air temperature	DCK, DBV, and DRL packages	-40	125	°C

# 6.4 Thermal Information

			SN74LVC1G86			
	THERMAL METRIC <sup>(1)</sup>	DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	UNIT	
		5 PINS	5 PINS	5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	132	°C/W	

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	ONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
	$I_{OH} = -100 \mu A$			1.65 V to 5.5 V	$V_{CC} - 0.1$			
	$I_{OH} = -4 \text{ mA}$			1.65 V	1.2			
V	$I_{OH} = -8 \text{ mA}$			2.3 V	1.9			V
V <sub>OH</sub>	$I_{OH} = -16 \text{ mA}$			2.1/	2.4			V
	$I_{OH} = -24 \text{ mA}$			3 V	2.3			
	$I_{OH} = -32 \text{ mA}$			4.5 V	3.8			
	I <sub>OL</sub> = 100 μA			1.65 V to 5.5 V			0.1	
V <sub>OL</sub>	I <sub>OL</sub> = 4 mA			1.65 V			0.45	
	$I_{OL} = 8 \text{ mA}$			2.3 V			0.3	V
	I <sub>OL</sub> = 16 mA			2.1/			0.4	V
	$I_{OL} = 24 \text{ mA}$			3 V			0.55	
	$I_{OL}$ = 32 mA			4.5 V	0.55			
I <sub>I</sub> A or B input	$V_I = 5.5 \text{ V or GND}$			0 to 5.5 V			±5	μΑ
I <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$			0			±10	μΑ
	V V as CND	I <sub>O</sub> = 0	-40°C to 85°C	4.05.7/+- 5.5.7/			10	
ICC	$I_{CC}$ $V_I = V_{CC}$ or GND,		-40°C to 125°C	1.65 V to 5.5 V			15	μA
Δl <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND			3 V to 5.5 V			500	μA
C <sub>i</sub>	$V_I = V_{CC}$ or GND			3.3 V		6		pF

(1) All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.



# 6.6 Switching Characteristics, $C_L = 15 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETE	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub> = 1 ± 0.15		V <sub>CC</sub> = ± 0.2		V <sub>CC</sub> = 3 ± 0.3		V <sub>CC</sub> = ± 0.		UNIT
K	(INFUT)	(001701)		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Υ	$T_A = -40$ °C to +85°C	2.1	9.1	1	4.5	0.6	4	8.0	3.3	ns

# 6.7 Switching Characteristics, $C_L = 30 \text{ pF}$ or 50 pF

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub> = 1 ± 0.1		V <sub>CC</sub> = ± 0.2		V <sub>CC</sub> = 3 ± 0.3		V <sub>CC</sub> = ± 0.5		UNIT
	(INPOT)	(OUTPUT)		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Δ or B	A or B Y	-40°C to +85°C temperature range, see Figure 2	3.5	9.9	1.8	5.5	1.3	5	1	4	20
	AOIB	ı	-40°C to +125°C temperature range, see Figure 2	3.5	12	1.8	7	1.3	6	1	5	ns

# 6.8 Operating Characteristics

 $T_A = 25^{\circ}C$ 

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	$V_{CC} = 2.5 V$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 V$	UNIT	
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	22	22	22	24	pF	

# 6.9 Typical Characteristics

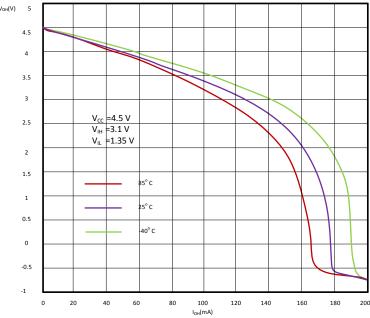
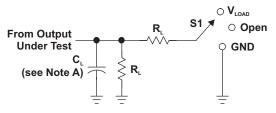


Figure 1. V<sub>oh</sub> vs I<sub>oh</sub> at 4.5 V



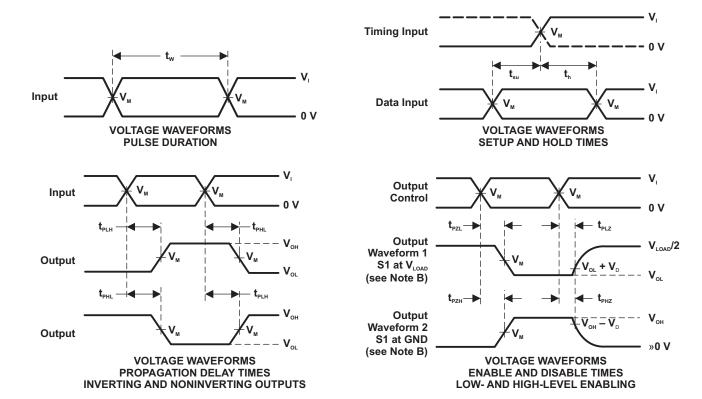
### 7 Parameter Measurement Information



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

.,	INI	PUTS	V	V		Б	V	
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	V <sub>LOAD</sub>	C	$R_{\scriptscriptstyle L}$	V <sub>D</sub>	
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 Μ</b> Ω	0.15 V	
2.5 V ± 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 Μ</b> Ω	0.15 V	
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	<b>1 Μ</b> Ω	0.3 V	
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 Μ</b> Ω	0.3 V	



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\mbox{\tiny PLZ}}$  and  $\dot{t}_{\mbox{\tiny PHZ}}$  are the same as  $t_{\mbox{\tiny dis}}.$
- F.  $t_{\mbox{\tiny PZL}}$  and  $t_{\mbox{\tiny PZH}}$  are the same as  $t_{\mbox{\tiny en}}.$
- G.  $t_{\mbox{\tiny PLH}}$  and  $t_{\mbox{\tiny PHL}}$  are the same as  $t_{\mbox{\tiny od}}$
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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## 8 Detailed Description

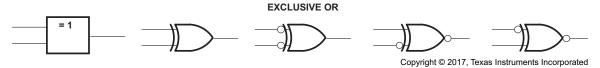
#### 8.1 Overview

The SN74LVC1G86 device performs the Boolean function  $Y = \overline{A}B + A\overline{B}$  in positive logic. This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

A common application is as a true and complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package. This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram



These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.

## 8.3 Feature Description

### 8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Recommended Operating Conditions*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in *Recommended Operating Conditions* to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

Product Folder Links: SN74LVC1G86

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# **Feature Description (continued)**

## 8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

## **CAUTION**

Avoid any voltage below or above the input or output voltage specified in the *Absolute Maximum Ratings*. In this event, the current must be limited to the maximum input or output clamp current value indicated in the *Absolute Maximum Ratings* to avoid damage to the device.

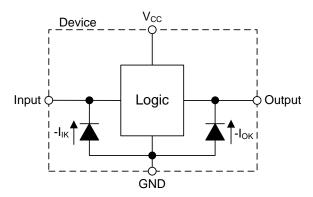


Figure 3. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.3.4 Partial Power Down (I<sub>off</sub>)

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I<sub>off</sub> in the *Electrical Characteristics*.

### 8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

## 8.4 Function Table

Table 1 lists the functional modes of the SN74LVC1G86 device.

**Table 1. Function Table** 

INP	UTS	OUTPUT
Α	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L



# 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

# 9.1 Application Information

The SN74LVC1G86 device can accept input voltages up to 5.5~V at any valid  $V_{CC}$  which makes the device suitable for down translation. This feature of the SN74LVC1G86 makes it ideal for various bus interface applications.

# 9.2 Typical Application

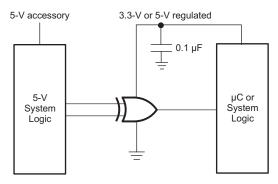


Figure 4. Typical Application Schematic

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the *Recommended Operating Conditions* table.
  - For specified High and low levels, see V<sub>IH</sub> and V<sub>II</sub> in the *Recommended Operating Conditions* table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V<sub>CC</sub>.
- 2. Recommended Output Conditions
  - Load currents should not exceed 32 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V<sub>CC</sub>.

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# **Typical Application (continued)**

## 9.2.3 Application Curve

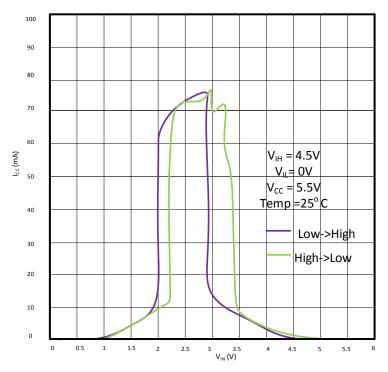


Figure 5. I<sub>CC</sub> vs. V<sub>IN</sub>

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu F$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu F$  or 0.022  $\mu F$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1- $\mu F$  and 1- $\mu F$  are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

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# 11 Layout

# 11.1 Layout Guidelines

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 6 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 11.2 Layout Example

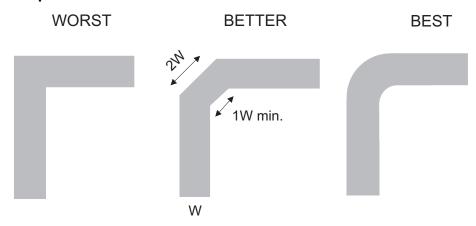


Figure 6. Trace Example

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# 12 Device and Documentation Support

## 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

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TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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7-Oct-2025

# **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G86DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C865, C86F, C86J, C86K, C86R)
SN74LVC1G86DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C865, C86F, C86J, C86K, C86R)
SN74LVC1G86DBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C865, C86F, C86J, C86K, C86R)
SN74LVC1G86DBVRE4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C86F
SN74LVC1G86DBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C86F
SN74LVC1G86DBVRG4.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C86F
SN74LVC1G86DBVT	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C865, C86F, C86J, C86K, C86R)
SN74LVC1G86DBVT.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C865, C86F, C86J, C86K, C86R)
SN74LVC1G86DCKR	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CH5, CHF, CHJ, CH K, CHR)
SN74LVC1G86DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CH5, CHF, CHJ, CH K, CHR)
SN74LVC1G86DCKR.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CH5, CHF, CHJ, CH K, CHR)
SN74LVC1G86DCKRE4	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DCKRG4	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DCKRG4.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DCKT	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CH5, CHF, CHJ, CH K, CHR)
SN74LVC1G86DCKT.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CH5, CHF, CHJ, CH K, CHR)
SN74LVC1G86DCKTG4	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DCKTG4.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DRLR	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CH7, CHR)
SN74LVC1G86DRLR.A	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CH7, CHR)
SN74LVC1G86DRLR.B	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CH7, CHR)
SN74LVC1G86YZPR	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CH7, CHN)

# PACKAGE OPTION ADDENDUM

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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LVC1G86YZPR.B	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CH7, CHN)

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN74LVC1G86:

Automotive: SN74LVC1G86-Q1

■ Enhanced Product : SN74LVC1G86-EP

NOTE: Qualified Version Definitions:

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



# PACKAGE OPTION ADDENDUM

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- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications



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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G86DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G86DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G86DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G86DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G86DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G86DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G86DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G86DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G86DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G86DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G86DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G86DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G86YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G86DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G86DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G86DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G86DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G86DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G86DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G86DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G86DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G86DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G86DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G86DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G86DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G86YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0





### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE



## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.
   This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-293 Variation UAAD-1



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



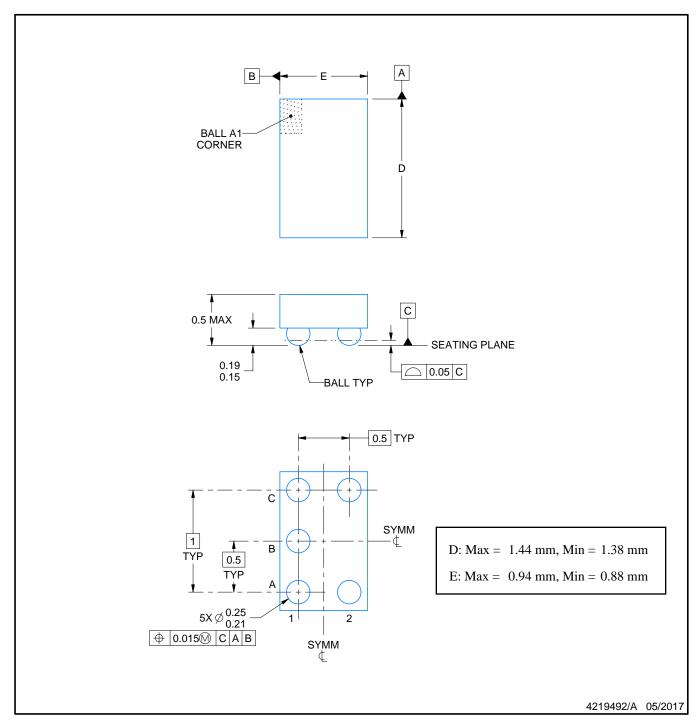
NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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