SN74LVC1G66-Q1 Single Bilateral Analog Switch

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM Classification Level H2
  - Device CDM Classification Level C5
  - Device MM Classification Level M3
- 1.65V to 5.5V V_{CC} Operation
- Inputs Accept Voltages to 5.5V
- Max t_{pd} of 0.8ns at 3.3V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5ns (V_{CC} = 3V, C_L = 50pF)
- Low ON-State Resistance, Typically ≠5.5Ω (V_{CC} = 4.5V)
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II

2 Applications

- Infotainment Systems
- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

3 Description

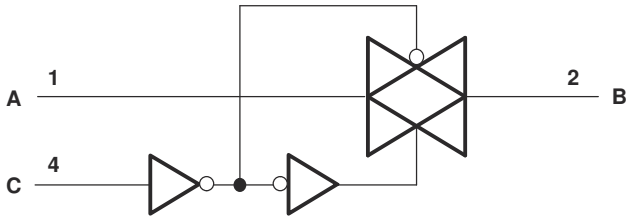
This single analog switch is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G66-Q1 device supports analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5V (peak).

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
SN74LVC1G66-Q1	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (5)	1.60mm × 1.20mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

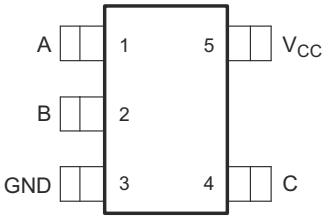


Figure 4-1. DBV and DCK Packages 5-Pin SOT-23 and SC70 Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I/O	Bidirectional signal to be switched
B	2	I/O	Bidirectional signal to be switched
C	4	I	Controls the switch (L = OFF, H = ON)
GND	3	—	Ground pin
V_{CC}	5	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	6	V
V_I	Input voltage(2) (3)		–0.5	6	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_I < 0		–50	mA
I_{IOK}	I/O port diode current	$V_{I/O}$ < 0		–50	mA
I_T	ON-state switch current	$V_{I/O}$ < 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011	1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65V to 1.95V	V_{CC} × 0.65		V
		V_{CC} = 2.3V to 2.7V	V_{CC} × 0.7		
		V_{CC} = 3V to 3.6V	V_{CC} × 0.7		
		V_{CC} = 4.5V to 5.5V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65V to 1.95V		V_{CC} × 0.35	V
		V_{CC} = 2.3V to 2.7V		V_{CC} × 0.3	
		V_{CC} = 3V to 3.6V		V_{CC} × 0.3	
		V_{CC} = 4.5V to 5.5V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
Δt/Δv	Input transition rise and fall time	V_{CC} = 1.65V to 1.95V		20	ns/V
		V_{CC} = 2.3V to 2.7V		20	
		V_{CC} = 3V to 3.6V		10	
		V_{CC} = 4.5V to 5.5V		10	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the Implications of Slow or Floating CMOS Inputs application note.

5.4 Thermal Information

THERMAL METRIC (1)		SN74LVC1G66-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262	313	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	198	203	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	142	195	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	123	120	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	142	194	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
r_{on}	ON-state switch resistance	V_I = V_{CC} or GND, V_C = V_{IH} (see Figure 6-1 and Figure 5-1)	I_S = 4mA	1.65V		12	35	Ω
			I_S = 8mA	2.3V		9	30	
			I_S = 24mA	3V		9	30	
			I_S = 32mA	4.5V		5.5	25	
$r_{on(p)}$	Peak on resistance	V_I = V_{CC} to GND, V_C = V_{IH} (see Figure 6-1 and Figure 5-1)	I_S = 4mA	1.65V		125	200	Ω
			I_S = 8mA	2.3V		35	60	
			I_S = 24mA	3V		12.5	35	
			I_S = 32mA	4.5V		7.5	25	
$I_{S(off)}$	OFF-state switch leakage current	V_I = V_{CC} and V_O = GND or V_I = GND and V_O = V_{CC}, V_C = V_{IL} (see Figure 6-2)		5.5V			±1	μA
							±0.1(1)	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_C = V_{IH}, V_O = Open (see Figure 6-3)		5.5V			±1	μA
							±0.1(1)	
I_I	Control input current	V_C = V_{CC} or GND		5.5V			±1	μA
							±0.1(1)	
I_{CC}	Supply current	V_C = V_{CC} or GND		5.5V			10	μA
							1(1)	
ΔI_{CC}	Supply current change	V_C = V_{CC} – 0.6V		5.5V			500	μA
C_{ic}	Control input capacitance			5V		2		pF
$C_{io(off)}$	Switch input and output capacitance			5V		6		pF
$C_{io(on)}$	Switch input and output capacitance			5V		15		pF

(1) T_A = 25°C

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-4)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} (1)	Propagation delay	A or B	B or A		5.5		3.2		2.8		2.6	ns
t_{en} (2)	Enable time	C	A or B	2.5	14	1.9	9.5	1.8	8	1.5	7.2	ns
t_{dis} (3)	Disable time	C	A or B	2.2	12	1.4	8.9	2	8.4	1.4	6.9	ns

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t_{PZL} and t_{PZH} are the same as t_{en}.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

5.7 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response(1) (switch ON)	A or B	B or A	C_L = 50pF, R_L = 600Ω, f_{in} = sine wave (see Figure 6-5)	1.65V	35	MHz
				2.3V	120	
				3V	175	
				4.5V	195	
			C_L = 5pF, R_L = 50Ω, f_{in} = sine wave (see Figure 6-5)	1.65V	>300	
				2.3V	>300	
				3V	>300	
				4.5V	>300	
Crosstalk (control input to signal output)	C	A or B	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (square wave) (see Figure 6-6)	1.65V	35	mV
				2.3V	50	
				3V	70	
				4.5V	100	
Feedthrough attenuation(2) (switch OFF)	A or B	B or A	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (sine wave) (see Figure 6-7)	1.65V	–58	dB
				2.3V	–58	
				3V	–58	
				4.5V	–58	
			C_L = 5pF, R_L = 50Ω, f_{in} = 1MHz (sine wave) (see Figure 6-7)	1.65V	–42	
				2.3V	–42	
				3V	–42	
				4.5V	–42	
Sine-wave distortion	A or B	B or A	C_L = 50pF, R_L = 10kΩ, f_{in} = 1kHz (sine wave) (see Figure 6-8)	1.65V	0.5%	
				2.3V	0.025%	
				3V	0.015%	
				4.5V	0.01%	
			C_L = 50pF, R_L = 10kΩ, f_{in} = 10kHz (sine wave) (see Figure 6-8)	1.65V	0.15%	
				2.3V	0.025%	
				3V	0.015%	
				4.5V	0.01%	

(1) Adjust f_{in} voltage to obtain 0dBm at output. Increase f_{in} frequency until dB meter reads –3dB.
(2) Adjust f_{in} voltage to obtain 0dBm at input.

5.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10MHz	8	9	9	11	pF

5.9 Typical Characteristics

T_A = 25°C

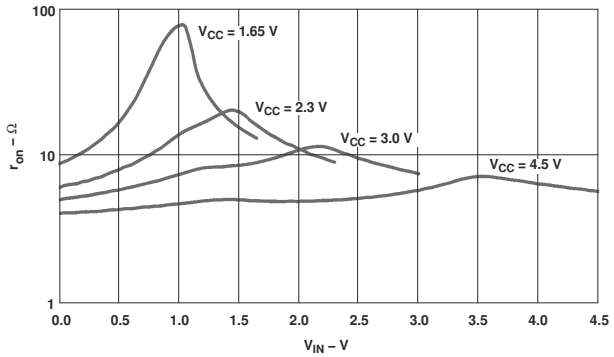


Figure 5-1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

6 Parameter Measurement Information

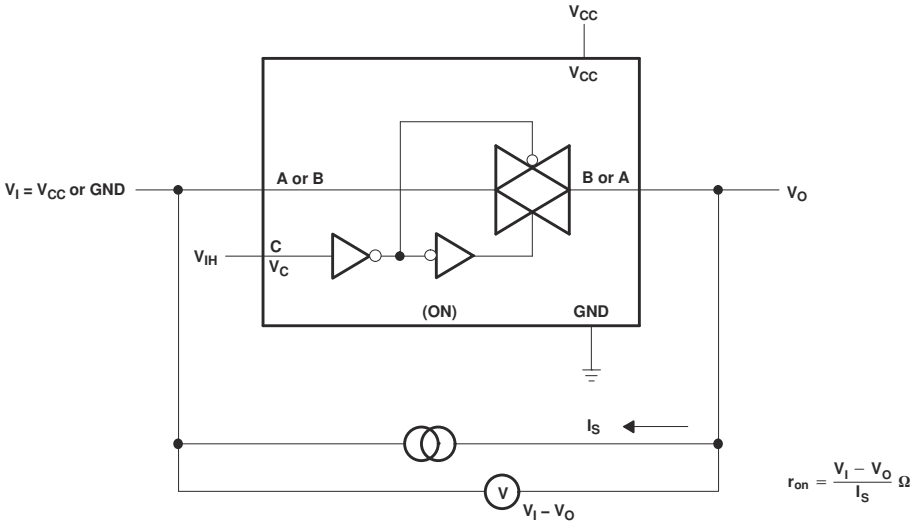


Figure 6-1. ON-State Resistance Test Circuit

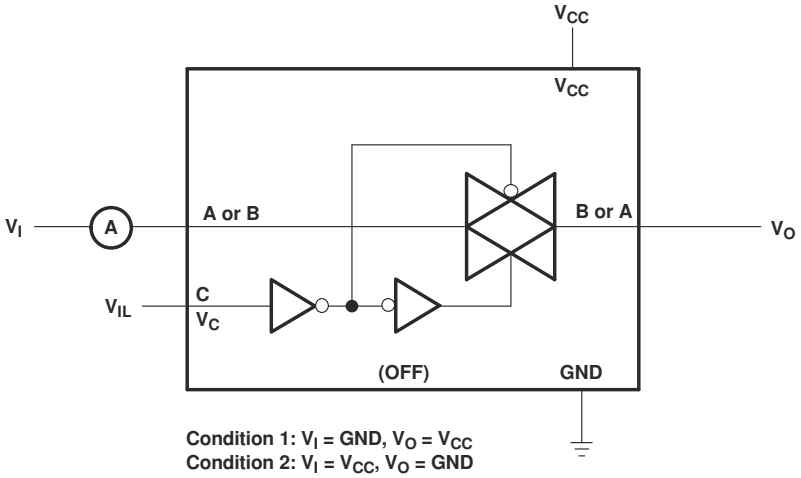


Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

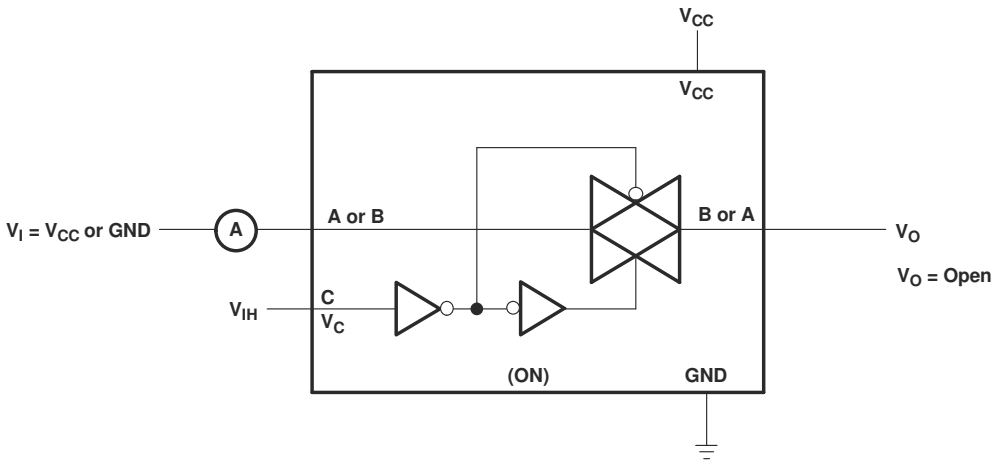
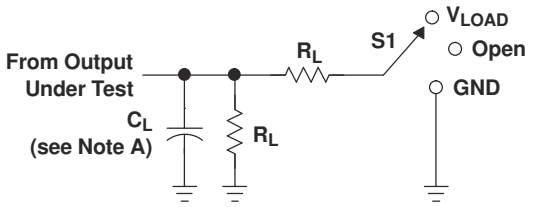


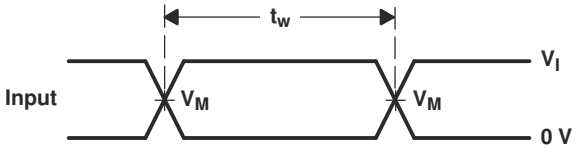
Figure 6-3. ON-State Switch Leakage-Current Test Circuit



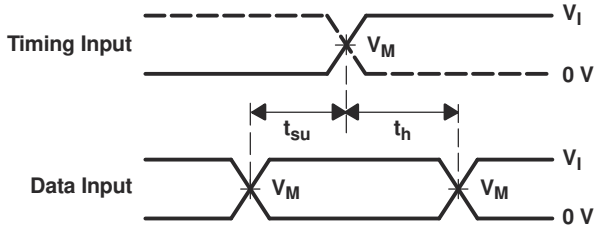
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

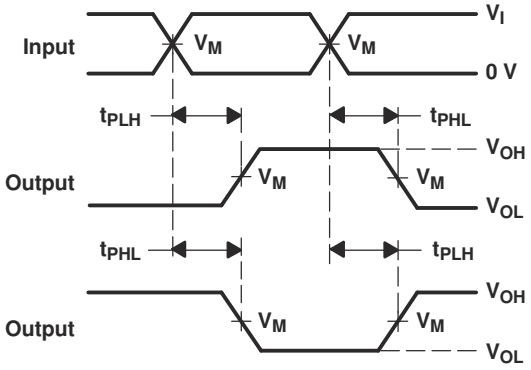
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



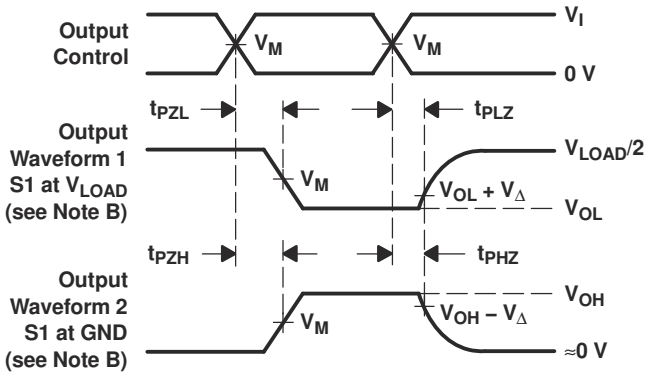
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-4. Load Circuit and Voltage Waveforms

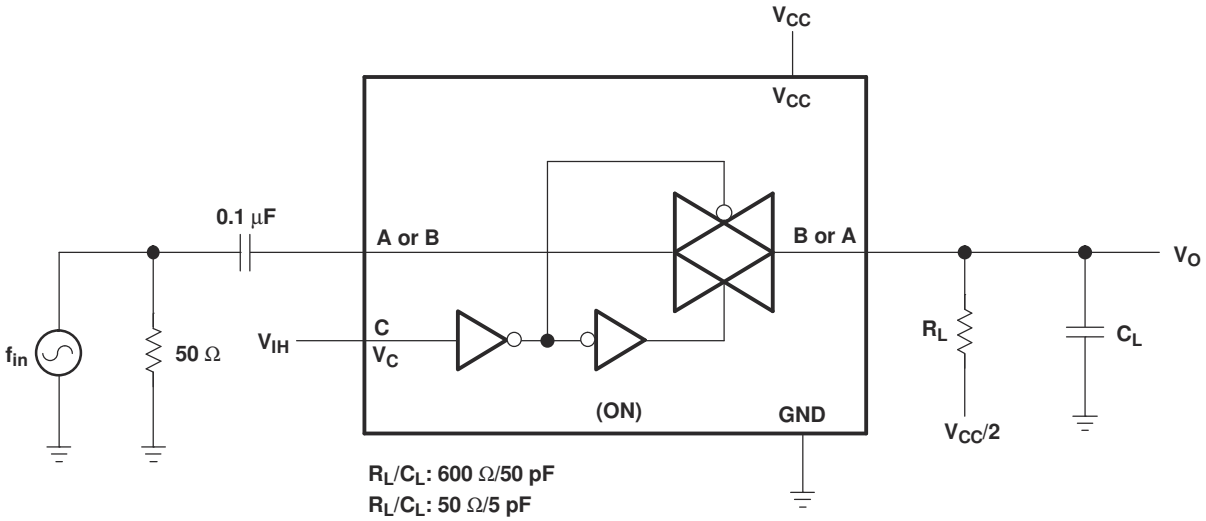


Figure 6-5. Frequency Response (Switch ON)

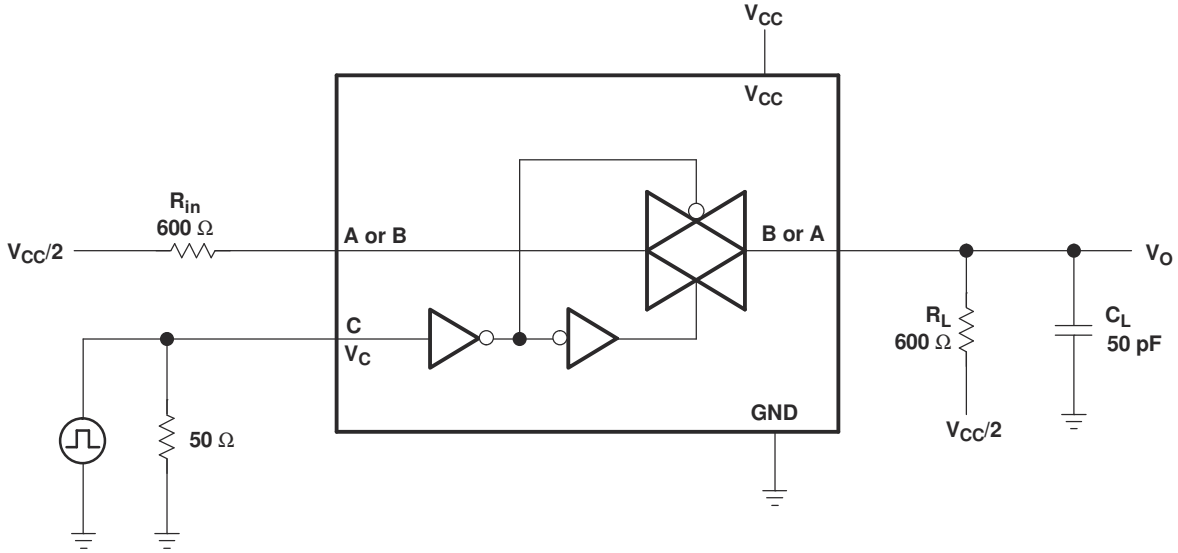


Figure 6-6. Crosstalk (Control Input – Switch Output)

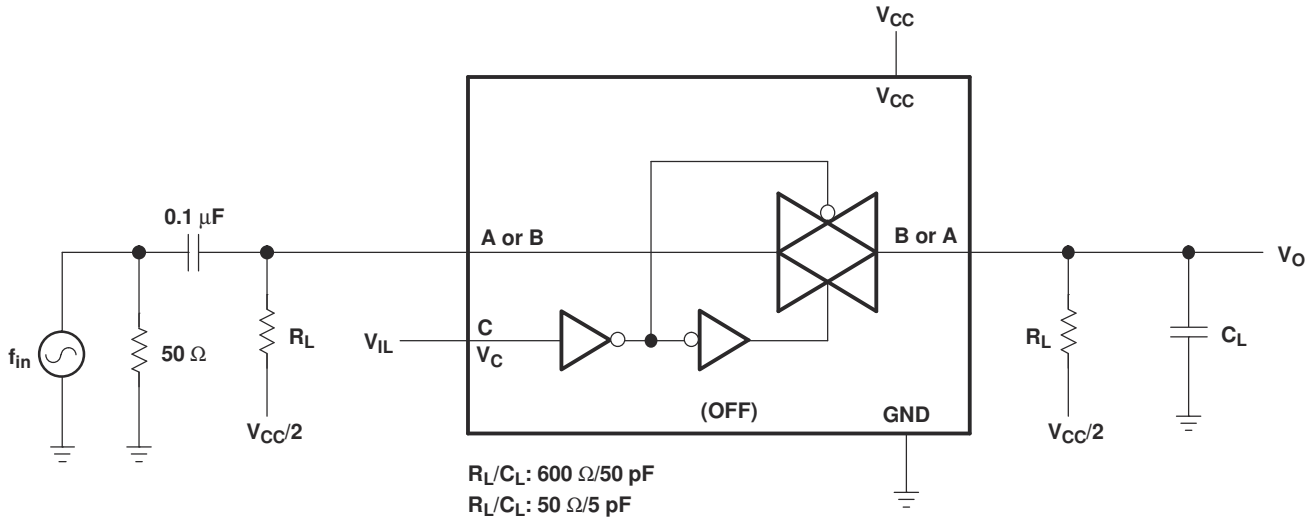


Figure 6-7. Feedthrough (Switch OFF)

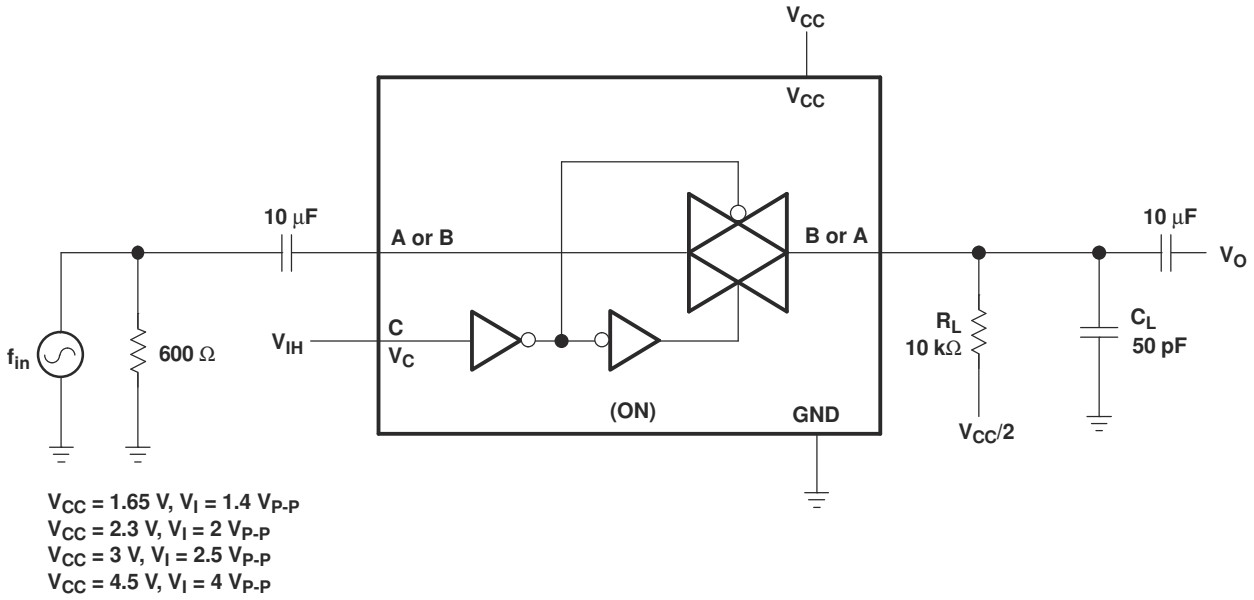


Figure 6-8. Sine-Wave Distortion

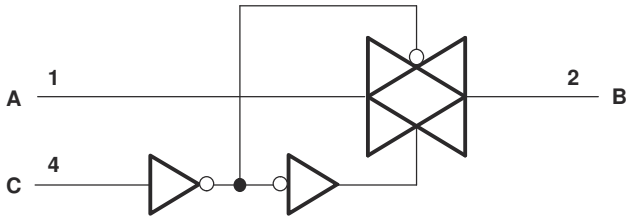
7 Detailed Description

7.1 Overview

This single analog switch is designed for 1.65V to 5.5V V_{CC} operation in automotive applications.

The SN74LVC1G66-Q1 device supports analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5V (peak). Like all analog switches, the SN74LVC1G66-Q1 is bidirectional.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

This device is tested for operation in automotive applications. The SN74LVC1G66-Q1 has a wide V_{CC} range, allowing rail-to-rail operation of signals anywhere from a 1.8V system to a 5V system. In addition, the control input (C Pin) is 5.5V tolerant, allowing higher-voltage logic to interface to the switch control system.

7.4 Device Functional Modes

Table 7-1. Function Table

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G66-Q1 device can be used in any situation where an SPST switch would be used and a solid-state, voltage-controlled version is preferred.

8.2 Typical Application

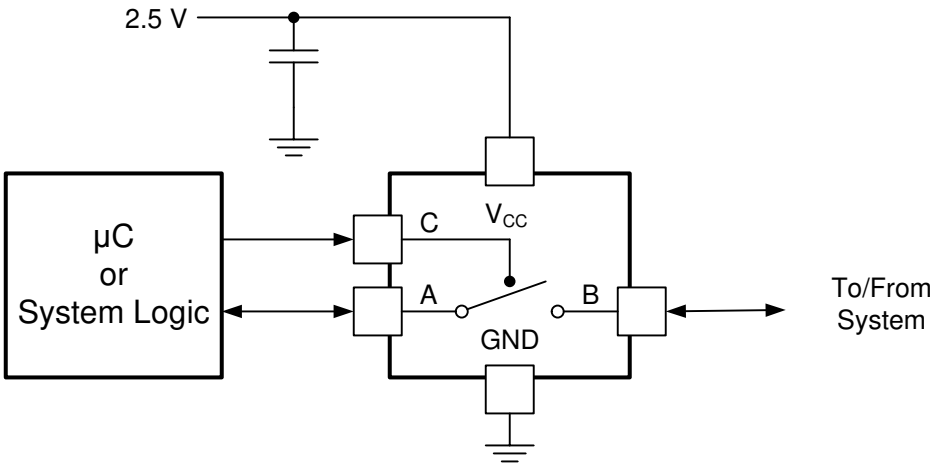


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

The SN74LVC1G66-Q1 device allows on and off control of analog and digital signals with a digital control signal. All input signals must be between 0V and V_{CC} for optimal operation.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specifications, see Δt/Δv in the *Section 5.3* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Section 5.3* table.
   - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5V at any valid V_{CC}.
2. Recommended output conditions:
   - Load currents should not exceed ±50mA.
3. Frequency selection criterion:
   - Maximum frequency tested is 150MHz.
   - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the *Section 10* section.

8.2.3 Application Curve

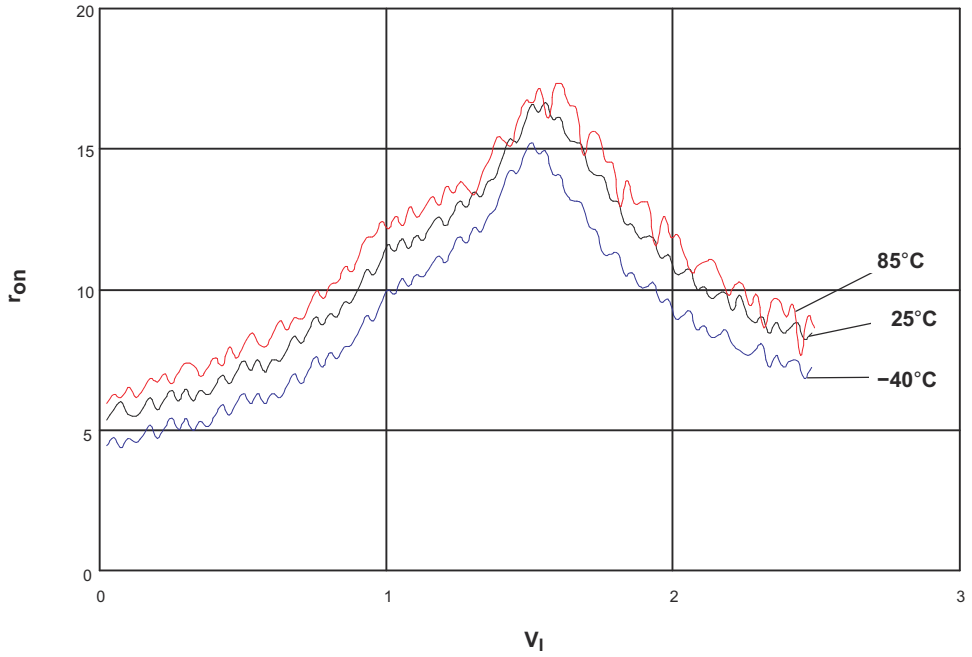


Figure 8-2. r_{on} vs V_I, V_{CC} = 2.5V (SN74LVC1G66-Q1)

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Section 5.3* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

10.2 Layout Example

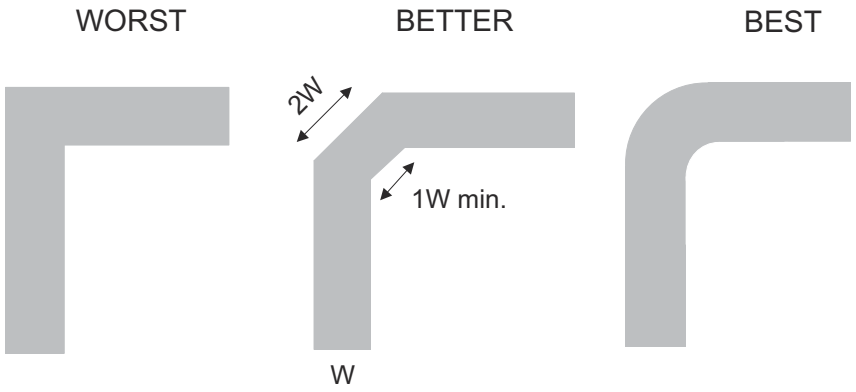


Figure 10-1. Trace Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2015) to Revision F (June 2025)	Page
• Updated Peak on resistance in Section 5.5	5
• Updated Switch capacitance in Section 5.5	5
• Updated Sine-wave distortion in Section 5.7	6

Changes from Revision D (January 2008) to Revision E (April 2015)	Page
• Added *Device Information* and *ESD Ratings* tables and the following sections: *Pin Configurations and Functions*, *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information*	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
1P1G66QDBVRG4Q1	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	C66R
1P1G66QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C66R
1P1G66QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C66R
1P1G66QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C66R
SN74LVC1G66QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C6O
SN74LVC1G66QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C6O
SN74LVC1G66QDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C6O

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC1G66-Q1 :

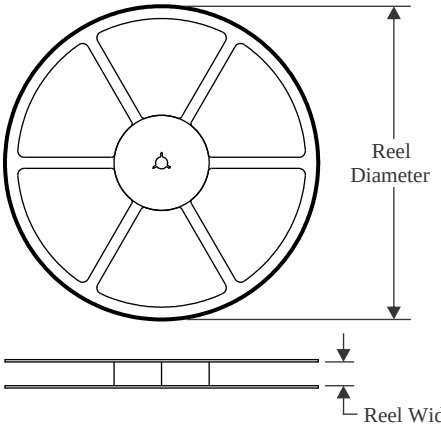
- Catalog : SN74LVC1G66

NOTE: Qualified Version Definitions:

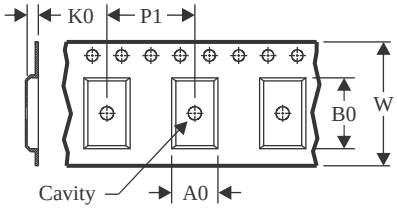
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

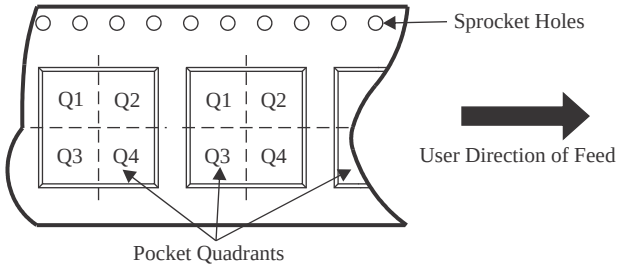


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

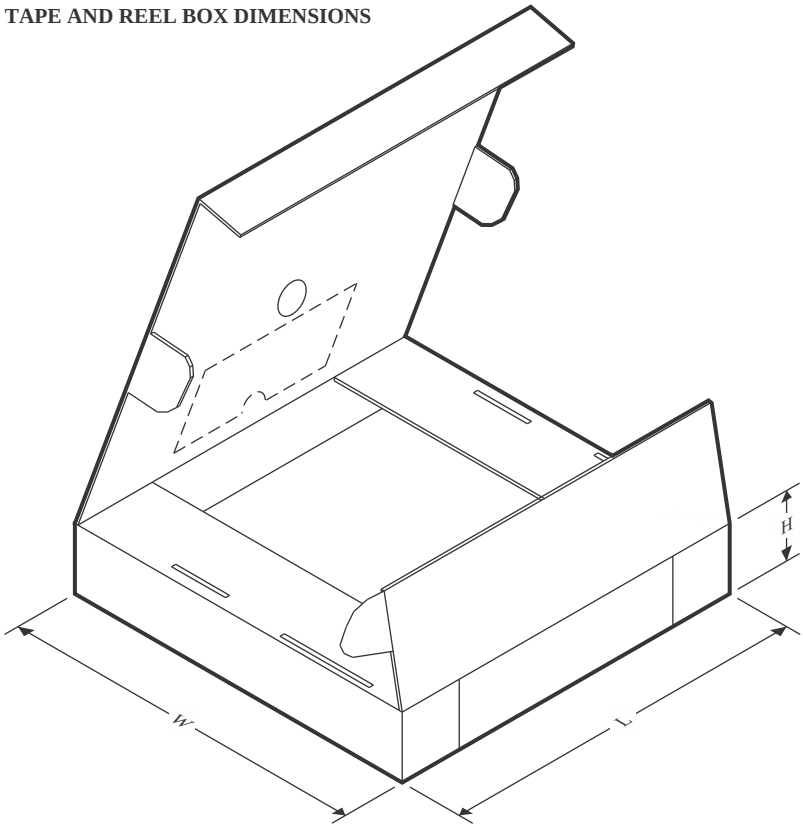
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1P1G66QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G66QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

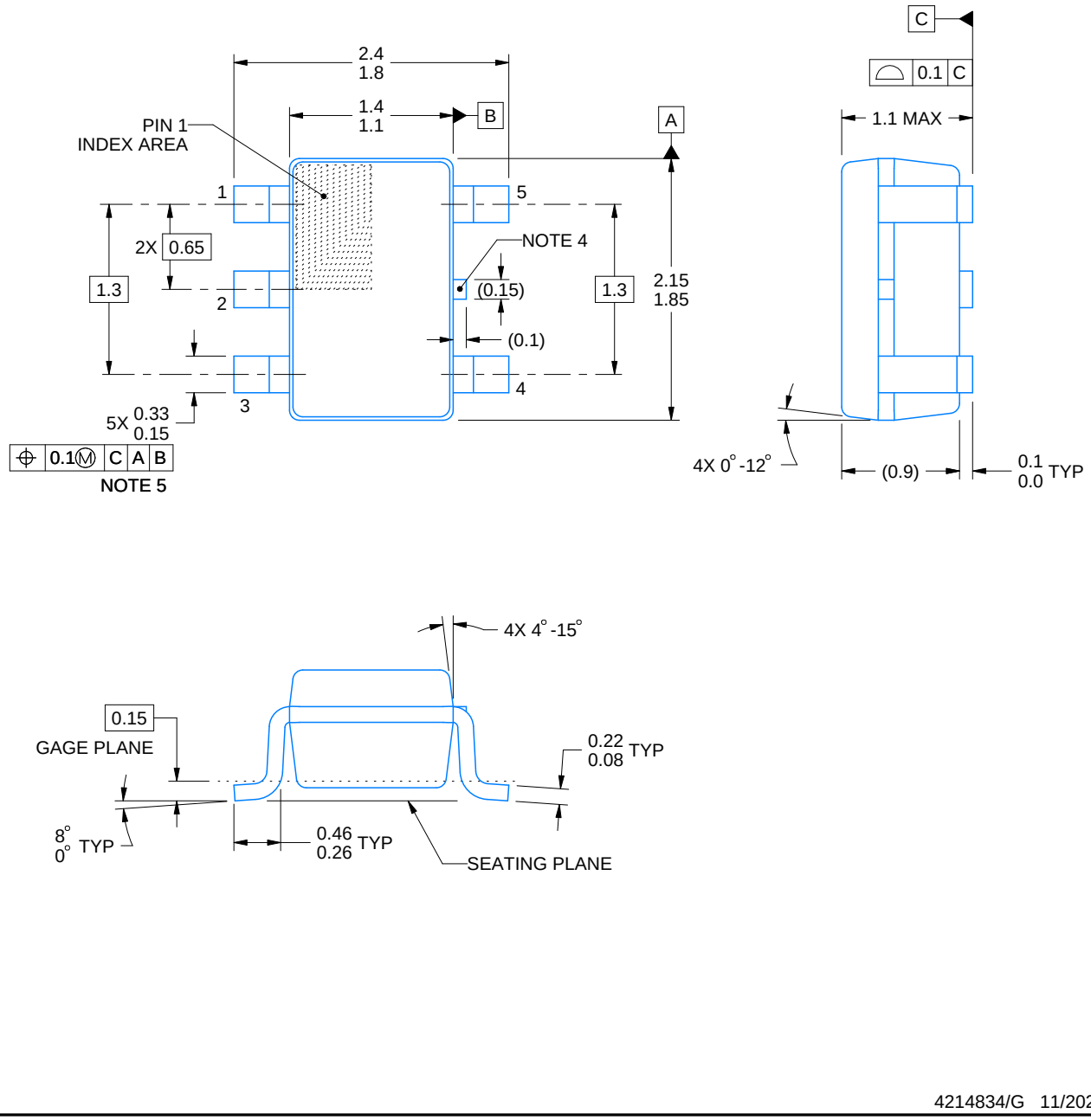
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1P1G66QDBVRQ1	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G66QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

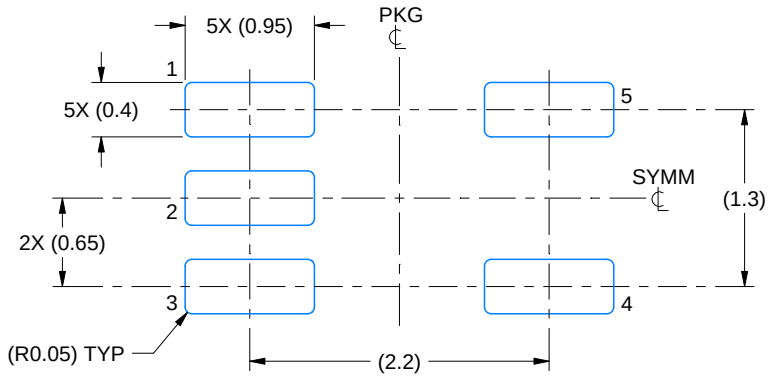
SMALL OUTLINE TRANSISTOR



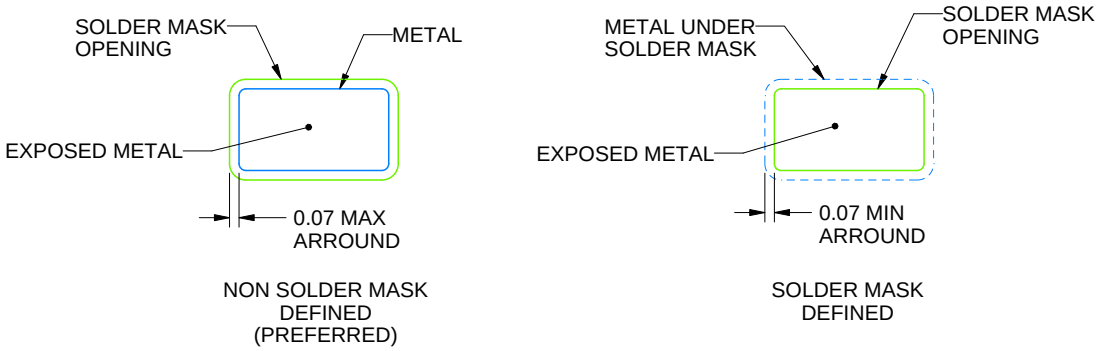
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

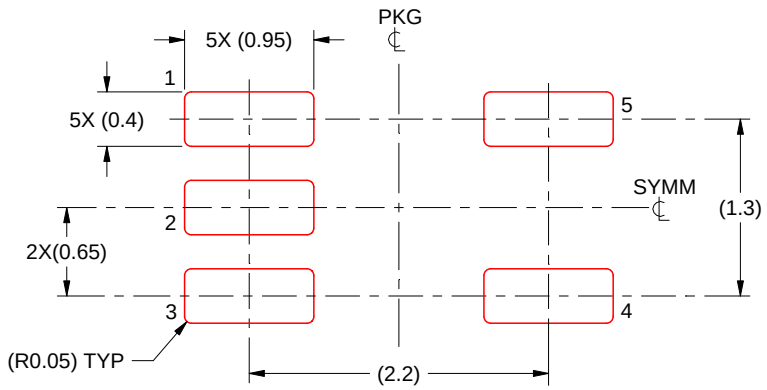


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

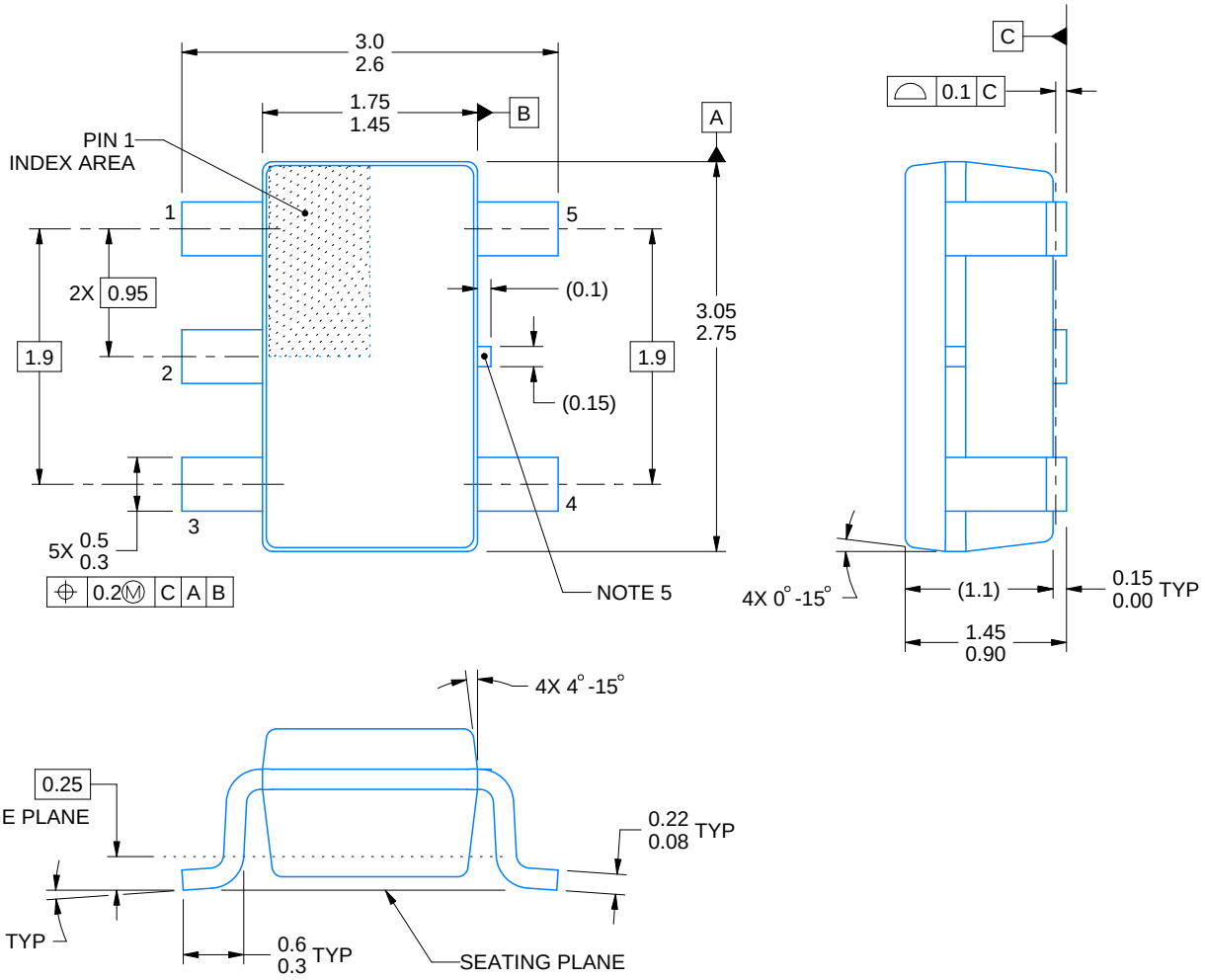
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

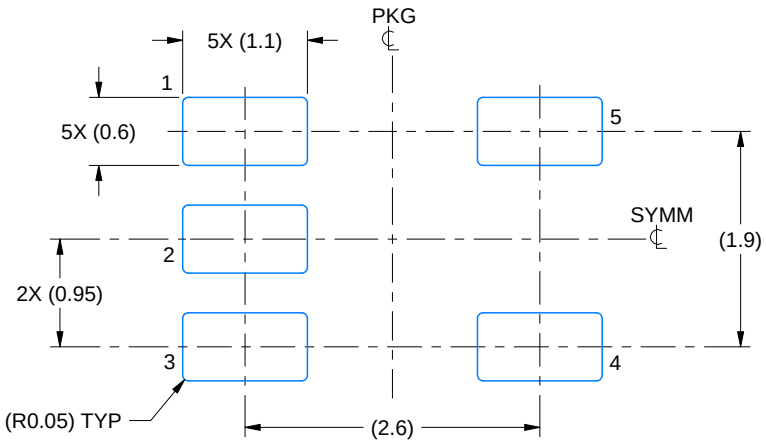
SMALL OUTLINE TRANSISTOR



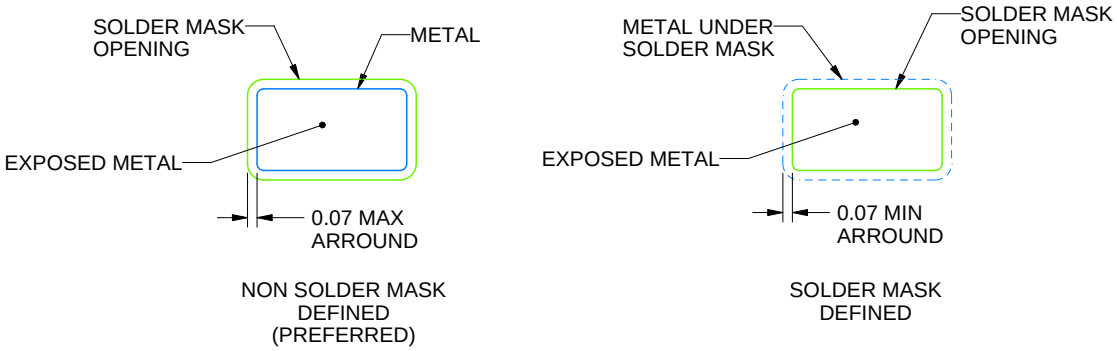
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

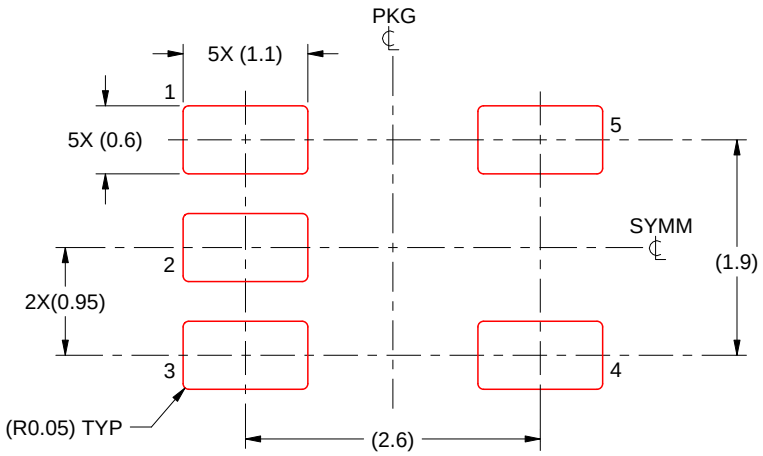


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025