











SN74LVC1G57

SCES414P - NOVEMBER 2002 - REVISED NOVEMBER 2016

SN74LVC1G57 Configurable Multiple-Function Gate

Features

- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
 - Supports Down Translation to V_{CC}
- Max t_{pd} of 6.3 ns at 3.3 V
- Schmitt-Triggered Inputs
- Low Power Consumption, 10-µA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Available in the Texas Instruments NanoFree™ Package

Applications

- Active Noise Cancellation (ANC)
- **Barcode Scanners**
- **Blood Pressure Monitors**
- **CPAP Machines**
- Cable Solutions
- **Embedded PCs**
- Field Transmitter: Temperature or Pressure Sensors
- HVAC: Heating, Ventilating, and Air Conditioning
- TVs: High-Definition (HDTV), LCD, and Digital
- Video Communications Systems

3 Description

The SN74LVC1G57 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negativegoing (V_{T_-}) signals.

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

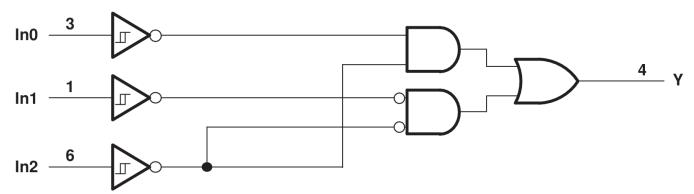
NanoFree™ package technology is breakthrough in IC packaging concepts, using the die as the package.

Device Information⁽¹⁾

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
SN74LVC1G57DBV	SOT-23 (6)	2.90 mm × 1.60 mm
SN74LVC1G57DCK	SC70 (6)	2.00 mm × 1.25 mm
SN74LVC1G57DRL	SOT (6)	1.60 mm × 1.20 mm
SN74LVC1G57DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G57DSF	SON (6)	1.00 mm × 1.00 mm
SN74LVC1G57YZP	DSBGA (6)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

Changes from Revision O (December 2013) to Revision P

Changes from Revision L (January 2007) to Revision M

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

 Added Applications section, Device Information table, ESD Ratings table, Thermal Information Description section, Device Functional Modes, Application and Implementation section, Power Recommendations section, Layout section, Device and Documentation Support section, and M Packaging, and Orderable Information section 	Supply lechanical,
 Changed Package thermal impedance, R_{θJA}, values From: 165°C/W To: 223°C/W (DBV), From: 271.7°C/W (DCK), From: 142°C/W To: 252.5°C/W (DRL), and From: 123°C/W To: 124°C/W (Y 	n: 259°C/W To:
Changes from Revision N (April 2013) to Revision O	Page
Changed I _{off} in Features	1
Changed Operating temperature range	4
Changes from Revision M (October 2011) to Revision N	Page
Removed Ordering Information table; package updates now included in Package Ordering Add	dendum 1

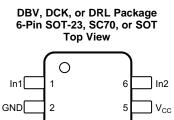
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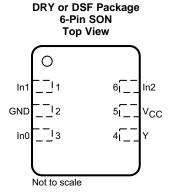


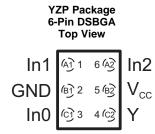
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5 Pin Configuration and Functions



Not to scale





Pin Functions

	PIN	1/0	DECORPORTION
NO.	NAME	1/0	DESCRIPTION
1	In1	I	Logic input 1
2	GND	_	Ground
3	In0	I	Logic input 0
4	Y	0	Logic output
5	V _{CC}	_	Power
6	ln2	I	Logic input 2

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, V _{CC}		-0.5	6.5	V
Input voltage, V _I ⁽²⁾		-0.5	6.5	V
Valtage record (applied to any extens) V	High-impedance or power-off state (2)	-0.5	6.5	
Voltage range (applied to any output), V _O	High or low state (2)(3)	-0.5	V _{CC} + 0.5	V
Input clamp current, I _{IK} (V _I < 0)			-50	mA
Output clamp current, I _{OK} (V _O < 0)			-50	mA
Continuous output current, I _O			±50	mA
Continuous current through V _{CC} or GND			±100	mA
Junction temperature, T _J			150	°C
Storage temperature, T _{stg}		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	\ /
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V	Cupply voltage	Operating	1.65	5.5	V
V _{CC}	Supply voltage	Data retention only	1.5		V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I_{OH}	I _{OH} High-level output current	High-level output current		-16	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current	V 2 V		16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		32	
-	Operation for a sin town part we	BGA package	-40	85	°C
T_A	Operating free-air temperature	All other packages	-40	125	-0

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation, see *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Product Folder Links: SN74LVC1G57

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the Recommended Operating Conditions table.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.4 Thermal Information

			SN74LVC1G57					
	THERMAL METRIC ⁽¹⁾	DBV (SOT)	DCK (SOT)	DRL (SOT)	YZP (DSGBA)	DSF (SON)	DRY (SON)	UNIT
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	223	271.7	252.5	124	360.1	332.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.4	129.8	111.6	1.4	158.8	198.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71	73.1	118.5	29.7	213.5	189	°C/W
ΨЈТ	Junction-to-top characterization parameter	57.1	8.3	11.8	0.5	20.4	44.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	70.3	72.4	118.8	30.1	213.2	189.7	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COM	IDITIONS	MIN	TYP ⁽¹⁾ MAX	UNIT
		V _{CC} = 1.65 V		0.79	1.16	
		V _{CC} = 2.3 V		1.11	1.56	
V_{T+}	Positive-going input threshold voltage	V _{CC} = 3 V	1.5	1.87	V	
		V _{CC} = 4.5 V		2.16	2.74	
		V _{CC} = 5.5 V		2.61	3.33	
		V _{CC} = 1.65 V		0.35	0.62	
		V _{CC} = 2.3 V		0.58	0.87	
V_{T-}	Negative-going input threshold voltage	V _{CC} = 3 V		0.84	1.19	V
		V _{CC} = 4.5 V		1.41	1.9	
		V _{CC} = 5.5 V		1.87	2.29	
		V _{CC} = 1.65 V		0.3	0.62	
		V _{CC} = 2.3 V		0.4	0.8	
ΔV_{T}	Hysteresis (V _{T+} – V _{T-})	V _{CC} = 3 V		0.53	0.87	V
		V _{CC} = 4.5 V	0.71	1.04		
		V _{CC} = 5.5 V	0.71	1.11		
		$V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}, I_{OH} = -100 \mu\text{A}$		V _{CC} - 0.1		
		V _{CC} = 1.65 V, I _{OH} = -4 mA		1.2		
		V _{CC} = 2.3 V, I _{OH} = -8 mA		1.9		
V _{OH}		$V_{CC} = 3 \text{ V}, I_{OH} = -16 \text{ mA}$		2.4		V
		$V_{CC} = 3 \text{ V}, I_{OH} = -24 \text{ mA}$		2.3		
		$V_{CC} = 4.5 \text{ V}, I_{OH} = -32 \text{ mA}$		3.8		
		$V_{CC} = 1.65 \text{ V to } 5.5 \text{ V, } I_{OL} =$	100 μΑ		0.1	
		V _{CC} = 1.65 V, I _{OL} = 4 mA			0.45	
		V _{CC} = 2.3 V, I _{OL} = 8 mA			0.3	
.,			$T_A = -40$ °C to 85°C		0.4	.,
V_{OL}		$V_{CC} = 3 \text{ V}, I_{OL} = 16 \text{ mA}$	$T_A = -40^{\circ}C$ to 125°C		0.45	V
		V _{CC} = 3 V, I _{OL} = 24 mA	+		0.55	
			$T_A = -40$ °C to 85°C		0.55	
		$V_{CC} = 4.5 \text{ V}, I_{OL} = 32 \text{ mA}$	$T_A = -40^{\circ}C \text{ to } 125^{\circ}C$		0.58	
l _l		V _{CC} = 0 V to 5.5 V, V _I = 5.5 V or GND			±1	μA
I _{off}		$V_{CC} = 0 \text{ V}, V_{I} \text{ or } V_{O} = 5.5 \text{ V}$			±10	μA
I _{CC}		$V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}, V_{I} = 5.5 \text{ V or GND}, I_{O} = 0$			10	μΑ
ΔI_{CC}		$V_{CC} = 3 \text{ V to } 5.5 \text{ V}$, one input at $V_{CC} - 0.6 \text{ V}$, other inputs at V_{CC} or GND			500	μΑ
Ci		$V_{CC} = 3.3 \text{ V}, V_{I} = V_{CC} \text{ or GN}$	D		3.5	pF

Product Folder Links: SN74LVC1G57

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C



Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

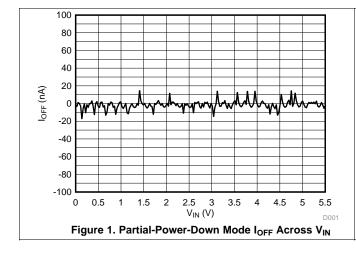
	PARAMETER	TEST CON	DITIONS	MIN TYP ⁽¹⁾ MAX	UNIT
			V _{CC} = 1.8 V	20	
	Dower dissination consistence	f 40 MH = T 25°C	V _{CC} = 2.5 V	20	
C_{pd}	Power dissipation capacitance	f = 10 MHz, T _A = 25°C	V _{CC} = 3.3 V	21	pF
			V _{CC} = 5 V	22	

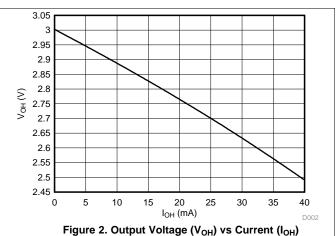
6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP MAX	UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	3.2	14.4		
		$T_A = -40$ °C to 85°C	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	2	8.3		
		1 _A = -40°C to 85°C	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	6.3		
	A : \		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1.1	5.1		
t _{pd}	Any input to Y (output)		V _{CC} = 1.8 V ± 0.15 V	3.2	16.4	ns	
		T = 40°C to 125°C	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	2	9.3		
		$T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C}$ $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	T _A = -40 C to 125 C	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	7.3	
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1.1	6.1		

6.7 Typical Characteristics



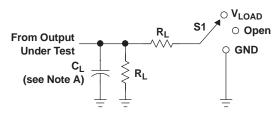


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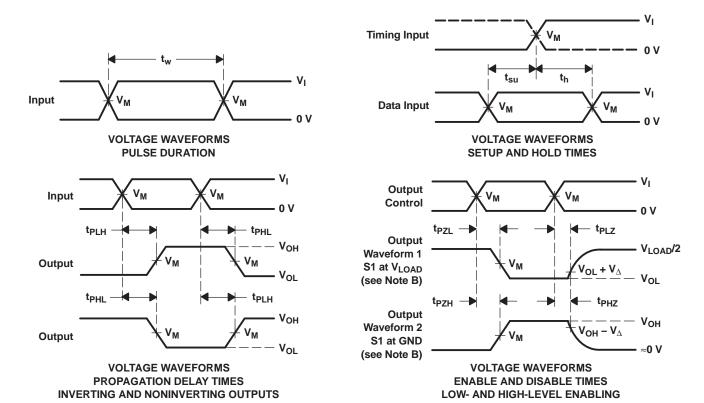
7 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

П	0	Δ	D	CI	R	CI	Ш	т
_	·	_	\boldsymbol{v}	v	1	v	u	

.,	INPUTS		.,	.,		В	.,
V _{CC}	V_{I}	V _I t _r /t _f V _N		V _{LOAD}	CL	R _L	V_{Δ}
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	v_{cc}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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8 Detailed Description

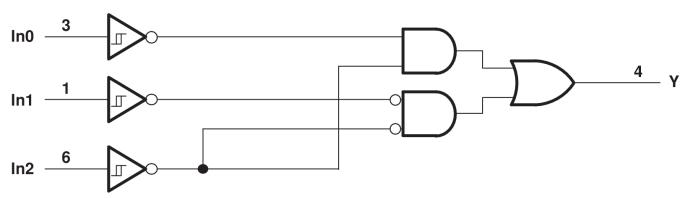
8.1 Overview

The SN74LVC1G57 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to $V_{\rm CC}$ or GND.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Schmitt-Trigger Inputs

Schmitt-trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs

8.3.2 Inputs Accept Voltages to 5.5 V

The SN74LVC1G57 is a configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation. Inputs are over-voltage tolerant up to 5.5 V. This feature allows the use of this device as a translator in a mixed 1.8-V, 3.3-V, and 5-V system environment.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G57 and Table 2 lists the logic configuration images.

Table 1. Function Table

	INPUTS					
ln2	In1	In0	Y			
L	L	L	Н			
L	L	Н	L			
L	Н	L	Н			
L	Н	Н	L			
Н	L	L	L			
Н	L	Н	L			
Н	Н	L	Н			
Н	Н	Н	Н			

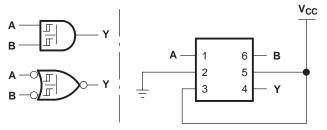
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Table 2. Logic Configurations

LOGIC FUNCTION	FIGURE NO.
2-Input AND	Figure 4
2-Input AND with both inputs inverted	Figure 7
2-Input NAND with inverted input	Figure 5 and Figure 6
2-Input OR with inverted input	Figure 5 and Figure 6
2-Input NOR	Figure 7
2-Input NOR with both inputs inverted	Figure 4
2-Input XNOR	Figure 8



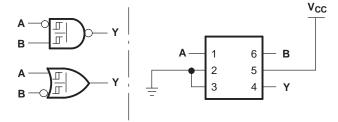
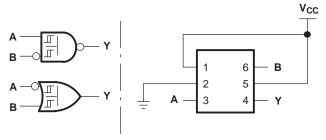


Figure 4. 2-Input AND Gate

Figure 5. 2-Input NAND Gate With Inverted A Input



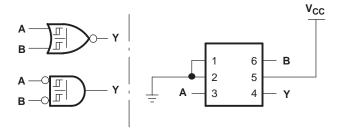


Figure 6. 2-Input NAND Gate With Inverted B Input

Figure 7. 2-Input NOR Gate

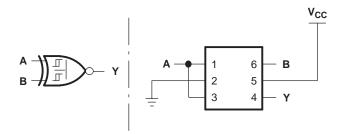


Figure 8. 2-Input XNOR Gate



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G57 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

9.2 Typical Application

This application shows the SN74LVC1G57 configured as an OR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high 1. Normally this application would require two external gates, but because the SN74LVC1G57 can be configured to meet this function the application can be implemented with a single chip solution.

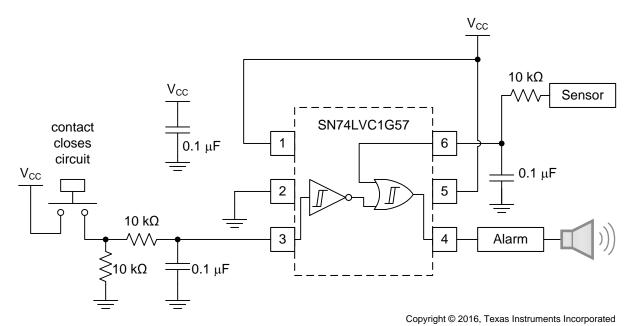


Figure 9. Dual-Sensor Alarm Trigger

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Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Application Truth Table

Because we are working with two independent alarm triggers, we need to ensure that the alarm signal is only sent whenever either condition is met. Therefore our resulting truth table will look very much like a logic OR function. However, since we are also assuming one of the conditions to always be true, i.e. a door that should remain closed, we make use of the inverted input in Table 3.

INPUTS OUTPUT ALARM TRIGGER OR SWITCH **SENSOR** Χ Н L L L Н Χ Н Н

Table 3. Dual-Sensor Truth Table

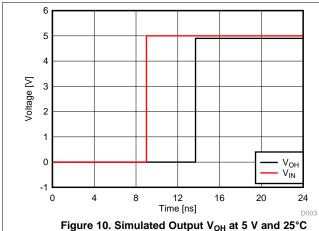
9.2.1.2 Schmitt-Trigger Inputs

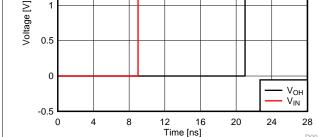
On a normal (non-Schmitt-Trigger) input the part will switch at the same point on the rising edge and falling edge. With a slow rising edge the part will switch at the threshold. When the switch occurs it will require current from V_{CC} . When current is forced from V_{CC} , the V_{CC} level can drop causing the threshold to shift. When the threshold shifts it will cross the input again causing the part to switch again. This can go on and on causing oscillation which can cause excessive current. The same thing can happen if there is noise on the input. The noise can cross the threshold multiple times and cause oscillation or multiple clocking. The solution to these problems is to use a Schmitt-Trigger type device to translate the slow or noisy edges into something faster that will meet the input rise and fall specs of the following device. A true Schmitt-Trigger input will not have rise and fall time limitations.

9.2.2 Detailed Design Procedure

- 1. Recommended Input conditions:
 - Specified high and low levels. See (V_{IH} and V_{IL}) in Recommended Operating Conditions.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- 2. Recommended output conditions:
 - Load currents should not exceed 20 mA on the output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves





1.5

Figure 11. Simulated Output VOH at 1.8 V and 25°C



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 12 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

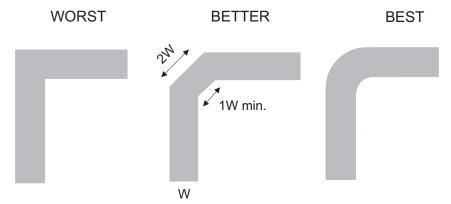


Figure 12. Trace Example

Submit Documentation Feedback



12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC1G57

www.ti.com

7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G57DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA7O, CA7R)
SN74LVC1G57DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA7O, CA7R)
SN74LVC1G57DBVRG4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA7R
SN74LVC1G57DBVRG4.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA7R
SN74LVC1G57DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CL5, CLF, CLJ, CL K, CLR)
SN74LVC1G57DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CL5, CLF, CLJ, CL K, CLR)
SN74LVC1G57DCKRG4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CLF
SN74LVC1G57DCKRG4.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CLF
SN74LVC1G57DRLR	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(1K2, CL7, CLR)
SN74LVC1G57DRLR.B	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(1K2, CL7, CLR)
SN74LVC1G57DRLRG4	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1K2
SN74LVC1G57DRLRG4.B	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1K2
SN74LVC1G57DRY2	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRY2.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57YZPR	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CLN
SN74LVC1G57YZPR.B	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CLN

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

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- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G57DBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G57DRLRG4	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G57DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G57DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G57DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G57DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G57DBVRG4	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC1G57DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G57DRLRG4	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G57DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-293 Variation UAAD



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. NanoFree[™] package configuration.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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