











SN74LVC1G32-Q1

SCES648A - FEBRUARY 2006 - REVISED AUGUST 2019

SN74LVC1G32-Q1 Single 2-input positive-OR gate

Features

- Available in the small 1.45 mm² Package (DRY) with 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5-V
- Supports Down Translation to V_{CC}
- Max t_{od} of 3.6 ns at 3.3-V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3-V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

Applications

- **AV Receiver**
- Blu-ray Player and Home Theater
- Digital Picture Frame (DPF)
- Embedded PC
- IP Phone: Wireless
- High-Speed Data Acquisition and Generation
- Motor Control: High-Voltage
- Optical Networking: Video Over Fiber and EPON
- Personal Navigation Device (GPS)
- Portable Media Player
- Private Branch Exchange (PBX)
- Server PSU
- SSD: Internal and External
- TV: LCD/Digital and High-Definition (HDTV)
- Telecom Shelter: Power Distribution Unit (PDU), Power Monitoring Unit (PMU), Wireless Battery Monitoring, Remote Electrical Tilt Unit (RET), Remote Radio Unit (RRU), Tower Mounted Amplifier (TMA)
- Video Conferencing: IP-Based HD
- Vector Signal Analyzer and Generator
- WiMAX and Wireless Infrastructure Equipment
- Wireless Headset, Keyboard, Mouse, and Repeater

3 Description

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G32-Q1 device performs the Boolean function $Y = A + B \text{ or } Y = \overline{A \cdot B}$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G32-Q1 device is available in a variety of packages, including the small DRY package with a body size of 1.45×1.00 mm.

Device Information

DEVICE NAME	PACKAGE (PINS)	BODY SIZE
SN74LVC1G32QDBV	SOT-23 (5)	2.90mm × 2.80mm
SN74LVC1G32QDCK	SC70 (5)	2.00mm × 1.25mm
SN74LVC1G32QDRY	SON (6)	1.45mm × 1.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.





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4 Revision History

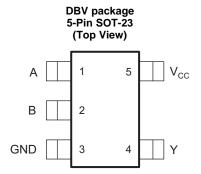
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

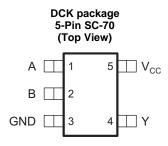
CI	hanges from Original (February 2006) to Revision A	Page
•	Changed data sheet format to new TI standard	1
•	Added SON (6) DRY package to Device Information table	1
•	Added DRY Package to Pin Configuration and Functions section.	3

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5 Pin Configuration and Functions





DRY package 6-Pin SON (Transparent Top View)



NC = No Connect

See Mechanical drawings at the end of the data sheet for dimensions

Pin Functions

	PIN		DESCRIPTION
NAME	DBV, DCK	DRY	DESCRIPTION
Α	1	1	Input
В	2	2	Input
GND	3	3	Ground
Υ	4	4	Output
VCC	5	6	Power pin
NC	-	5	Not connected

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impe	dance or power-off state ⁽²⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or lov	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current $V_I < 0$			-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
TJ	Junction temperature		150	°C	
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

	PARAMETER	DEFINITION	VAUE	UNIT
	Floring	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT			
.,	Complexed to me	Operating	1.65	5.5	V			
V_{CC}	Supply voltage	Data retention only	1.5		V			
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}					
.,	High level input valtage	V _{CC} = 2.3 V to 2.7 V	1.7		V			
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V			
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	0.7 × V _{CC}				
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}				
.,	Level level Construction	V _{CC} = 2.3 V to 2.7 V		0.7	V			
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8				
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}				
VI	Input voltage		0	5.5	V			
Vo	Output voltage		0	V _{CC}	V			
		V _{CC} = 1.65 V		-4				
		V _{CC} = 2.3 V		-8	1			
I_{OH}	High-level output current	V 2V		-16	mA			
		$V_{CC} = 3 V$		-24				
		V _{CC} = 4.5 V		-32				
		V _{CC} = 1.65 V		4				
		V _{CC} = 2.3 V		8				
I_{OL}	Low-level output current	V 2V		16	mA			
		$V_{CC} = 3 V$		24				
		V _{CC} = 4.5 V		32				
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20				
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		ns/V				
		V _{CC} = 5 V ± 0.5 V		5				
_	Operating free circumperature	DSBGA package	-40	85	°C			
T_A	Operating free-air temperature	All other packages	-40	125	°C			

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

U	iormar imormation				
			SN74LVC1G32-Q1		
	THERMAL METRIC ⁽¹⁾	DBV	DCK	DRY	UNIT
		5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229	278	439	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	164	93	277	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	65	271	°C/W
ΨЈТ	Junction-to-top characterization parameter	44	2	84	°C/W
ΨЈВ	Junction-to-board characterization parameter	62	64	271	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	_	-	-	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

Product Folder Links: SN74LVC1G32-Q1



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	-40°0	C to 85°C	−40°C RECO	UNIT			
			MIN	TYP ⁽¹⁾ MAX	MIN	TYP	MAX		
	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1		V _{CC} - 0.1				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		1.2				
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		1.9			.,	
V _{OH}	I _{OH} = -16 mA	3 V	2.4		2.4			V	
	$I_{OH} = -24 \text{ mA}$	3 V	2.3		2.3				
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		3.8				
	I _{OL} = 100 μA	1.65 V to 5.5 V		0.1			0.1		
	I _{OL} = 4 mA	1.65 V		0.45			0.45		
V	I _{OL} = 8 mA	2.3 V		0.3			0.4	0.4 V	
V _{OL}	I _{OL} = 16 mA	3 V		0.4			0.5	V	
	I _{OL} = 24 mA	3 V		0.55			0.65		
	I _{OL} = 32 mA	4.5 V		0.55			0.65		
I _I A or B inputs	V _I = 5.5 V or GND	0 to 5.5 V		±5			±5	μΑ	
I _{off}	V _I or V _O = 5.5 V	0		±10			±25	μΑ	
I _{CC}	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		10			10	μΑ	
Δl _{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V	500				500	μA	
C _i	$V_I = V_{CC}$ or GND	3.3 V		4		4		pF	

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

6.6 Switching Characteristics, $C_L = 15 pF$

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3)

						-40°C t	o 85°C				
PARAMETER FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Υ	1.9	7.2	8.0	4.4	0.9	3.6	0.8	3.4	ns

6.7 Switching Characteristics, 1.8 V and 2.5V

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted)⁽¹⁾ (see Figure 4)

	DADAMETED		FROM TO (OUTPUT)	-40°C to 85°C -40°C to RECOMM			–40°C to	85°C	-40°C to			
		FROM (INPUT)		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.5 V ± 0.2 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	t_{pd}	A or B	Υ	2.8	8	2.8	9	1.2	5.5	1.2	6	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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6.8 Switching Characteristics, 3.3 V and 5 V

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted)⁽¹⁾ (see Figure 4)

FDG			-40°C to 85°C		-40°C to 125°C RECOMMENDED		–40°C to 85°C		-40°C to 125°C RECOMMENDED		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Υ	1.1	4.5	1	4	1	4	1	4.5	ns

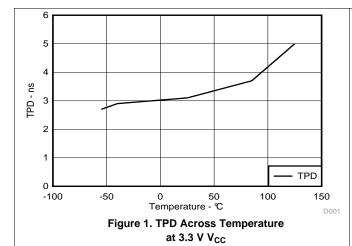
⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested

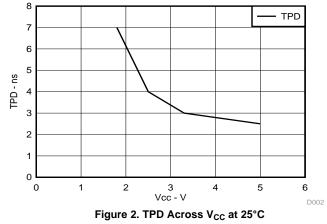
6.9 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST	V _{CC} = 1.8 V	$V_{CC} = 2.5 V$	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
	FARAMETER	CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C_{po}	d Power dissipation capacitance	f = 10 MHz	20	20	21	22	pF

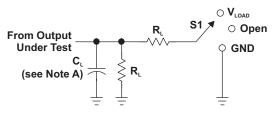
6.10 Typical Characteristics







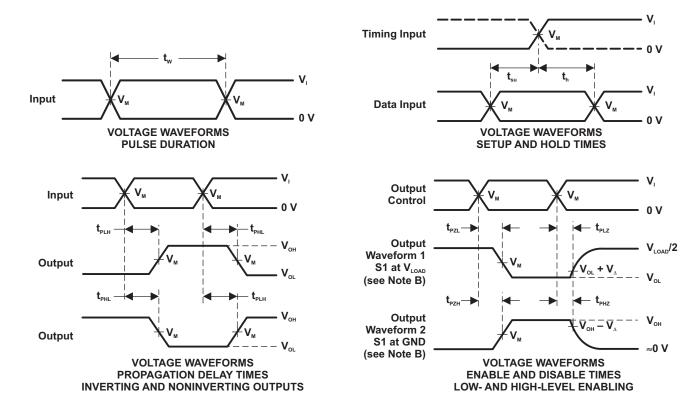
7 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INPUTS			V		_	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _⊾	V _Δ
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
$2.5~\textrm{V}~\pm~0.2~\textrm{V}$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.3 V



NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{\circ} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}.$
- G. t_{PlH} and t_{PHl} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

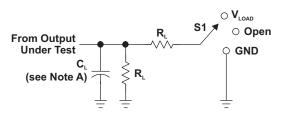
Figure 3. Load Circuit and Voltage Waveforms

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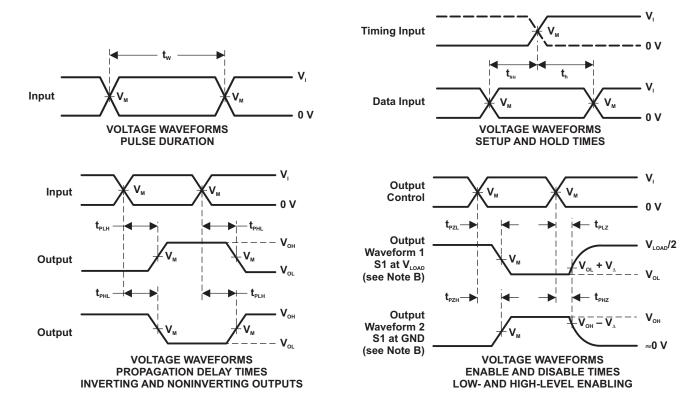
Parameter Measurement Information (continued)



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INPUTS		.,	.,		_	.,	
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	$R_{\scriptscriptstyle L}$	$V_{\scriptscriptstyle{\Delta}}$	
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V	
$2.5~\textrm{V}~\pm~0.2~\textrm{V}$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V	
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V	



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. $t_{\text{PLH}}^{\text{F2L}}$ and $t_{\text{PHL}}^{\text{F2L}}$ are the same as $t_{\text{pd}}^{\text{eff}}$
- H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

The SN74LVC1G32-Q1 device contains one 2-input positive OR gate device and performs the Boolean function $Y = A + B \text{ or } Y = \overline{A \cdot B}$ This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

- · Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

8.4 Device Functional Modes

Table 1. Function Table

INP	UTS	OUTPUT
Α	В	Υ
Н	X	Н
X	Н	Н
L	L	L

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G32-Q1 device is a high drive CMOS device that can be used for implementing OR logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing translation down to $V_{\rm CC}$.

9.2 Typical Application

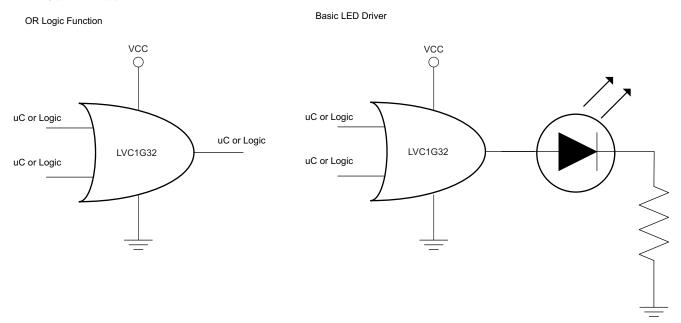


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions:
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in the *Recommended Operating Conditions* table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating
 Conditions table at any valid V_{CC}.

2. Recommend Output Conditions:

 Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table.

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Typical Application (continued)

Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

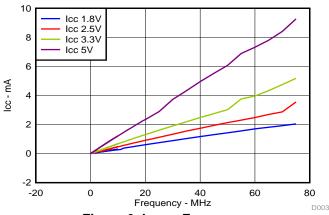


Figure 6. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended. If there are multiple VCC pins, then a 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used, or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Layout Example are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever make more sense or is more convenient.

11.2 Layout Example

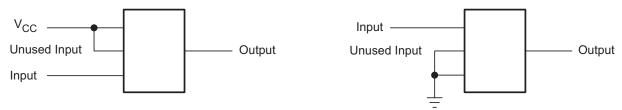


Figure 7. Layout Example

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community T's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC1G32-Q1

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www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(5)	(4)	(5)		(0)
74LVC1G32QDBVRQ1G4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34P5, C32O)
74LVC1G32QDBVRQ1G4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34P5, C32O)
SN74LVC1G32QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34P5, C32O)
SN74LVC1G32QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34P5, C32O)
SN74LVC1G32QDBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34P5, C32O)
SN74LVC1G32QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CGJ, CGO)
SN74LVC1G32QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CGJ, CGO)
SN74LVC1G32QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CGJ, CGO)
SN74LVC1G32QDRYRQ1	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FW
SN74LVC1G32QDRYRQ1.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FW

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G32-Q1:

Catalog : SN74LVC1G32

● Enhanced Product: SN74LVC1G32-EP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G32QDBVRQ1G4	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G32QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G32QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G32QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)			
74LVC1G32QDBVRQ1G4	SOT-23	DBV	5	3000	190.0	190.0	30.0			
SN74LVC1G32QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0			
SN74LVC1G32QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0			
SN74LVC1G32QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0			





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





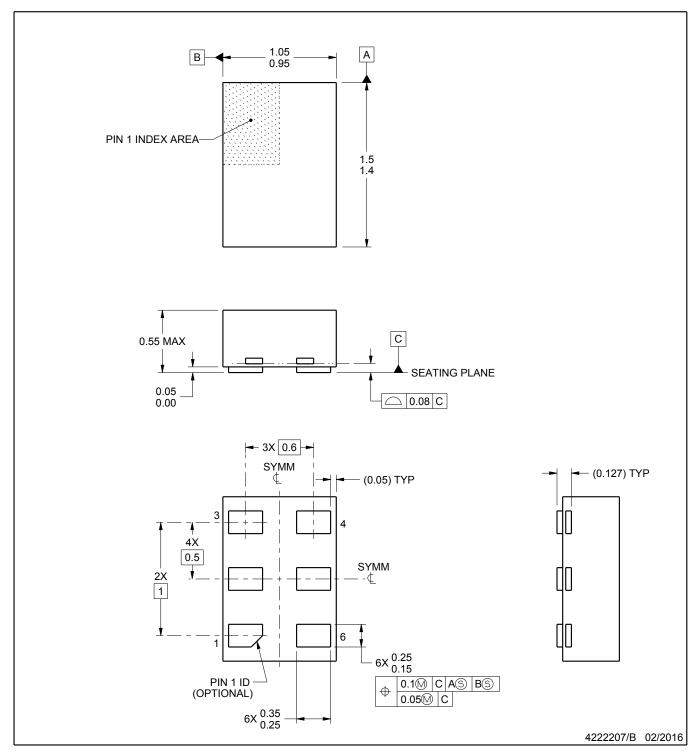
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.







PLASTIC SMALL OUTLINE - NO LEAD



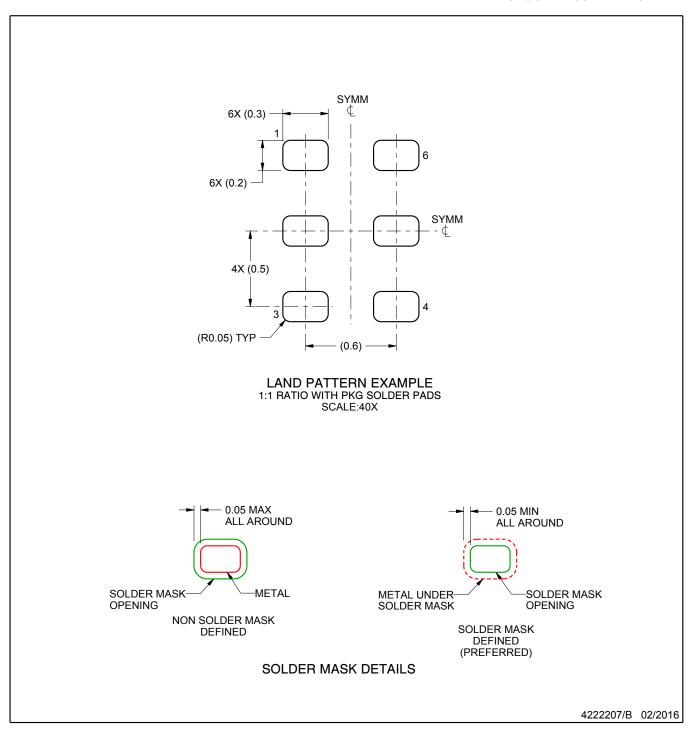
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.



PLASTIC SMALL OUTLINE - NO LEAD

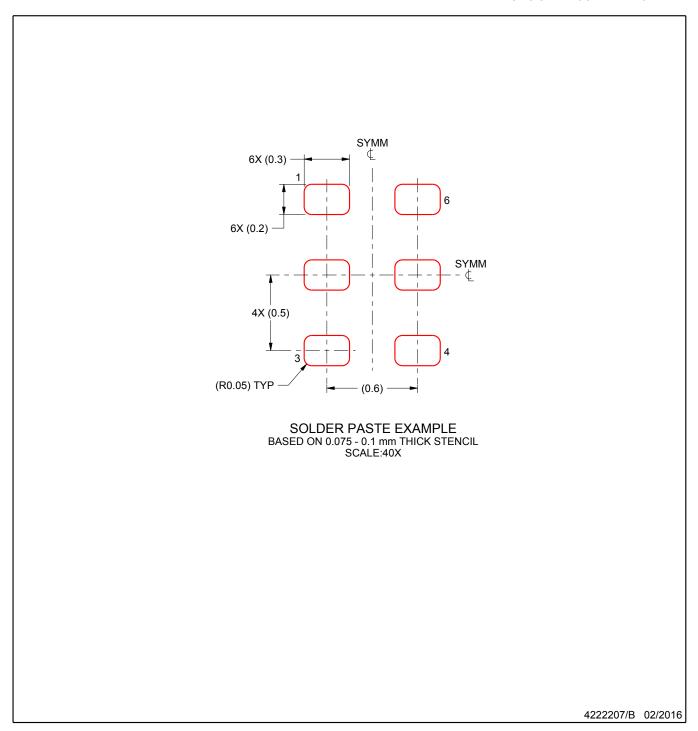


NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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