SN74LVC1G18 1-of-2 Noninverting Demultiplexer With 3-State Deselected Output

1 Features

- Operating temperature from –40°C to +125°C
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Supports down translation to V_{CC}
- Max t_{pd} of 3.4 ns at 3.3 V
- Low power consumption, 10-µA max I_{CC}
- ±24-mA Output drive at 3.3 V
- Typical V_{OLP} (output ground bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V Human-body model (A114-A)
  - 200-V machine model (A115-A)
  - 1000-V Charged-device model (C101)

2 Applications

- Data center switch
- Baseband unit (BBU)
- Wi-Fi access point
- Notebook PC
- Active antenna system (AAS)
- Appliances
- Industrial monitor
- Coffee machine
- Wired speaker
- Vacuum robot
- Professional audio interface

3 Description

This non-inverting demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G18 device is a 1-of-2 non-inverting demultiplexer with a 3-state output. This device buffers the data on input A and passes it to either output Y0 or Y1, depending on whether the state of the select (S) input is low or high, respectively.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

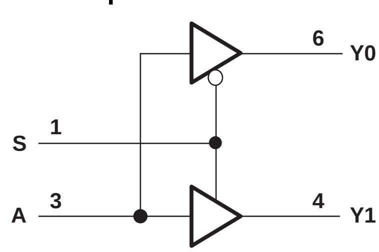
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G18DBVR	SOT-23 (6)	2.90 mm × 2.80 mm
SN74LVC1G18DCKR	SC70 (6)	2.00 mm × 1.10 mm
SN74LVC1G18DRYR	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G18DSFR	SON (6)	1.00 mm × 1.00 mm
SN74LVC1G18YZPR	DSBGA (6)	1.39 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

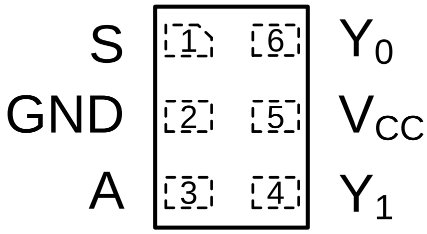
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (July 2012) to Revision L **Page**

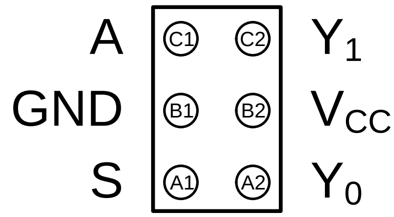
- Updated document to new TI data sheet format. ... 1
- Deleted Ordering Information table. ... 1
- Updated I_{off} in Features. ... 1
- Added Applications. ... 1
- Added Device Information table. ... 1
- Added Operating junction temperature ... 5
- Added Handling Ratings table. ... 5
- Added Thermal Information table. ... 6

5 Pin Configuration and Functions

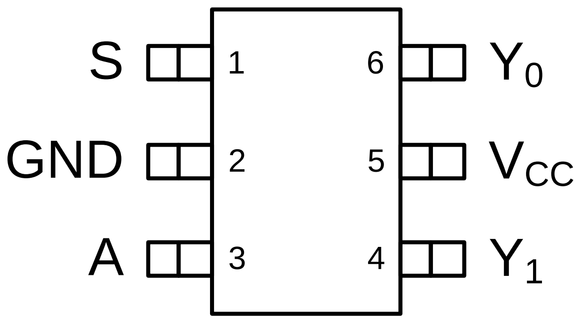
DRY and DSF Package
6-Pin SON
Transparent Top View



YZP Package
6-Pin DSBGA
Bottom View



DBV and DCK Package
6-Pin SOT-23 and SC70
Top View

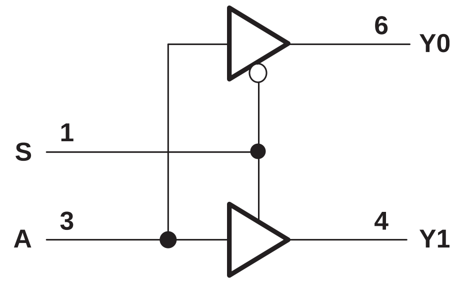


Not to scale. See the mechanical drawings at the end of the data sheet for package dimensions.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV, DCK, DRY, DSF	YZP		
S	1	A1	Input	Active output selection (LOW = Y0, HIGH = Y1)
GND	2	B1	—	Ground
A	3	C1	Input	Input A
Y_1	4	C2	Output	Output Y_1
V_{CC}	5	B2	—	Positive supply
Y_0	6	A2	Output	Output Y_0

Logic Diagram (Positive Logic)



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(3)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)(1)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Operating junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1G18					UNIT
		DBV	DCK	DRY	DSF	YZP	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	236.1	278.7	306.7	300.3	123.8	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	174.0	217.8	207.2	183.5	1.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	111.5	124.6	181.1	170.7	38.9	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	93.5	105.2	49.9	24.2	0.5	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	111.2	124.1	180.3	170.2	38.9	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40 to 85°C MIN	-40 to 85°C TYP(1)	-40 to 85°C MAX	-40 to 125°C MIN	-40 to 125°C TYP(1)	-40 to 125°C MAX	UNIT
V_{OH}	I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OH} = –4 mA	1.65 V	1.2			1.2			
	I_{OH} = –8 mA	2.3 V	1.9			1.9			
	I_{OH} = –16 mA	3 V	2.4			2.4			
	I_{OH} = –24 mA		2.3			2.3			
	I_{OH} = –32 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
	I_{OL} = 4 mA	1.65 V			0.45			0.45	
	I_{OL} = 8 mA	2.3 V			0.3			0.3	
	I_{OL} = 16 mA	3 V			0.4			0.4	
	I_{OL} = 24 mA				0.55			0.55	
	I_{OL} = 32 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}	V_I or V_O = 5.5 V	0			±10			±10	µA
I_{OZ}	V_O = 0 to 5.5 V	3.6 V			10			10	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	µA
C_I	V_I = V_{CC} or GND	3.3 V		4			4		pF
C_o	V_O = V_{CC} or GND	3.3 V		6			6		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, –40 to 85°C

T_A = –40 to 85°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITION	V_{CC} = 1.8 V ± 0.15 V MIN	V_{CC} = 1.8 V ± 0.15 V MAX	V_{CC} = 2.5 V ± 0.2 V MIN	V_{CC} = 2.5 V ± 0.2 V MAX	V_{CC} = 3.3 V ± 0.3 V MIN	V_{CC} = 3.3 V ± 0.3 V MAX	V_{CC} = 5 V ± 0.5 V MIN	V_{CC} = 5 V ± 0.5 V MAX	UNIT
t_{pd}	A	Y	C_L = 15 pF	2.3	8.4	1.1	4.2	1.1	3.4	0.8	2.7	ns
			C_L = 30 pF or 50 pF	3.5	9.3	1.7	5	1.5	4.2	0.7	3.2	ns
t_{en}	S	Y	C_L = 30 pF or 50 pF	3.6	10.2	1.7	5.6	1.5	4.6	0.9	3.4	ns
t_{dis}	S	Y	C_L = 30 pF or 50 pF	1.9	12.7	1	5.3	1.1	4.9	0.5	3.3	ns

6.7 Switching Characteristics, –40 to 125°C

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITION	V_{CC} = 1.8 V ± 0.15 V MIN	V_{CC} = 1.8 V ± 0.15 V MAX	V_{CC} = 2.5 V ± 0.2 V MIN	V_{CC} = 2.5 V ± 0.2 V MAX	V_{CC} = 3.3 V ± 0.3 V MIN	V_{CC} = 3.3 V ± 0.3 V MAX	V_{CC} = 5 V ± 0.5 V MIN	V_{CC} = 5 V ± 0.5 V MAX	UNIT
t_{pd}	A	Y	C_L = 30 pF or 50 pF	3.5	9.8	1.7	5.5	1.5	4.7	0.7	3.7	ns
t_{en}	S	Y	C_L = 30 pF or 50 pF	3.6	11.2	1.7	6.6	1.5	6.1	0.9	4.9	ns
t_{dis}	S	Y	C_L = 30 pF or 50 pF	1.9	13.7	1	6.3	1.1	6.4	0.5	4.8	ns

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	17	17	18	21	pF

6.9 Typical Characteristics

T_A = 25°C; Simulated data

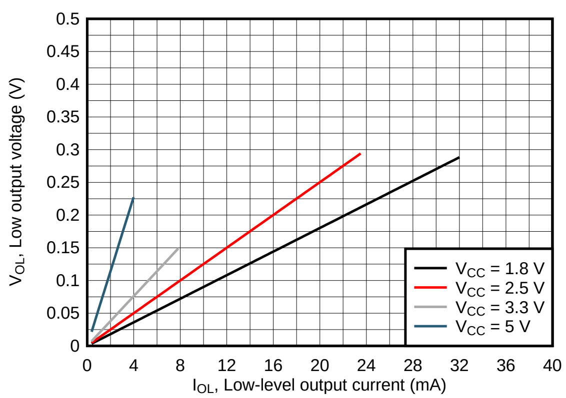


Figure 1. Typical low-level output voltage at common supply values and currents

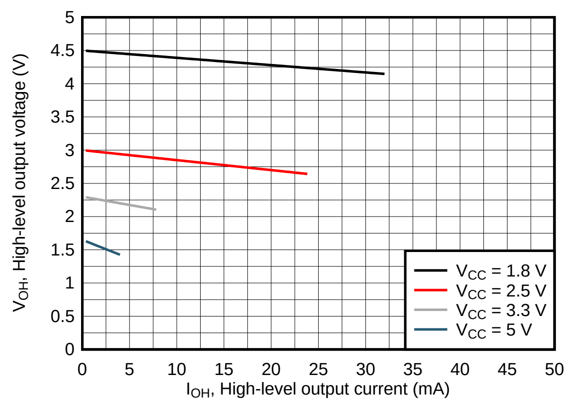
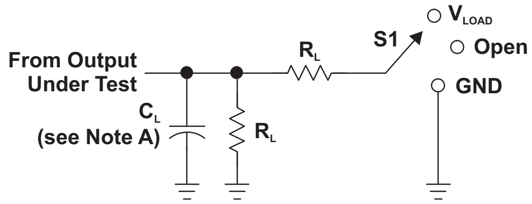


Figure 2. Typical high-level output voltage at common supply values and currents

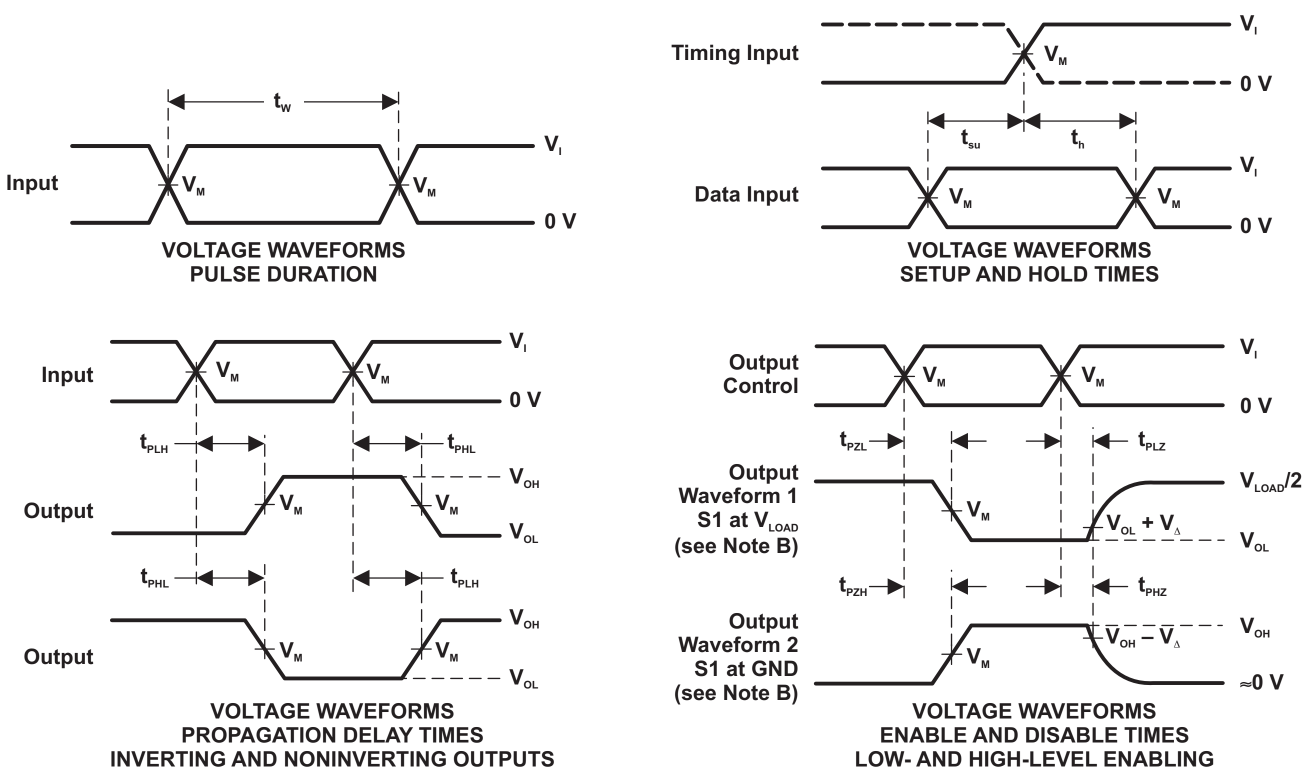
7 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

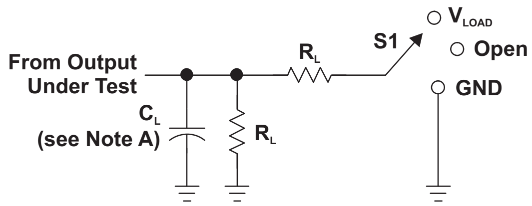
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

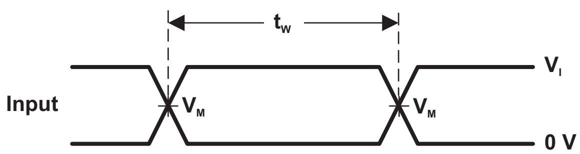
Parameter Measurement Information (continued)



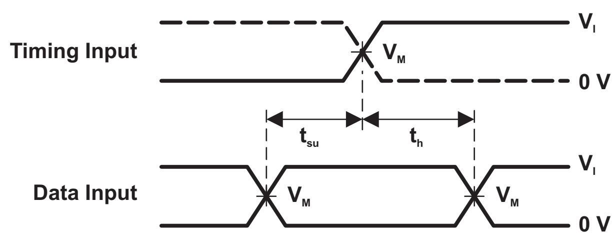
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

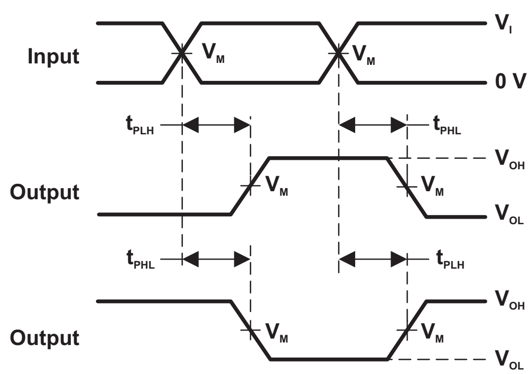
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



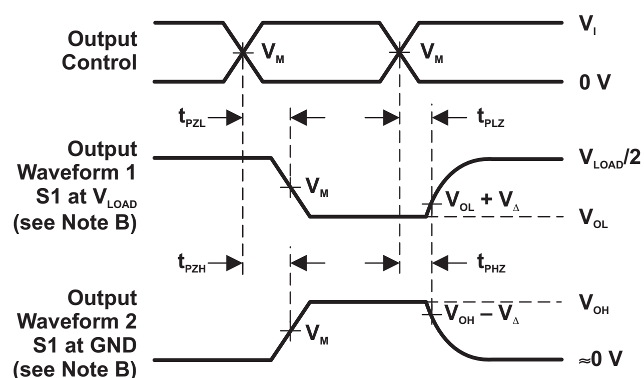
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

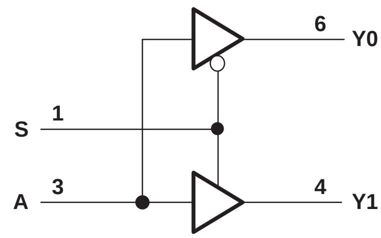
Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This device contains one independent 1-of-2 noninverting demultiplexer with high-impedance outputs when disabled.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

3-State outputs can be placed into a high-impedance state. In this state, the output will neither source nor sink current, and leakage current is defined by the I_{OZ} specification in the *Electrical Characteristics*. A pull-up or pull-down resistor can be used to ensure that the output remains HIGH or LOW, respectively, during the high-impedance state.

8.3.2 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.3 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* , and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions* .

8.3.5 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in Figure 5.

Feature Description (continued)

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

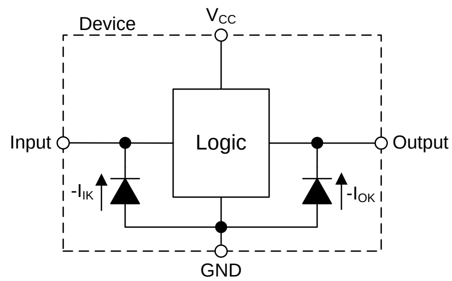


Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUTS	
S	A	Y0	Y1
L	L	L	Z
L	H	H	Z
H	L	Z	L
H	H	Z	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G18 can be used to select between controlling two analog switches. In this use case, pull-down resistors are connected to both outputs of the SN74LVC1G18 to ensure that a valid state is available for the inputs to the switches at all times. This defaults the switches into the "off" state to prevent unwanted data transmission.

9.2 Typical Application

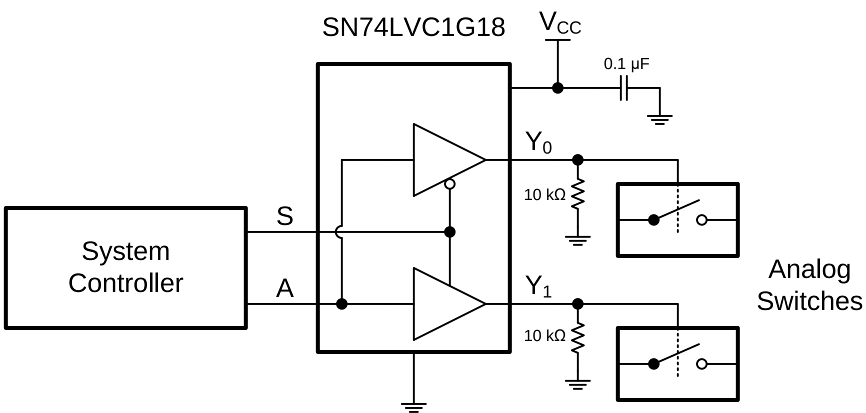


Figure 6. Typical application block diagram

9.2.1 Design Requirements

- Each analog switch must be controlled by the system controller, but only when the other switch is disabled.
- When the input S is low, the Y_0 output is selected and the Y_1 output is in the high impedance state
- When the input S is high, the Y_1 output is selected and the Y_0 output is in the high impedance state
- When the input A is high, the selected analog switch must be closed
- When the input A is low, the selected analog switch must be open

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions* . The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC1G18 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings* .

The SN74LVC1G18 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

Typical Application (continued)

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and C_{pd} Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

> **CAUTION**
>
> The maximum junction temperature, T_J(max) listed in the *Absolute Maximum Ratings* , is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings* . These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74LVC1G18, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74LVC1G18 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions* .

Refer to the *Feature Description* for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*. The plots in the *Typical Characteristics* provide a relationship between output voltage and current for this device.

Unused outputs can be left floating.

Refer to *Feature Description* for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC1G18 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / 25 mA) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*

Typical Application (continued)

9.2.3 Application Curves

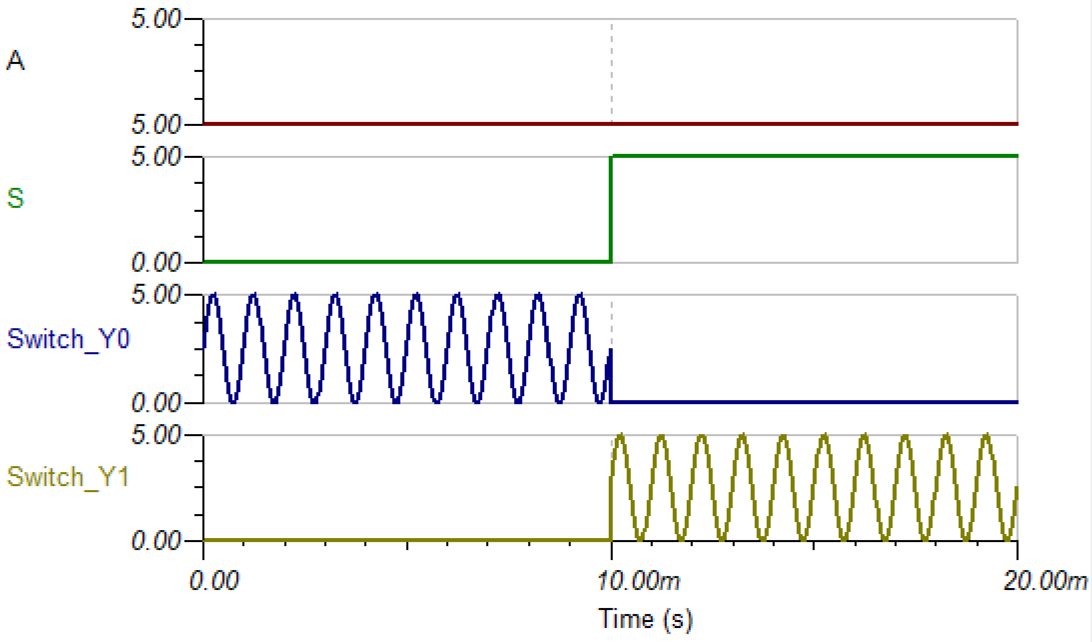


Figure 7. Simulated application transient response

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* . Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in Figure 8.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

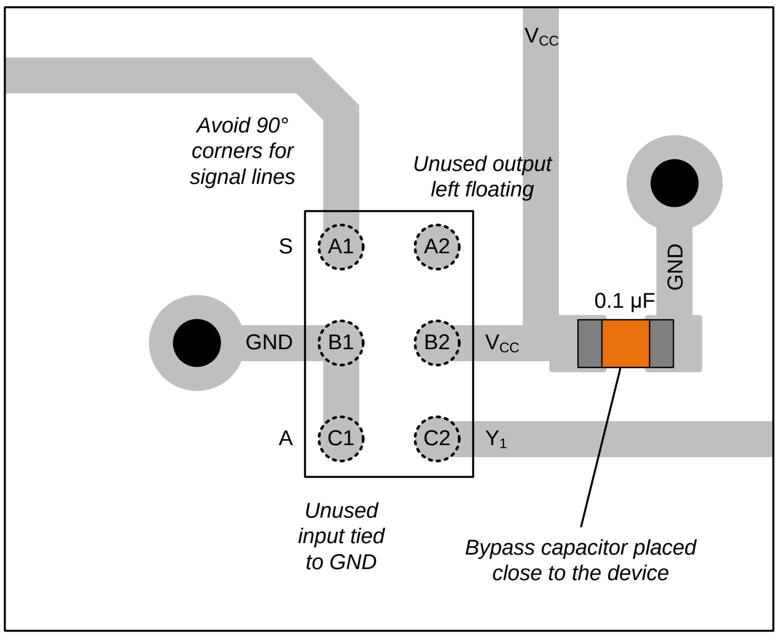


Figure 8. Example layout for the SN74LVC1G18

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*
- *CMOS Power Consumption and C_{pd} Calculation*
- *Understanding and Interpreting Standard-Logic Data Sheets*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G18DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C185, C18R)
SN74LVC1G18DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C185, C18R)
SN74LVC1G18DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C185, C18R)
SN74LVC1G18DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CJ5, CJF, CJJ, CJ K, CJR)
SN74LVC1G18DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CJ5, CJF, CJJ, CJ K, CJR)
SN74LVC1G18DCKRE4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ5
SN74LVC1G18DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ5
SN74LVC1G18DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ5
SN74LVC1G18DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ
SN74LVC1G18DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ
SN74LVC1G18DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ
SN74LVC1G18DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ
SN74LVC1G18YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CJN
SN74LVC1G18YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CJN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

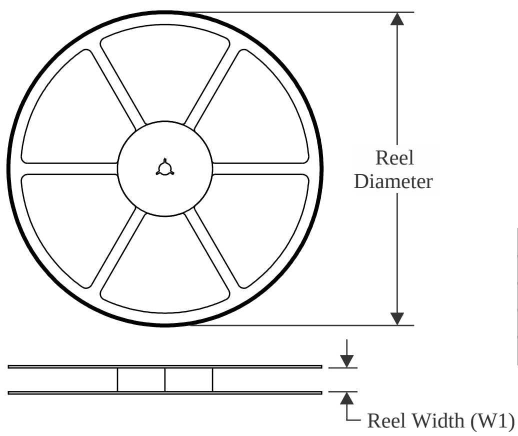
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

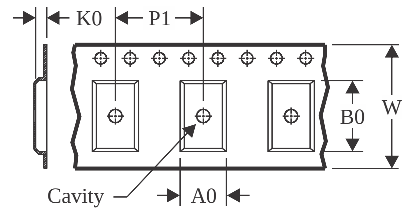
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

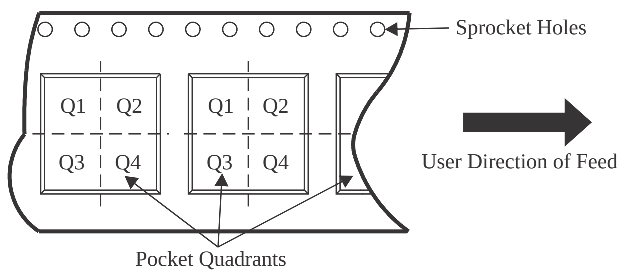


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

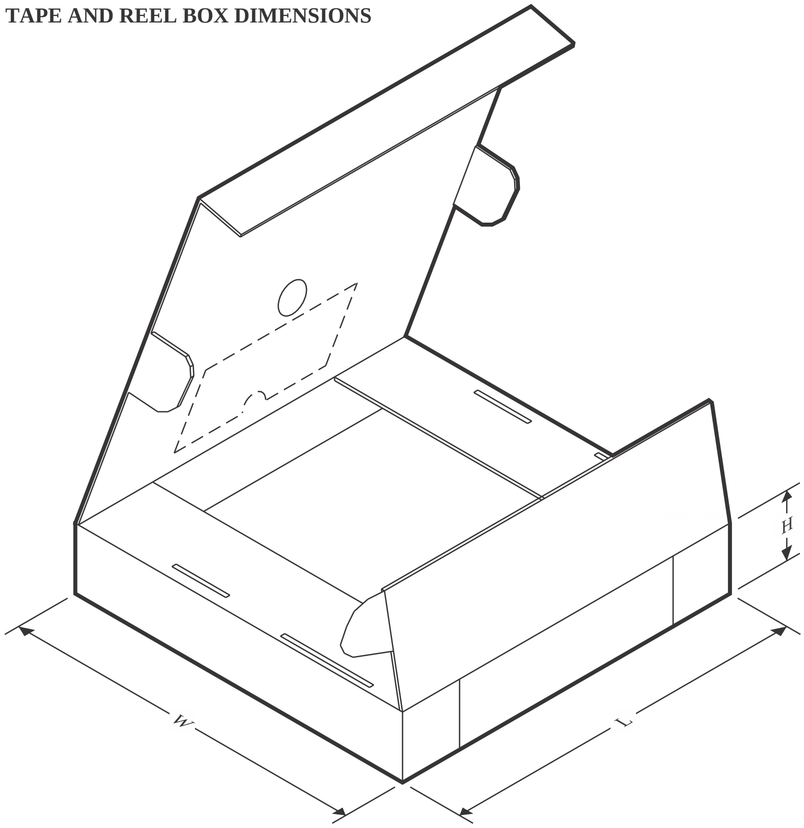
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G18DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G18DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G18DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G18DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G18DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G18DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G18YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



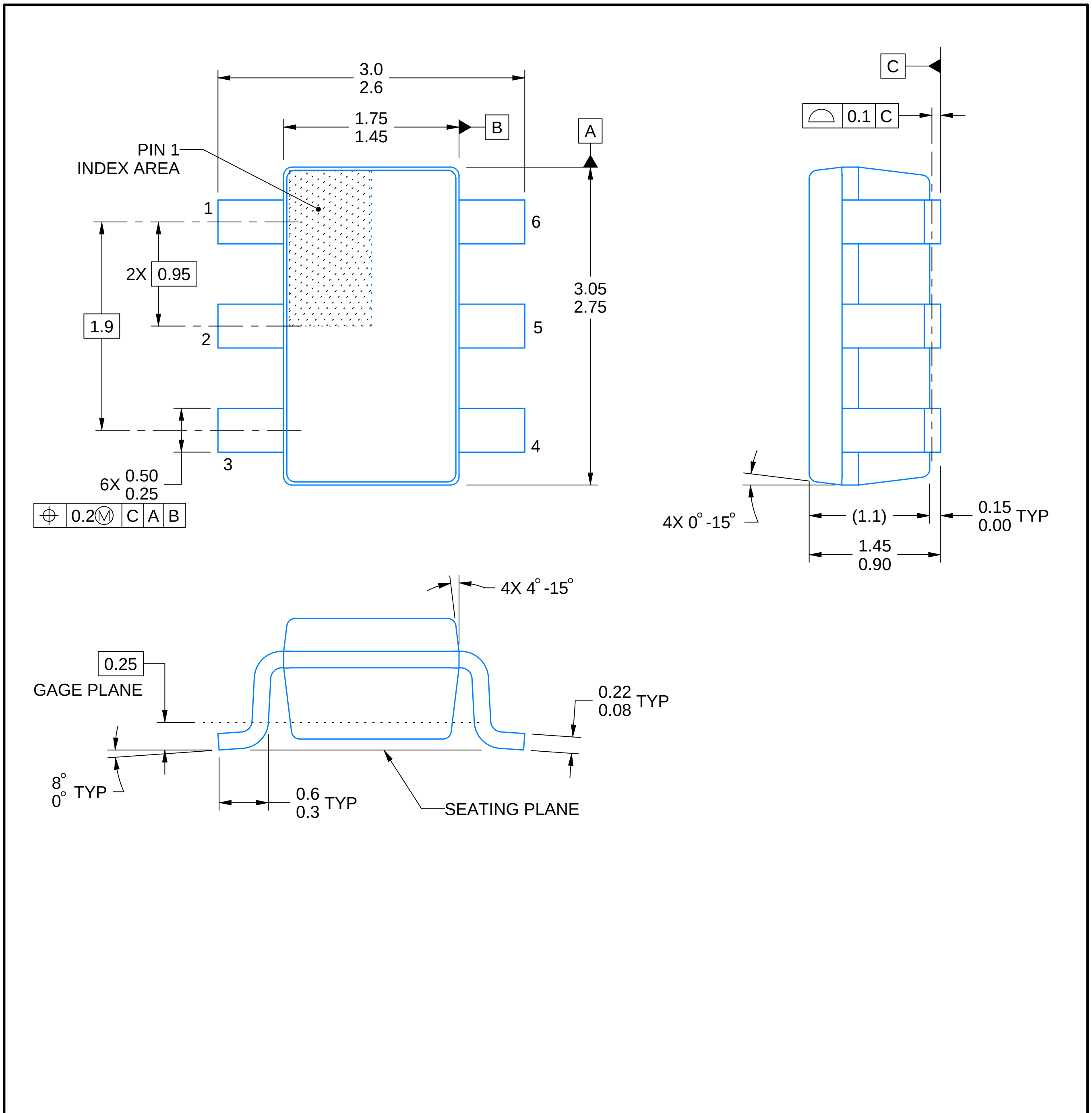
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G18DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G18DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G18DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G18DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G18DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G18DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G18YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV0006A

SOT-23 - 1.45 mm max height

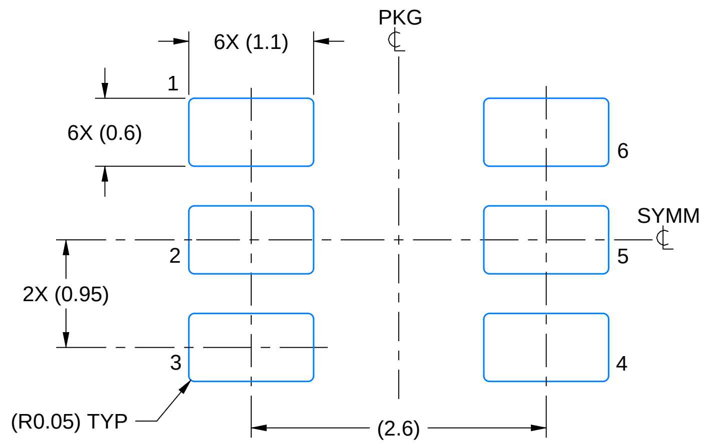
SMALL OUTLINE TRANSISTOR



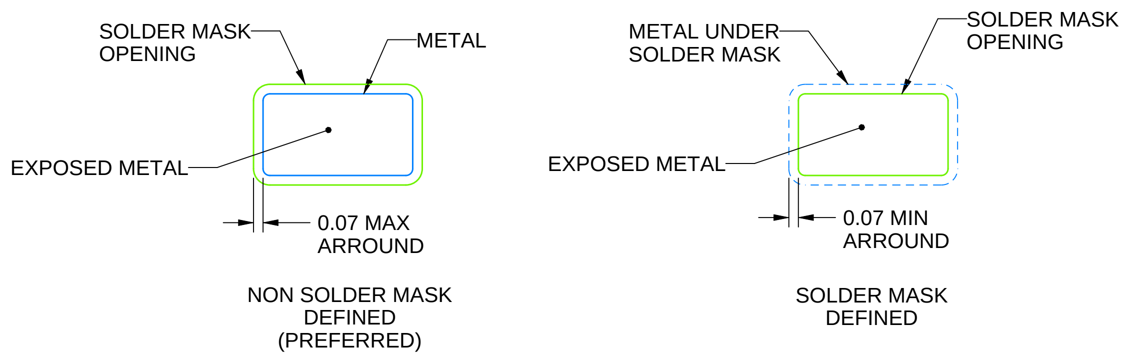
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

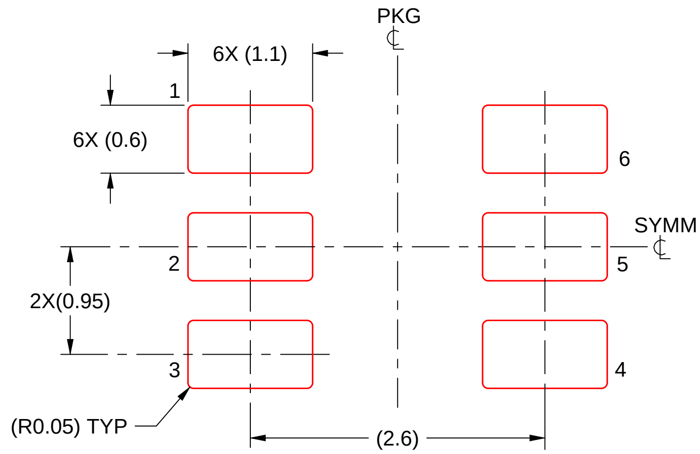


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

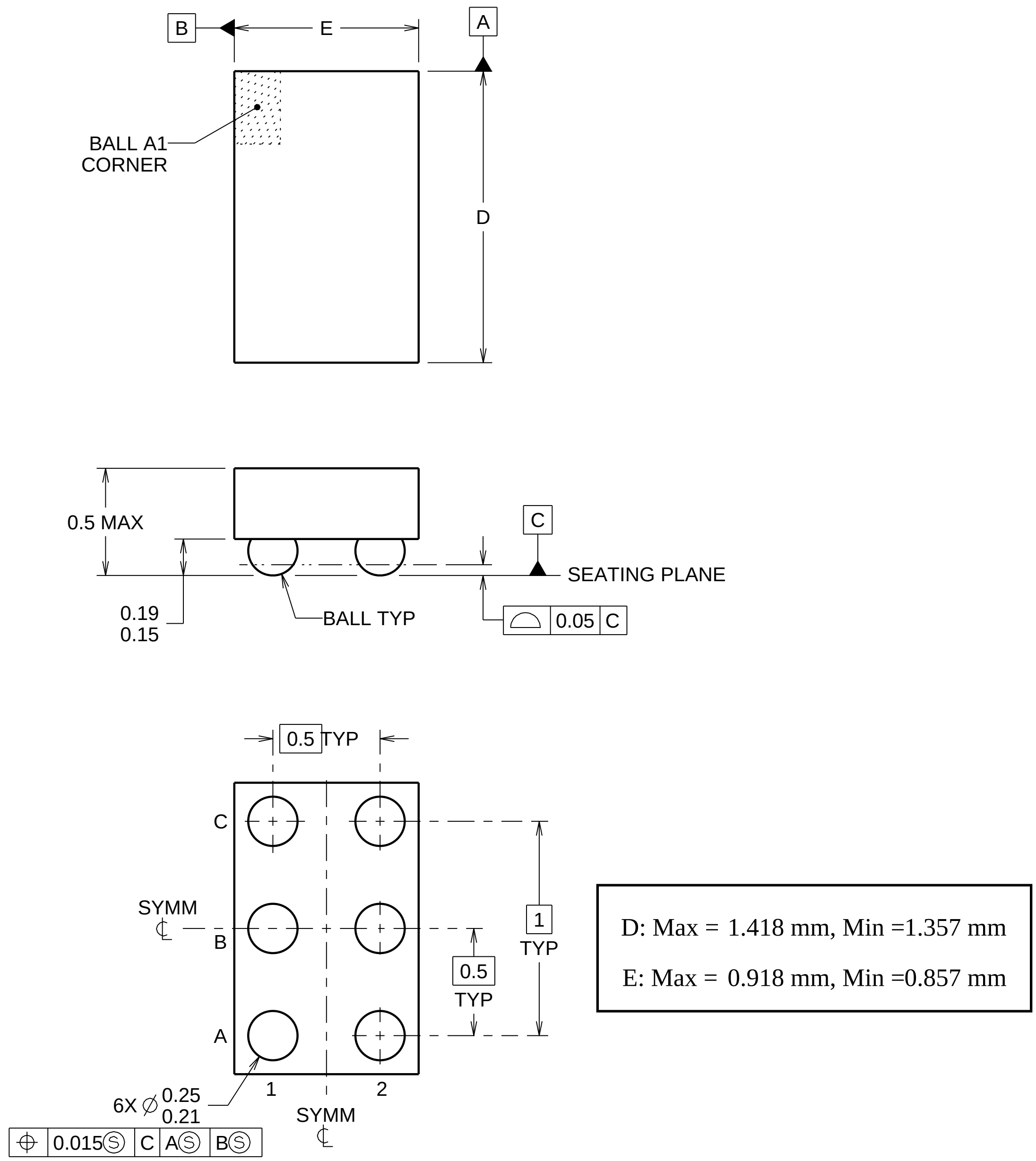


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

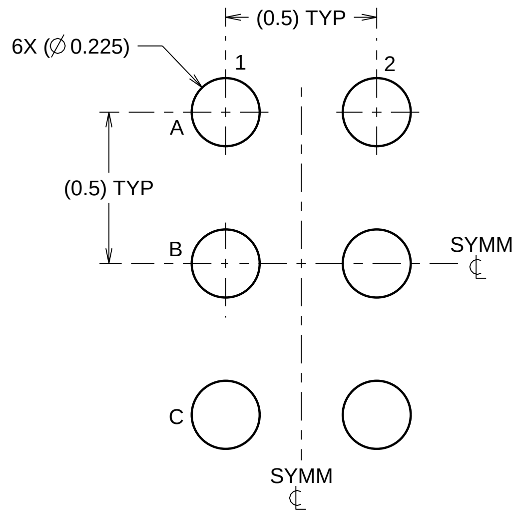


4219524/A 06/2014

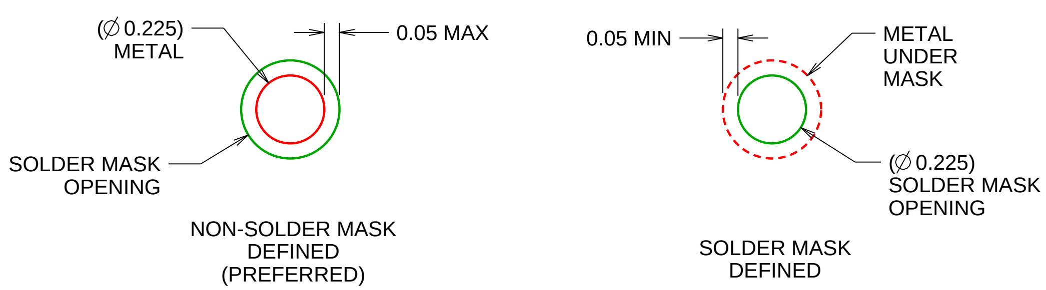
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

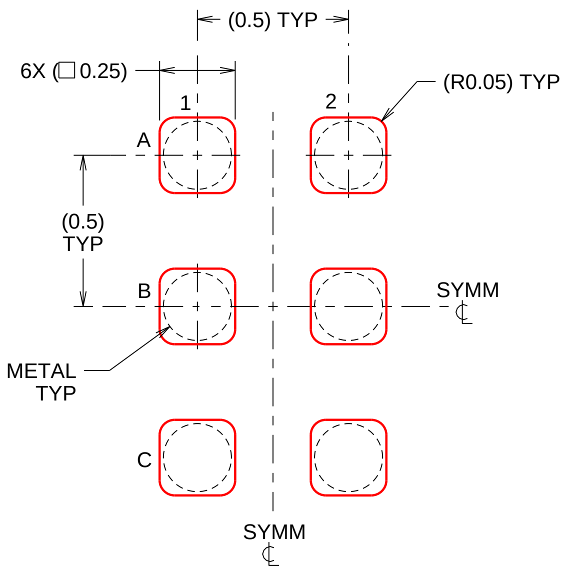


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

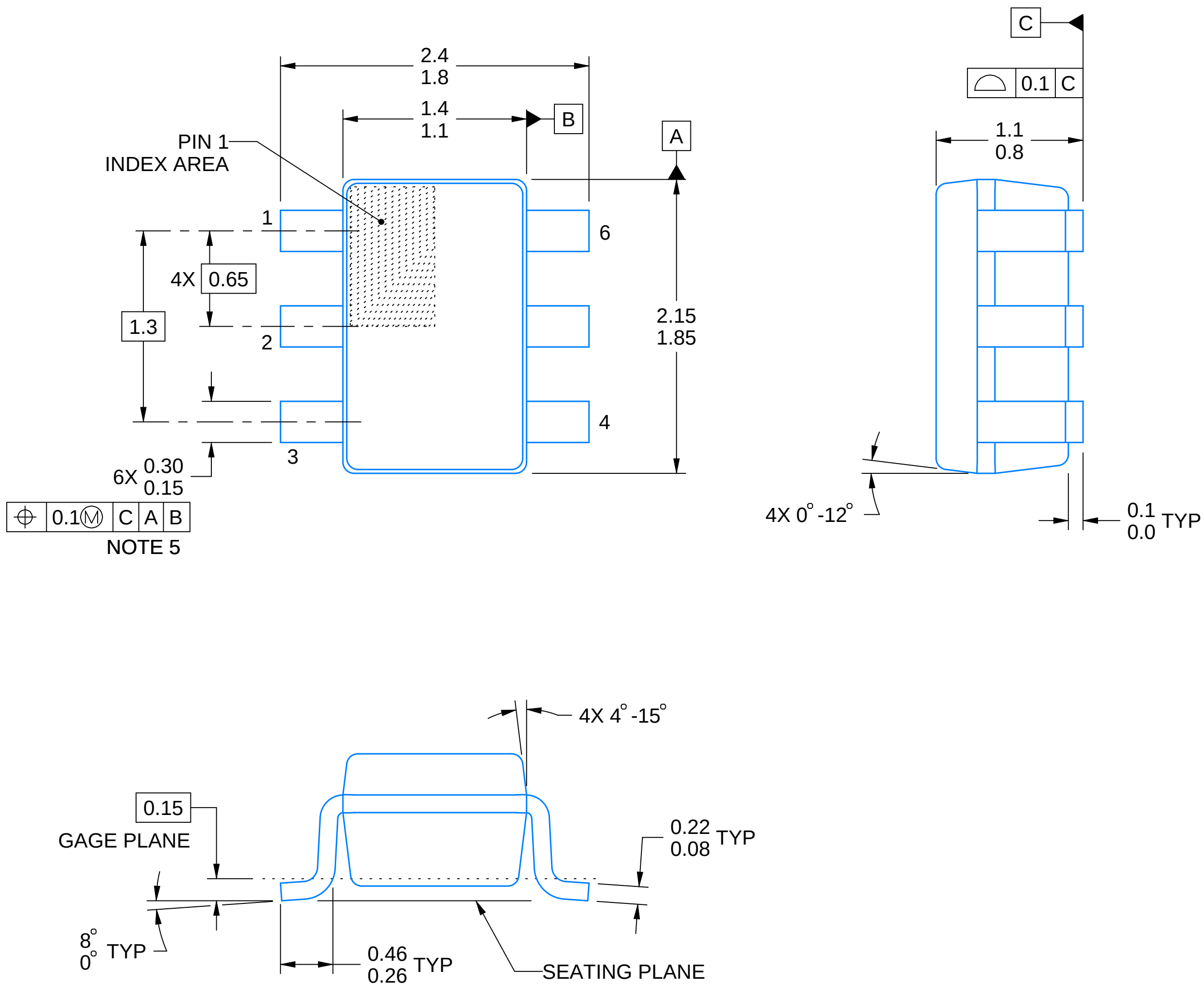


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

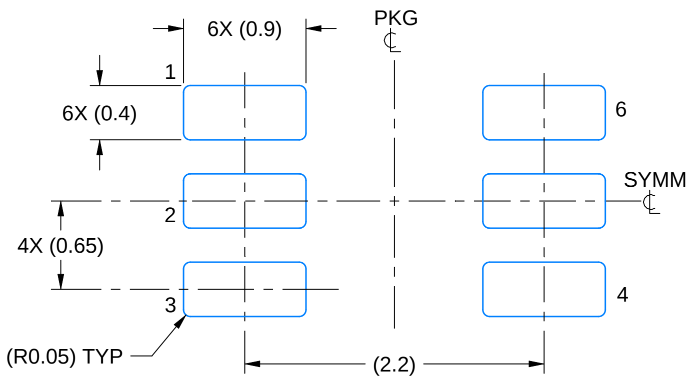
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



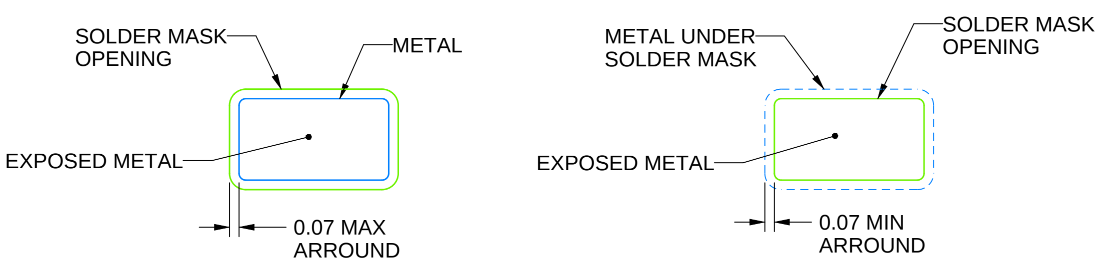
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK DEFINED (PREFERRED)

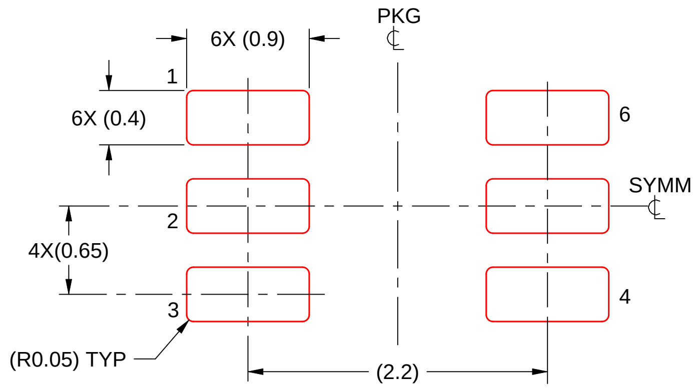
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



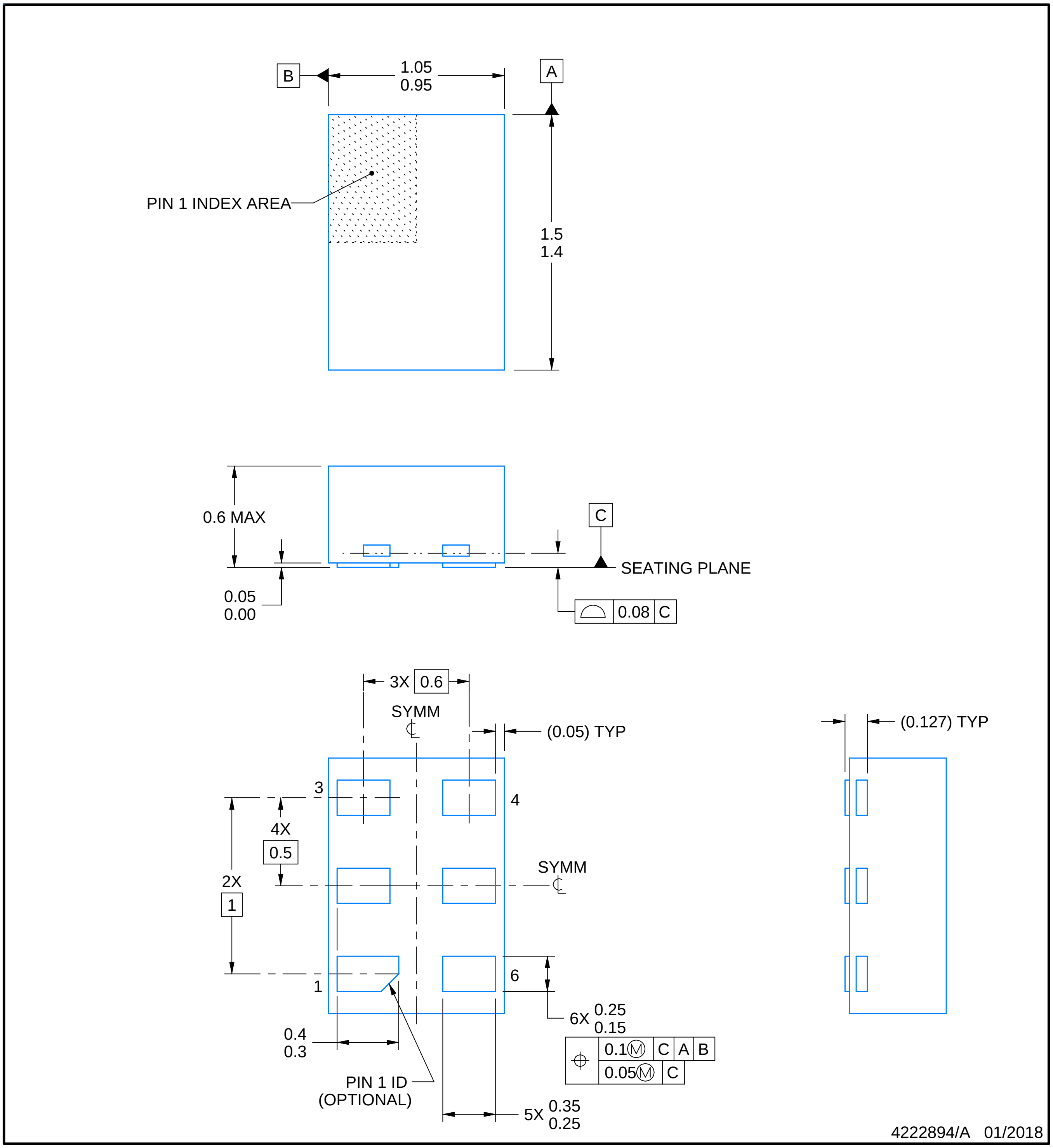
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

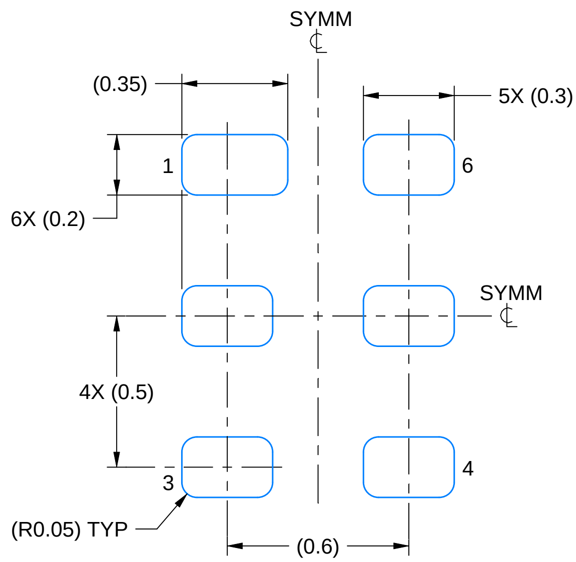
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

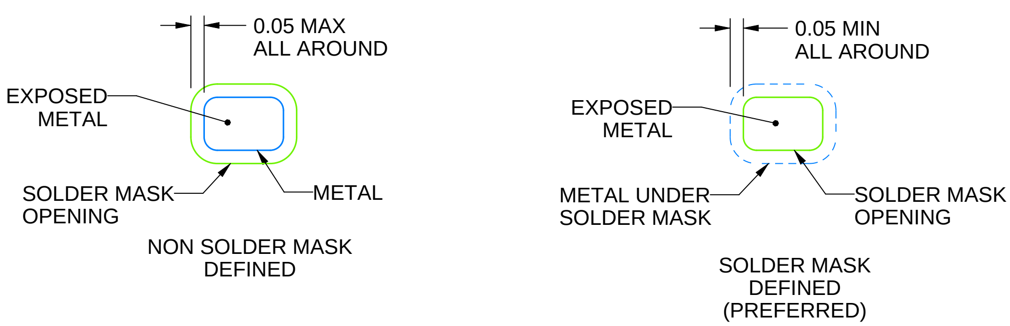


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

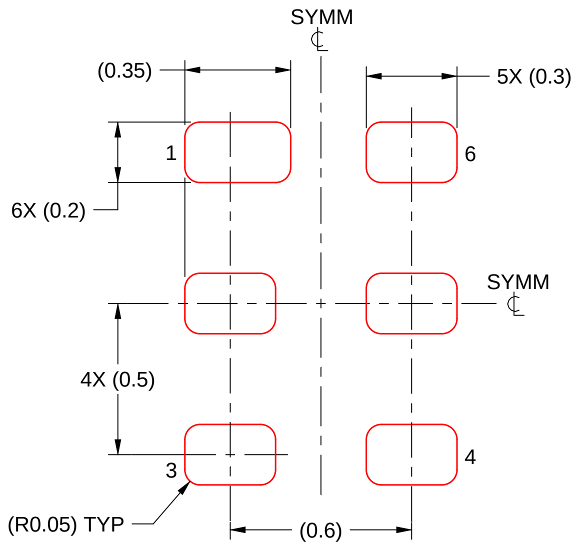


SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

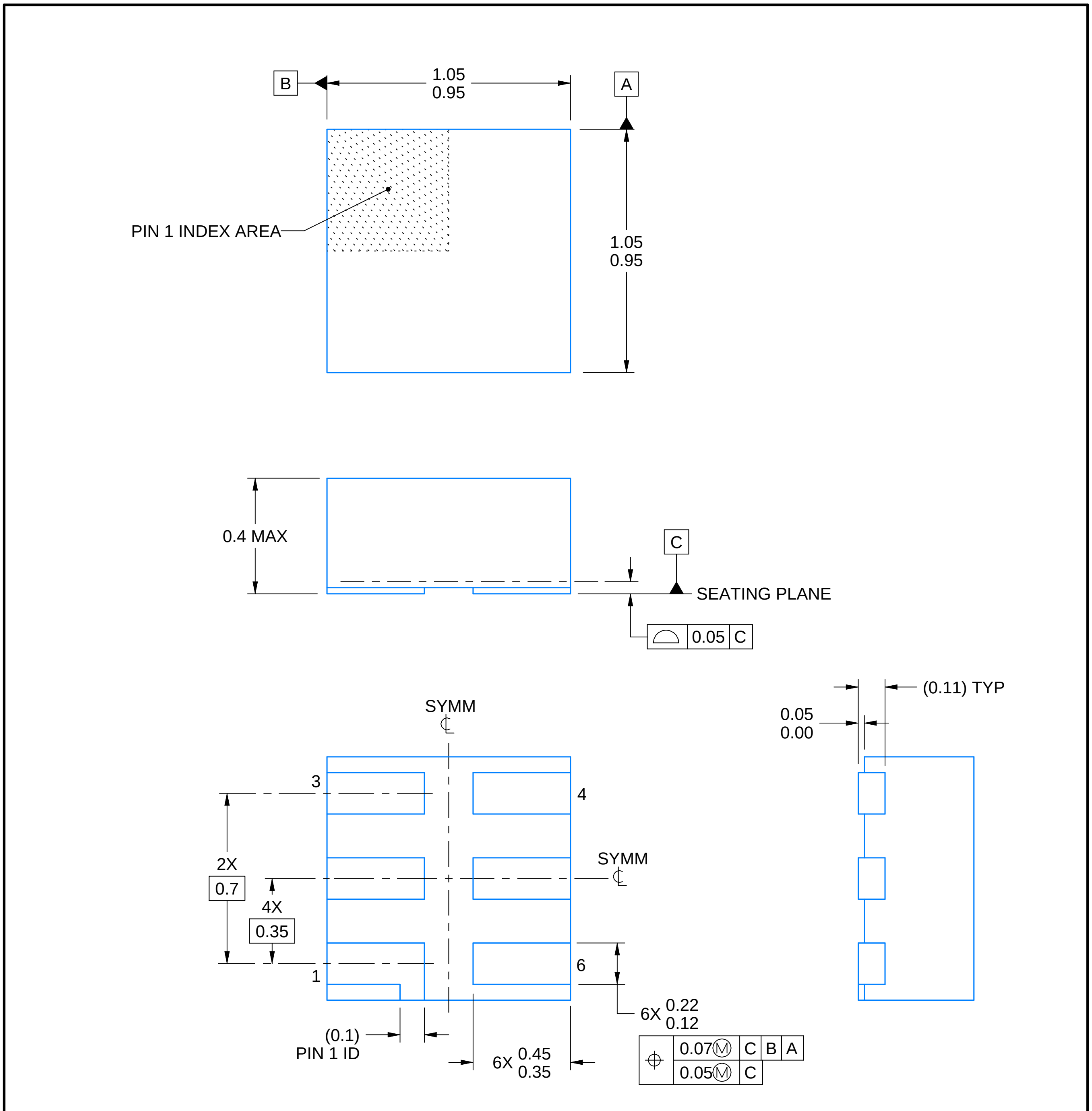


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

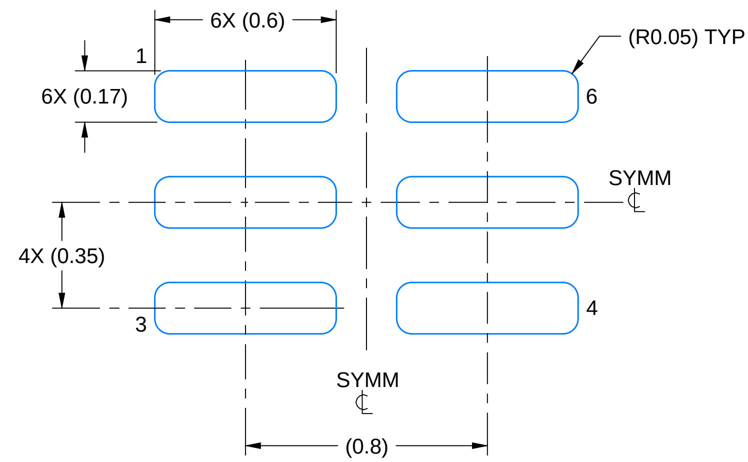
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



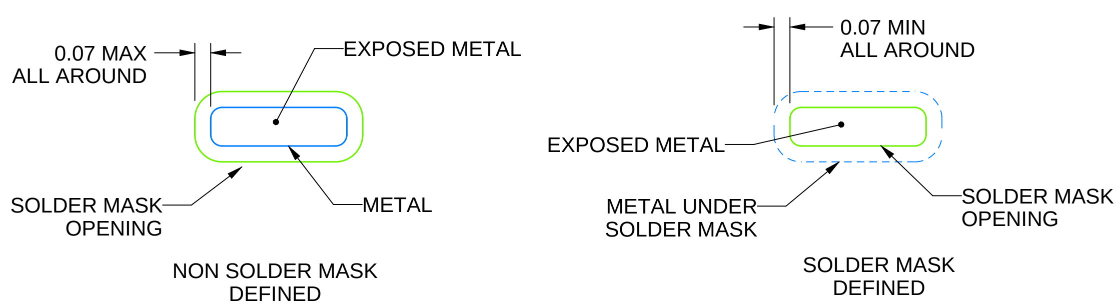
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

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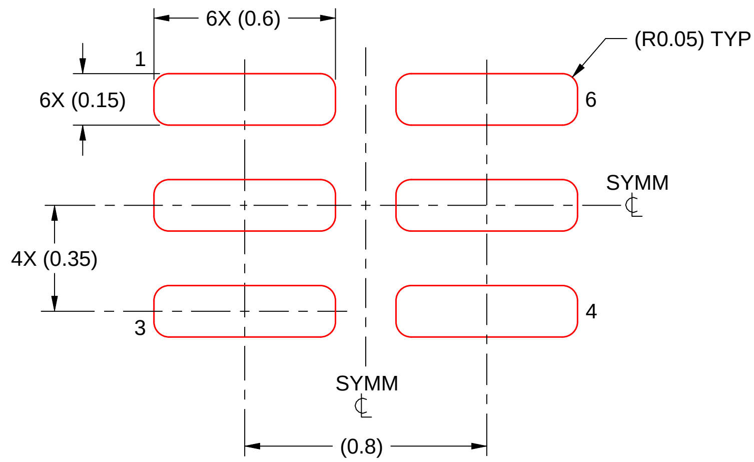
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

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4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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