

SN74LVC1G16 Inverting Buffer with Schmitt-Trigger Input and Open-Drain Output

1 Features

- Operating range from 1.65V to 5.5V
- 5.5V tolerant input pins
- Supports standard pinouts
- Latch-up performance exceeds 100mA per JESD 17

2 Applications

- [Combining power good signals](#)
- [Enable digital signals](#)

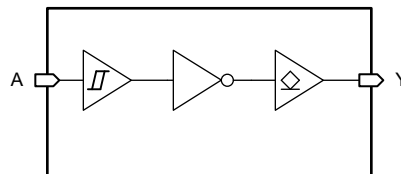
3 Description

The SN74LVC1G16 device is an Inverter Buffer with a Schmitt-Trigger input and an Open-Drain output.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74LVC1G16	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SOT-SC70, 5)	2mm × 2.1mm	2mm × 1.25mm

- (1) For more information, see Section 11.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram



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4 Pin Configuration and Functions

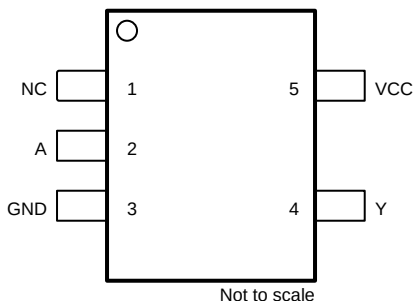


Figure 4-1. SN74LVC1G16 DBV Package, 5-Pin SOT-23 (Top View)

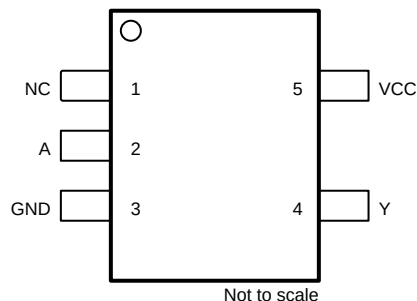


Figure 4-2. SN74LVC1G16 DCK Package, 5-Pin SOT-SC70 (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
NC	1	—	No Connect, Leave floating or connect to ground
A	2	Input	Input A
GND	3	—	Ground
Y	4	Output	Output Y
V _{CC}	5	—	Positive Supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
V _I	Input voltage range ⁽²⁾		-0.5	6.5	V
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
V _O	Output voltage range ⁽²⁾		-0.5	6.5	V
I _{IK}	Input clamp current	V _I < 0 V		-50	mA
I _{OK}	Output clamp current	V _O < 0 V		-50	mA
I _O	Continuous output current			±50	mA
I _O	Continuous output current through V _{CC} or GND			±100	mA
T _J	Junction temperature		-65	150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Functional	1.2		
V _I	Input voltage		0	5.5	V
V _O	Output voltage	(High or low state)	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-8	
		V _{CC} = 3.0 V		-16	
				-24	
		V _{CC} = 4.5 V		-32	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3.0 V		16	
				24	
		V _{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.1 V to 5.5V		100	ms/V

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
T _A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
DBV (SOT-23, 5)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W
DCK (SOT-SC70, 5)	5	371.0	297.5	258.6	195.6	256.2	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V _{T+}	Positive-going input threshold voltage	1.65 V	0.76	1.08	1.16	V
V _{T+}	Positive-going input threshold voltage	2.3 V	1.08	1.35	1.56	V
V _{T+}	Positive-going input threshold voltage	3 V	1.3	1.66	1.92	V
V _{T+}	Positive-going input threshold voltage	4.5 V	2.16	2.37	2.74	V
V _{T+}	Positive-going input threshold voltage	5.5 V	2.61	2.86	3.33	V
V _{T-}	Negative-going input threshold voltage	1.65 V	0.35	0.57	0.7	V
V _{T-}	Negative-going input threshold voltage	2.3 V	0.56	0.79	0.89	V
V _{T-}	Negative-going input threshold voltage	3 V	0.84	1.04	1.2	V
V _{T-}	Negative-going input threshold voltage	4.5 V	1.41	1.59	1.97	V
V _{T-}	Negative-going input threshold voltage	5.5 V	1.71	1.94	2.4	V
ΔV _T	Hysteresis (V _{T+} - V _{T-})	1.65 V	0.3	0.52	0.8	V
ΔV _T	Hysteresis (V _{T+} - V _{T-})	2.3 V	0.4	0.56	0.78	V
ΔV _T	Hysteresis (V _{T+} - V _{T-})	3 V	0.4	0.62	0.87	V
ΔV _T	Hysteresis (V _{T+} - V _{T-})	4.5 V	0.58	0.78	1.04	V
ΔV _T	Hysteresis (V _{T+} - V _{T-})	5.5 V	0.69	0.91	1.14	V
V _{OL}	I _{OL} = 100 μA	Over Recommended Operating Conditions			0.2	V
V _{OL}	I _{OL} = 4 mA	1.65 V			0.45	V
V _{OL}	I _{OL} = 8 mA	2.3 V			0.3	V
V _{OL}	I _{OL} = 12 mA	2.7 V			0.4	V
V _{OL}	I _{OL} = 16 mA	3 V			0.4	V
V _{OL}	I _{OL} = 24 mA	3 V			0.55	V
V _{OL}	I _{OL} = 32 mA	4.5 V			0.55	V
I _I	V _I = V _{CC} or GND	V _{CC} = 0V to 5.5 V		±1	±5	μA
I _{off}	V _I or V _O = V _{CC}	V _{CC} = 0 V		±1	±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	V _{CC} = 1.65 V to 5.5 V		1	10	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND	3.0 V to 5.5 V			500	μA
C _I	V _I = V _{CC} or GND	3.3 V		3.5		pF
C _O	V _O = V _{CC} or GND	3.3 V		6.3		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See [Parameter Measurement Information](#)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$	$1.8\text{ V} \pm 0.15\text{ V}$	2.7		9.9	ns
t_{pd}	A	Y	$C_L = 15\text{ pF}$	$2.5\text{ V} \pm 0.2\text{ V}$	1.6		5.5	ns
t_{pd}	A	Y	$C_L = 15\text{ pF}$	$3.3\text{ V} \pm 0.3\text{ V}$	1.5		4.6	ns
t_{pd}	A	Y	$C_L = 15\text{ pF}$	$5.0\text{ V} \pm 0.5\text{ V}$	0.9		4.4	ns
t_{pd}	A	Y	$C_L = 30\text{ pF}$	$1.8\text{ V} \pm 0.15\text{ V}$	3.0		13	ns
t_{pd}	A	Y	$C_L = 30\text{ pF}$	$2.5\text{ V} \pm 0.2\text{ V}$	2		8	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$	$3.3\text{ V} \pm 0.3\text{ V}$	1.8		6.5	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$	$5.0\text{ V} \pm 0.5\text{ V}$	1.2		6	ns
C_{pd}			No Load, $f = 10\text{ MHz}$	1.8 V		3		pF
C_{pd}			No Load, $f = 10\text{ MHz}$	2.5 V		3		pF
C_{pd}			No Load, $f = 10\text{ MHz}$	3.3 V		3		pF
C_{pd}			No Load, $f = 10\text{ MHz}$	5.0 V		4		pF

5.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

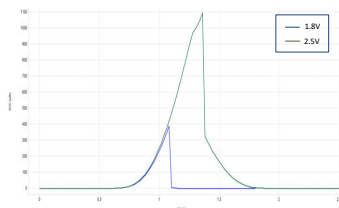


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

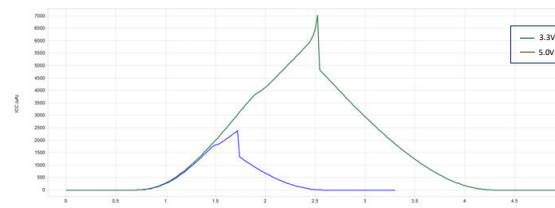


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

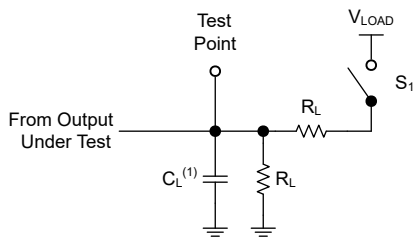
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_f \leq 2.5\text{ns}$.

The outputs are measured individually with one input transition per measurement.

TEST	S1	R_L	C_L	ΔV	V_{LOAD}
t_{PLZ} , t_{PZL}	CLOSED	500Ω	50pF	0.3V	$2 \times V_{CC}$

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
$1.8\text{V} \pm 0.15\text{V}$	$V_{CC}/2$	$1\text{k}\Omega$	$15\text{pF}/30\text{pF}$	0.15V	$2 \times V_{CC}$
$2.5\text{V} \pm 0.2\text{V}$	$V_{CC}/2$	500Ω	$15\text{pF}/30\text{pF}$	0.15V	$2 \times V_{CC}$
$3.3\text{V} \pm 0.3\text{V}$	1.5V	500Ω	$15\text{pF}/50\text{pF}$	0.3V	6V
$5.0\text{V} \pm 0.5\text{V}$	1.5V	500Ω	$15\text{pF}/50\text{pF}$	0.3V	6V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Open-Drain Outputs

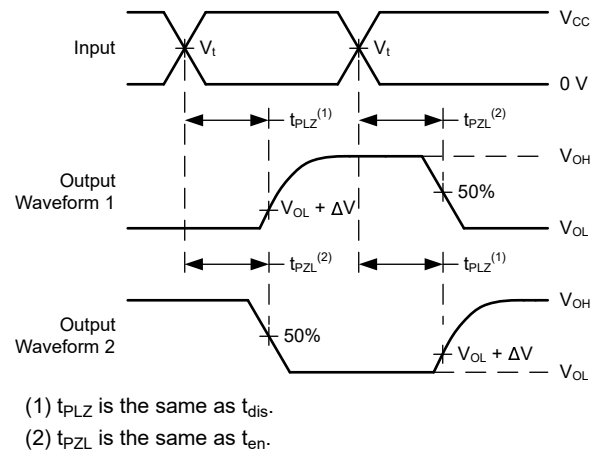
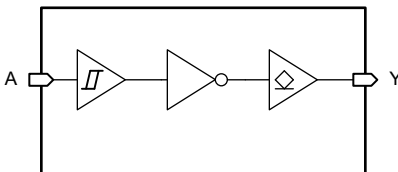


Figure 6-2. Voltage Waveforms Propagation Delays

7 Overview

The SN74LVC1G16 device contains one open-drain inverter with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

8 Functional Block Diagram



9 Detailed Description

9.1 Feature Description

9.1.1 Open-Drain CMOS Outputs

This device includes open-drain CMOS outputs. Open-drain outputs can only drive the output low. When in the high logical state, open-drain outputs will be in a high-impedance state. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused open-drain CMOS outputs should be left disconnected.

9.1.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

9.1.3 Clamp Diode Structure

Figure 9-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

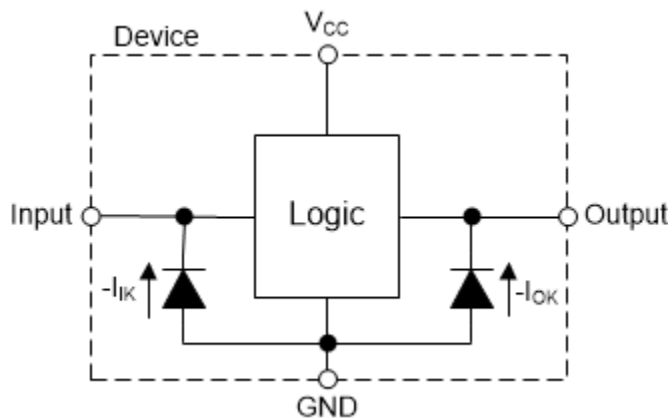


Figure 9-1. Electrical Placement of Clamping Diodes for Each Input and Output

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

In this application, an open-drain inverter is used to drive an LED as shown in [Figure 10-1](#).

10.2 Typical Application

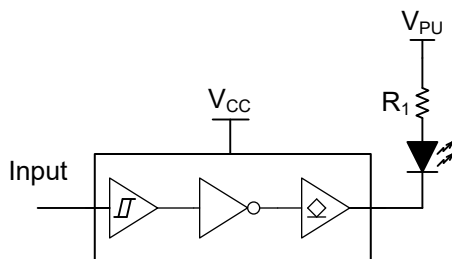


Figure 10-1. Typical Application Block Diagram

10.2.1 Design Requirements

10.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G16 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G16 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC1G16 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

10.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G16 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC1G16 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

10.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

10.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq 50\text{pF}$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC1G16 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in $M\Omega$; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

10.3 Application Curves

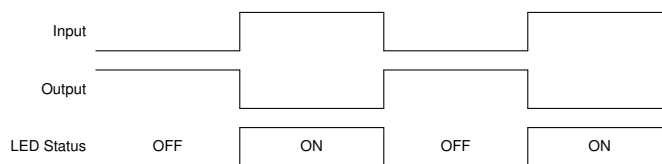


Figure 10-2. Application Curve

10.4 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10.5 Layout

10.5.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

10.5.2 Layout Example

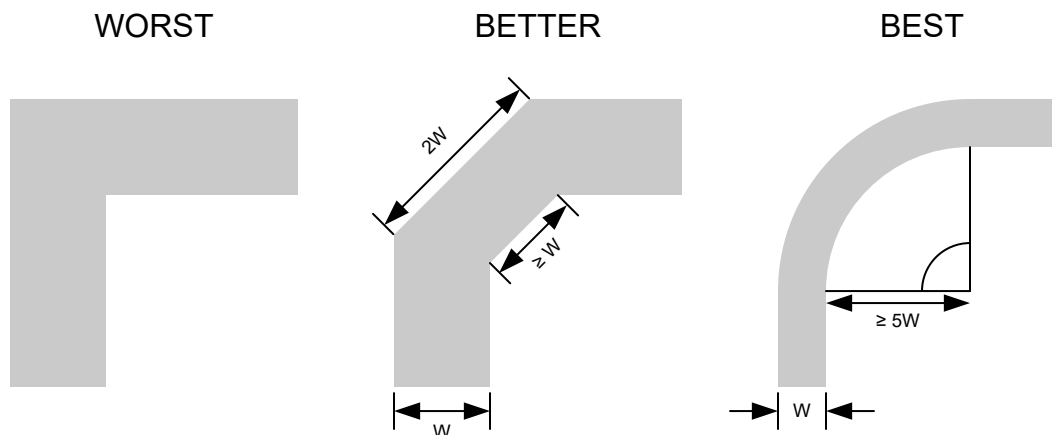


Figure 10-3. Example Trace Corners for Improved Signal Integrity

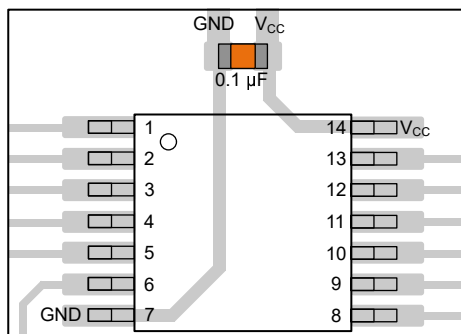


Figure 10-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

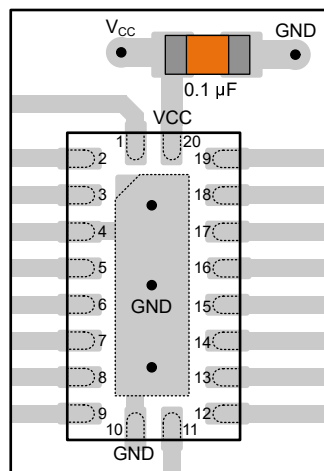


Figure 10-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

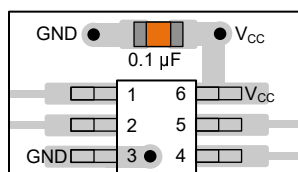


Figure 10-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

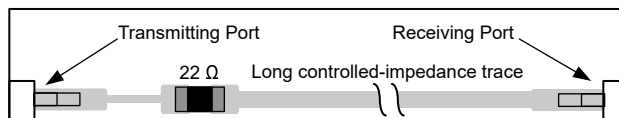


Figure 10-7. Example Damping Resistor Placement for Improved Signal Integrity

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application report](#)
- Texas Instruments, [Designing With Logic application report](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application report](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

Changes from Revision A (April 2025) to Revision B (May 2025)	Page
• Updated Thermal Information.....	4

Changes from Revision * (October 2024) to Revision A (April 2025)	Page
• Changed the status from: <i>Advanced Information</i> to: <i>Production Data</i>	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN74LVC1G16DBVR	Active	Preproduction	SOT-23 (DBV) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PSN74LVC1G16DBVR.A	Active	Preproduction	SOT-23 (DBV) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PSN74LVC1G16DCKR	Active	Preproduction	SC70 (DCK) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PSN74LVC1G16DCKR.A	Active	Preproduction	SC70 (DCK) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
SN74LVC1G16DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(3L2U, 3OGH)
SN74LVC1G16DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1TX

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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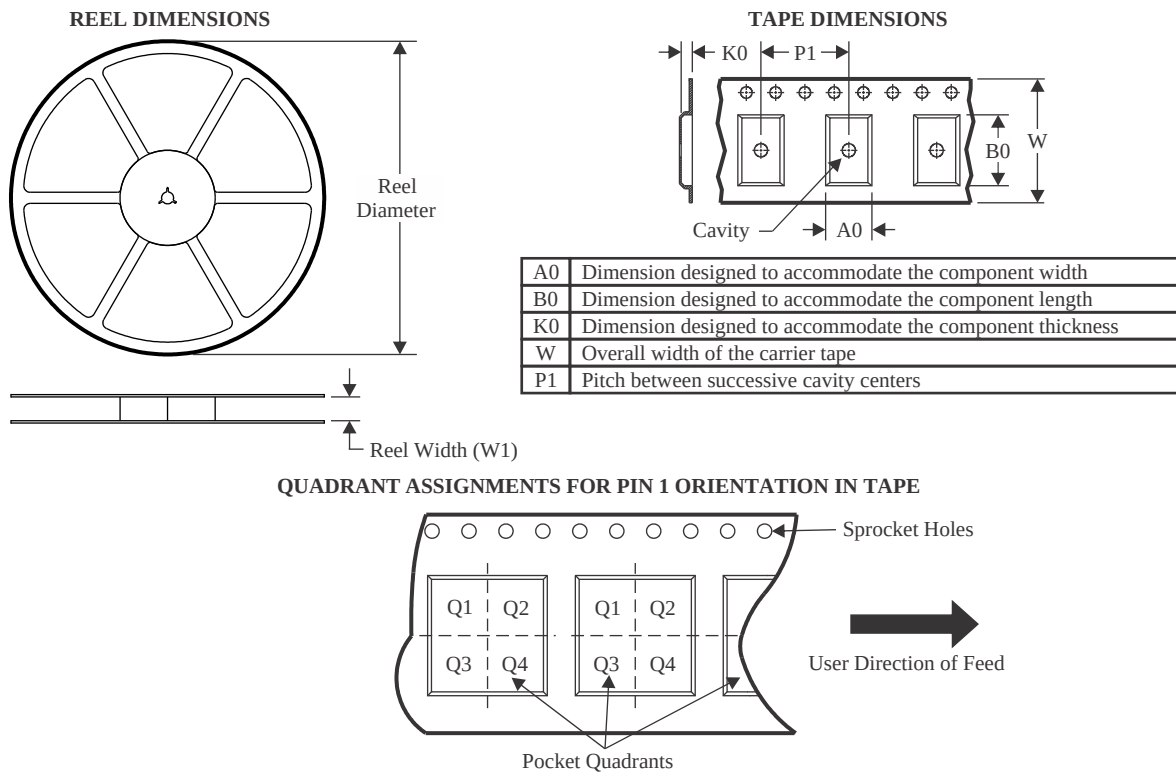
OTHER QUALIFIED VERSIONS OF SN74LVC1G16 :

- Automotive : [SN74LVC1G16-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

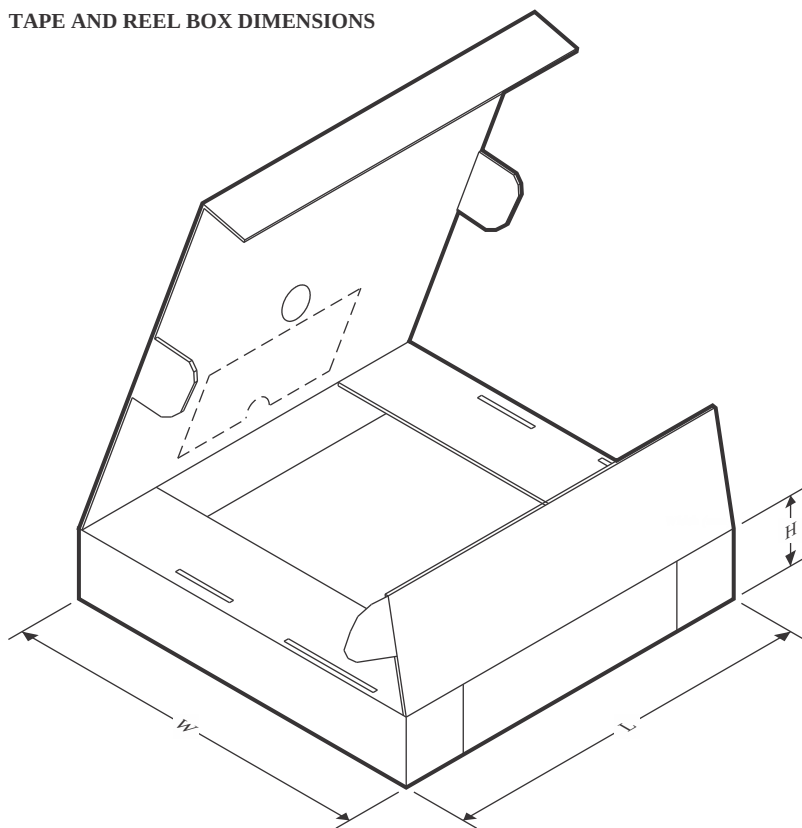
TAPE AND REEL INFORMATION



*All dimensions are nominal

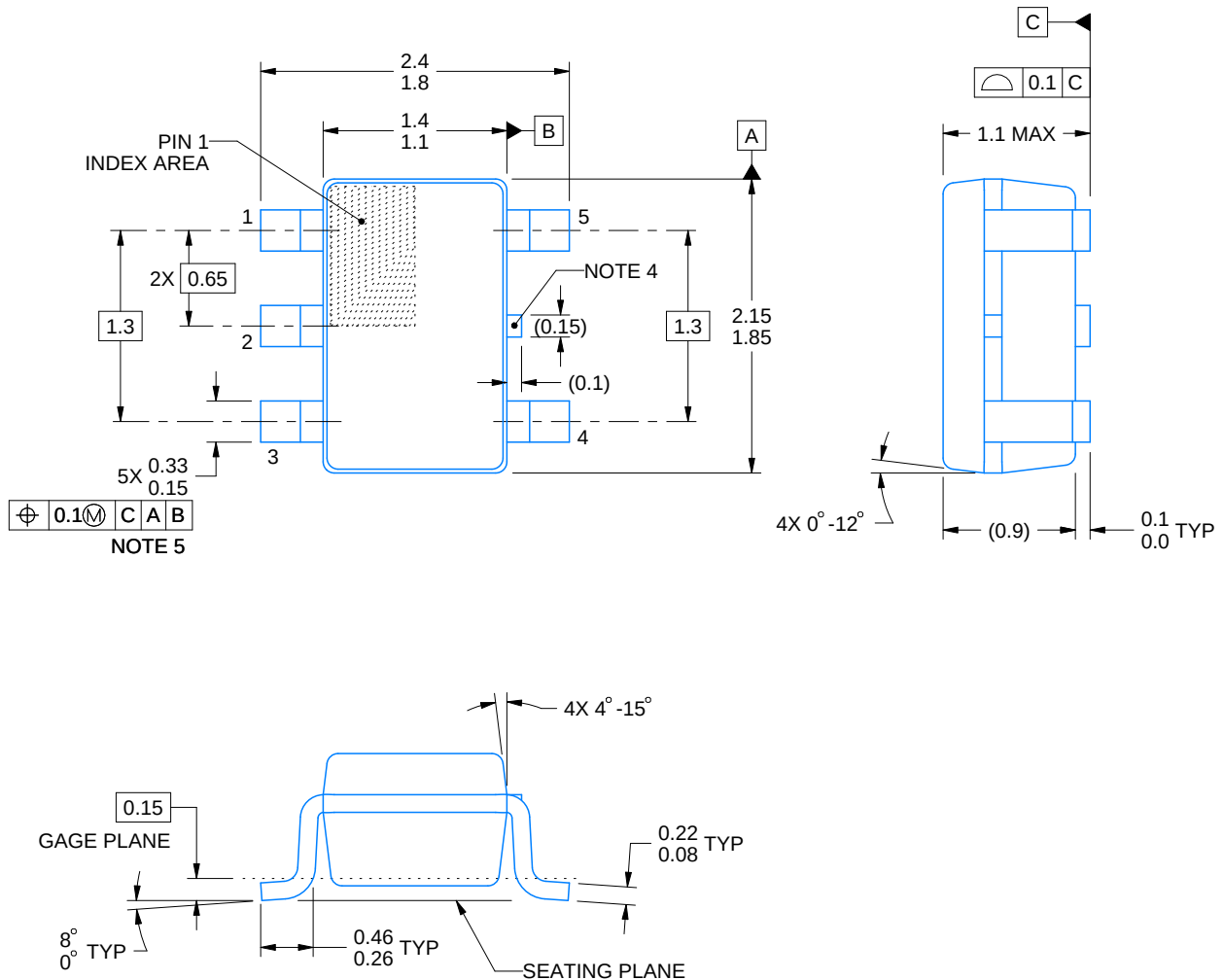
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G16DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G16DCKR	SC70	DCK	5	3000	210.0	185.0	35.0



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NOTES:

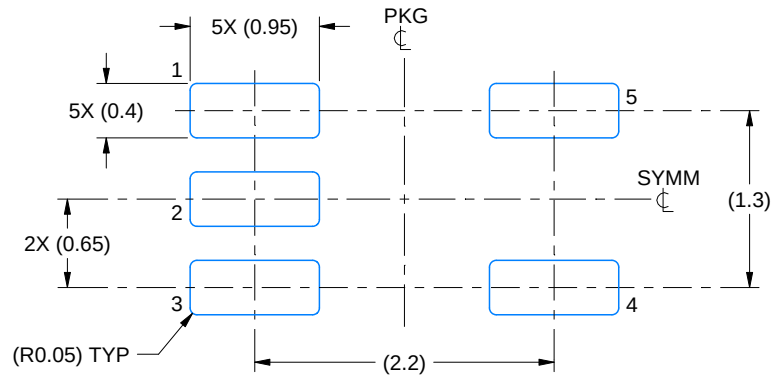
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

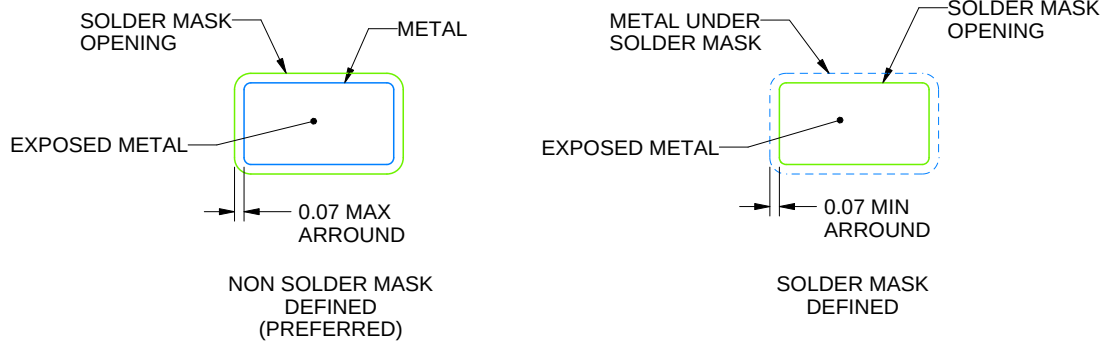
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

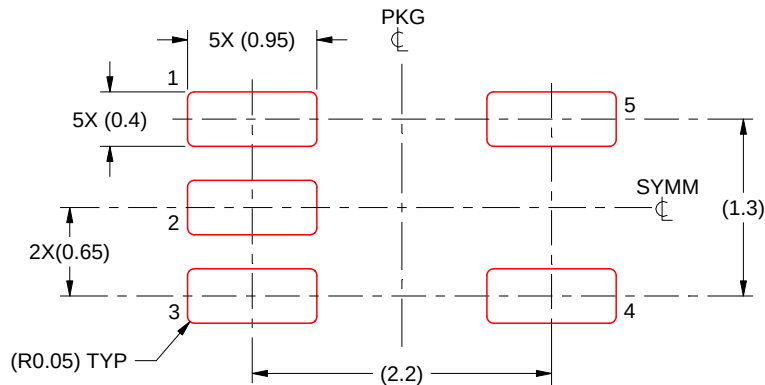
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

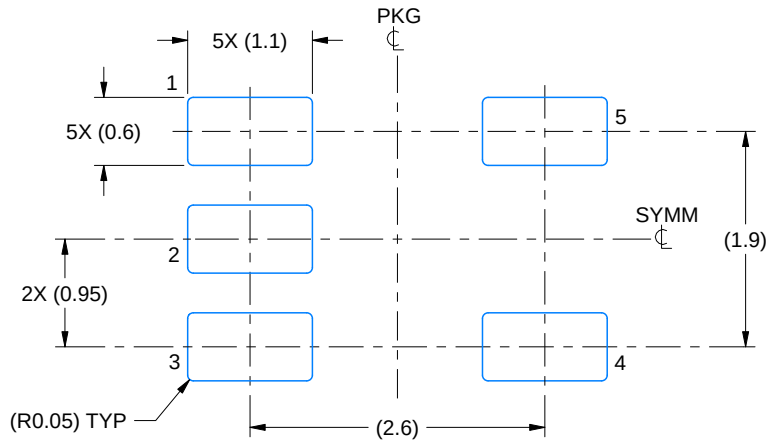
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

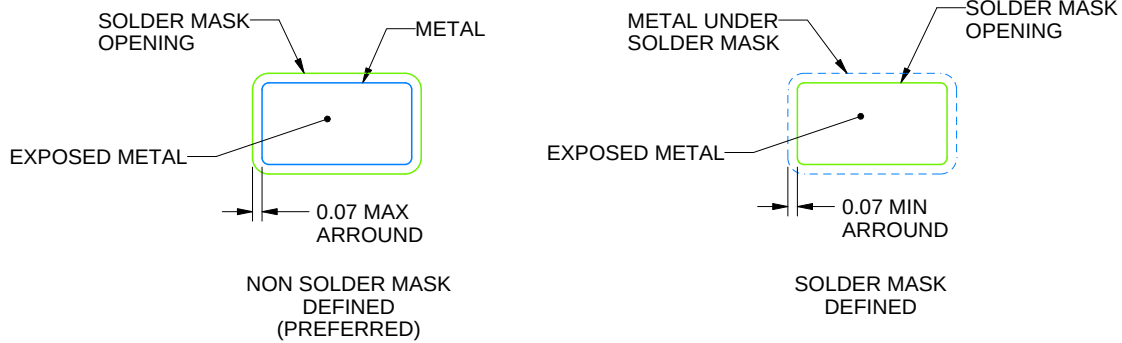
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

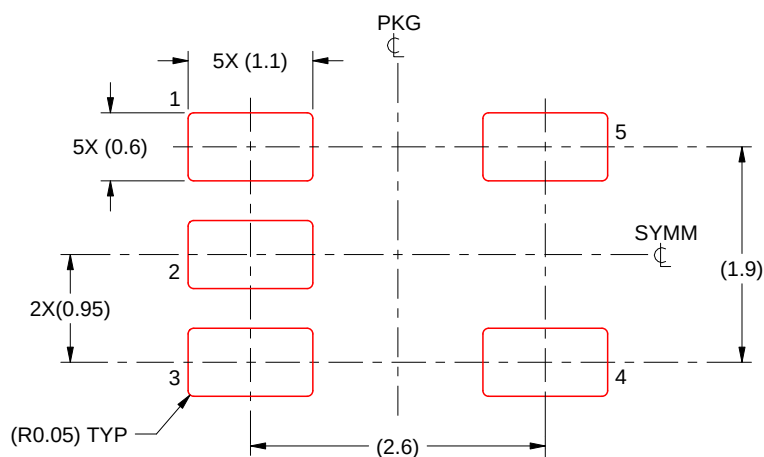
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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