











SN74LVC1G125

SCES223T - APRIL 1999-REVISED OCTOBER 2014

SN74LVC1G125 Single Bus Buffer Gate With 3-State Output

Features

- Available in the Ultra Small 0.64-mm² Package (DPW) With 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Cable Modem Termination System
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Motor Control: High-Voltage
- Power Line Communication Modem
- SSD: Internal or External
- Video Broadcasting and Infrastructure: Scalable Platform
- Video Broadcasting: IP-Based Multi-Format Transcoder
- Video Communications System

3 Description

This bus buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G125 device is a single line driver with a 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G125 device is available in a variety of packages including the ultra-small DPW package with a body size of $0.8 \text{ mm} \times 0.8 \text{ mm}$.

Device Information⁽¹⁾

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
	SOT-23 (5)	2.90 mm x 1.60 mm
	SC70 (5)	2.00 mm x 1.25 mm
SN74LVC1G125	SON (6)	1.45 mm × 1.00 mm
	DSBGA (5)	1.40 mm × 0.90 mm
	X2SON (4)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

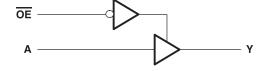


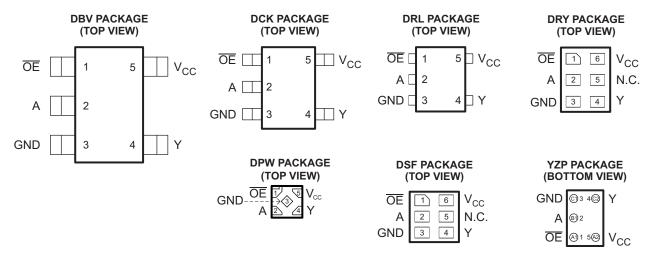


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6 Pin Configuration and Functions



N.C. – No internal connection
See mechanical drawings for dimensions.

Pin Functions

					iii i dilottorio					
		PIN								
NAME	DRL, DCK, DBV	DRY, DSF	DPW	YZP	DESCRIPTION					
ŌĒ	1	1	1	A1	Input					
Α	2	2	2	B1	Input					
GND	3	3	3	C1	Ground					
Υ	4	4	4	C2	Output					
V _{CC}	5	6	5	A2	Power pin					
NC	-	5	-	_	Not connected					

Product Folder Links: SN74LVC1G125



7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾	-0.5	6.5	V	
Vo	Voltage range applied to any output in the h	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		6.5	V
Vo	Voltage range applied to any output in the h	nigh or low state (2)(3)	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature rang	ne e	-65	150	°C
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	0	1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the *Recommended Operating* table.



7.3 Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
,	Owner by see the see	Operating	1.65	5.5	
/ _{cc}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
,	LPak Israel Construction	V _{CC} = 2.3 V to 2.7 V	1.7		
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
.,	Law law Law Law at walkana	V _{CC} = 2.3 V to 2.7 V		0.7	.,
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
VI	Input voltage	•	0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
ОН	High-level output current			-16	mA
		$V_{CC} = 3 V$		-24	
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
OL	Low-level output current	V 2.V		16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		32	
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
∆t/Δv	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	
T _A	Operating free-air temperature		-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

7.4 Thermal Information

	nonna miorination									
			SN74LVC1G125							
	THERMAL METRIC (1)	DBV	DCK	DRL	DRY	YZP	DPW	UNIT		
		5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229	278	243	439	130	340			
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164	93	78	277	54	215			
$R_{\theta JB}$	Junction-to-board thermal resistance	62	65	78	271	51	294	°C/W		
ΨЈТ	Junction-to-top characterization parameter	44	2	10	84	1	41	*C/VV		
Ψ_{JB}	Junction-to-board characterization parameter	62	64	77	271	50	294			
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	_	_	_	-	_	250			

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Product Folder Links: SN74LVC1G125



7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLETIONS	.,	–40 C to 85 °C	;	−40 C t	o 125 °C	LINUT	
PARAMETER	TEST CONDITIONS	V _{CC}	MIN TYP(1)	MAX	MIN	TYP ⁽¹⁾ MAX	UNIT	
	$I_{OH} = -100 \ \mu A$	1.65 V to 5.5 V	V _{CC} – 0.1		V _{CC} – 0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		1.2			
V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		1.9		V	
V _{OH}	$I_{OH} = -16 \text{ mA}$	3 V	2.4		2.4		V	
	$I_{OH} = -24 \text{ mA}$	3 V	2.3		2.3			
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		3.8			
	I _{OL} = 100 μA	1.65 V to 5.5 V		0.1		0.1		
	I _{OL} = 4 mA	1.65 V		0.45		0.45		
V	I _{OL} = 8 mA	2.3 V		0.3		0.3	V	
V _{OL}	I _{OL} = 16 mA	2.1/		0.4		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		0.55		
	I _{OL} = 32 mA	4.5 V		0.55		0.55		
I _I A or OE inputs	V _I = 5.5 V or GND	0 to 5.5 V		±5		±5	μA	
I _{off}	V_I or $V_O = 5.5 \text{ V}$	0		±10		±10	μΑ	
l _{OZ}	V _O = 0 to 5.5 V	3.6 V		10		10	μΑ	
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		10		10	μA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500		500	μΑ	
C _I	$V_I = V_{CC}$ or GND	3.3 V	4		4		pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

7.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range of -40° C to 85°C, $C_L = 15$ pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.9	6.9	0.7	4.6	0.6	3.7	0.5	3.4	ns

7.7 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range -40° C to 85°C, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = 0.2		V _{CC} = 0.3	3.3 V 3 V	V _{CC} = ± 0.5	5 V 5 V	UNIT
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	2.8	9	1.2	5.5	1	4.5	1	4	ns
t _{en}	ŌĒ	Υ	3.3	10.1	1.5	6.6	1	5.3	1	5	ns
t _{dis}	ŌĒ	Υ	1.3	9.2	1	5	1	5	1	4.2	ns

Product Folder Links: SN74LVC1G125



7.8 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range -40° C to 125°C, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see Figure 4)

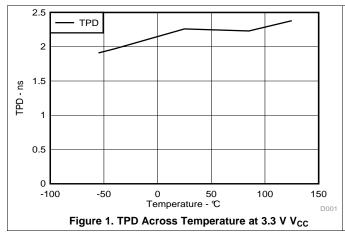
	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = 2 ± 0.2		V _{CC} = 0.3		V _{CC} =		UNIT
		(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	t_{pd}	Α	Υ	2.8	9.3	1.2	5.8	1	4.7	1	4.2	ns
	t _{en}	ŌĒ	Υ	3.3	10.4	1.5	6.9	1	5.6	1	5.2	ns
	t _{dis}	ŌĒ	Υ	1.3	9.3	1	5.2	1	5.2	1	4.4	ns

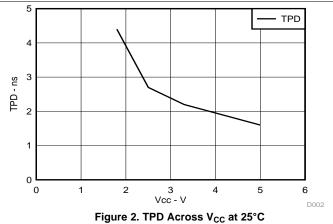
7.9 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	V _{CC} = 5 V TYP	UNIT	
Power dissipation	Outputs enabled	f 40 MH-	18	18	19	21			
C _{pd}	capacitance	Outputs disabled	f = 10 MHz	2	2	2	4	pF	

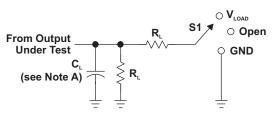
7.10 Typical Characteristics







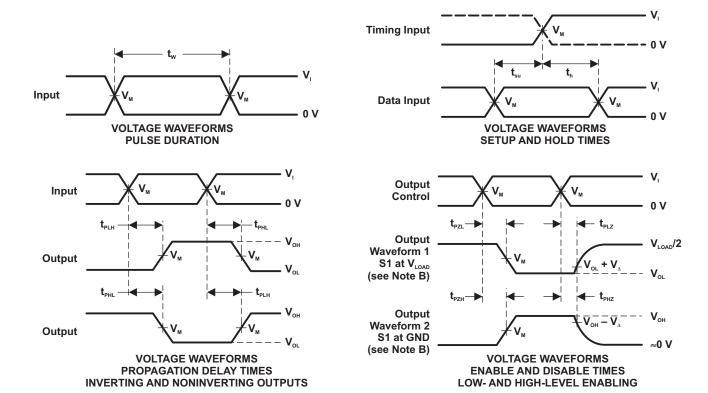
8 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

L	OA	D	CI	R	CI	UΙ	т

,,	INI	PUTS		v		-	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _⊾	V _A
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
$2.5~\textrm{V}~\pm~0.2~\textrm{V}$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
$3.3~V~\pm~0.3~V$	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{\circ} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\mbox{\tiny PLZ}}$ and $t_{\mbox{\tiny PHZ}}$ are the same as $t_{\mbox{\tiny dis}}.$
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

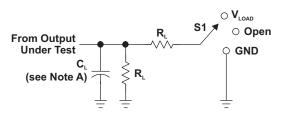
Figure 3. Load Circuit and Voltage Waveforms

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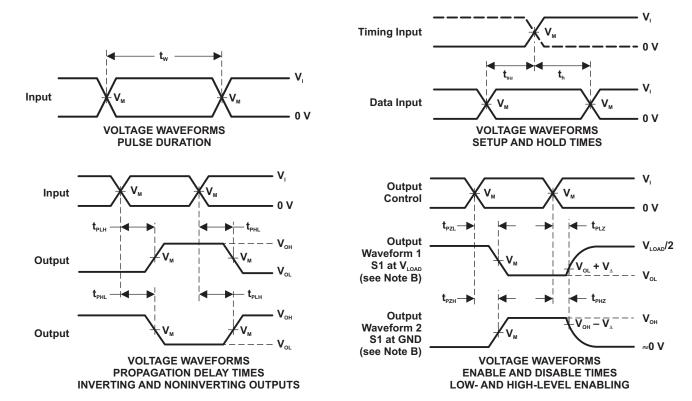
Parameter Measurement Information (continued)



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INI	PUTS		.,		-	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _∟	R _⊾	V _A
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
$2.5~V~\pm~0.2~V$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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9 Detailed Description

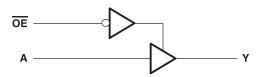
9.1 Overview

The SN74LVC1G125 device contains one buffer gate device with output enable control and performs the Boolean function Y = A. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

9.2 Functional Block Diagram



9.3 Feature Description

- · Wide operating voltage range
 - Operates from 1.65 V to 5.5 V
- Allows down voltage translation
- Inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V

9.4 Device Functional Modes

Table 1. Function Table

INP	UTS	OUTPUT				
ŌĒ	Α	Υ				
L	Н	Н				
L	L	L				
Н	X	Z				

Product Folder Links: SN74LVC1G125

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10 Application and Implementation

10.1 Application Information

The SN74LVC1G125 device is a high drive CMOS device that can be used as a output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC}.

10.2 Typical Application

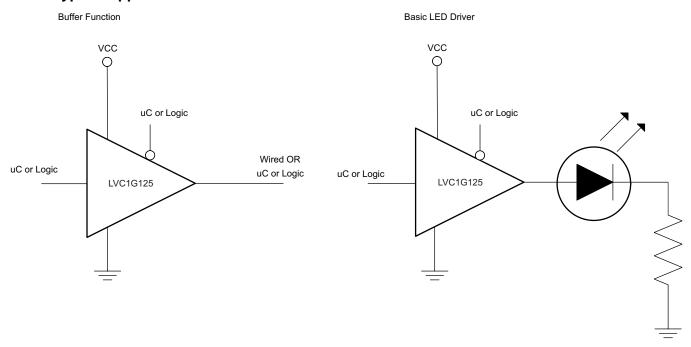


Figure 5. Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V₁ max) in the Recommended Operating Conditions table at any valid V_{CC}.

2. Recommend Output Conditions

- Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
- Outputs should not be pulled above V_{CC}.

Product Folder Links: SN74LVC1G125



Typical Application (continued)

10.2.3 Application Curves

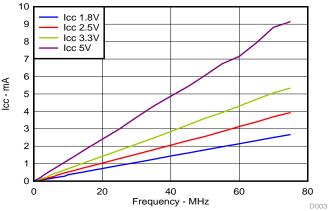


Figure 6. I_{CC} vs Frequency

11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-µF capacitor is recommended and if there are multiple VCC pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 7 shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

12.2 Layout Example



Figure 7. Package Layout

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13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC1G125

www.ti.com

7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74LVC1G125DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DBVRE4.B	Active	Production	SOT-23 (DBV) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DBVTE4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DBVTE4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DBVTG4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
74LVC1G125DCKRE4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM5
74LVC1G125DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM5
74LVC1G125DCKRG4.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM5
74LVC1G125DCKTE4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM5
74LVC1G125DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM5
74LVC1G125DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM5
SN74LVC1G125DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25J, C25K, C25R, C 25T)
SN74LVC1G125DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25J, C25K, C25R, C 25T)
SN74LVC1G125DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
SN74LVC1G125DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255, C25F, C25K, C25R)
SN74LVC1G125DCK3	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	(CMF, CMZ)





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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G125DCK3.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	(CMF, CMZ)
SN74LVC1G125DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CM5, CMF, CMJ, CM K, CMR, CMT)
SN74LVC1G125DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CM5, CMF, CMJ, CM K, CMR, CMT)
SN74LVC1G125DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CM5, CMF, CMJ, CM K, CMR, CMT)
SN74LVC1G125DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM5, CMF, CMJ, CM K, CMR, CMT)
SN74LVC1G125DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	
SN74LVC1G125DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4
SN74LVC1G125DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4
SN74LVC1G125DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CM7, CMR)
SN74LVC1G125DRLR.B	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CM7, CMR)
SN74LVC1G125DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM, DM)
SN74LVC1G125DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM, DM)
SN74LVC1G125DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM
SN74LVC1G125DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM
SN74LVC1G125DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM
SN74LVC1G125DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM
SN74LVC1G125DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM
SN74LVC1G125YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(CM7, CMN)
SN74LVC1G125YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(CM7, CMN)

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G125:

Automotive: SN74LVC1G125-Q1

Enhanced Product : SN74LVC1G125-EP

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G125DBVTE4	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
74LVC1G125DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
74LVC1G125DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
74LVC1G125DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G125DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G125DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G125DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G125DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G125DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G125DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G125DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G125DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G125YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G125DBVTE4	SOT-23	DBV	5	250	180.0	180.0	18.0
74LVC1G125DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
74LVC1G125DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
74LVC1G125DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G125DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G125DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G125DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G125DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G125DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G125DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G125DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G125DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G125DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G125DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G125YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



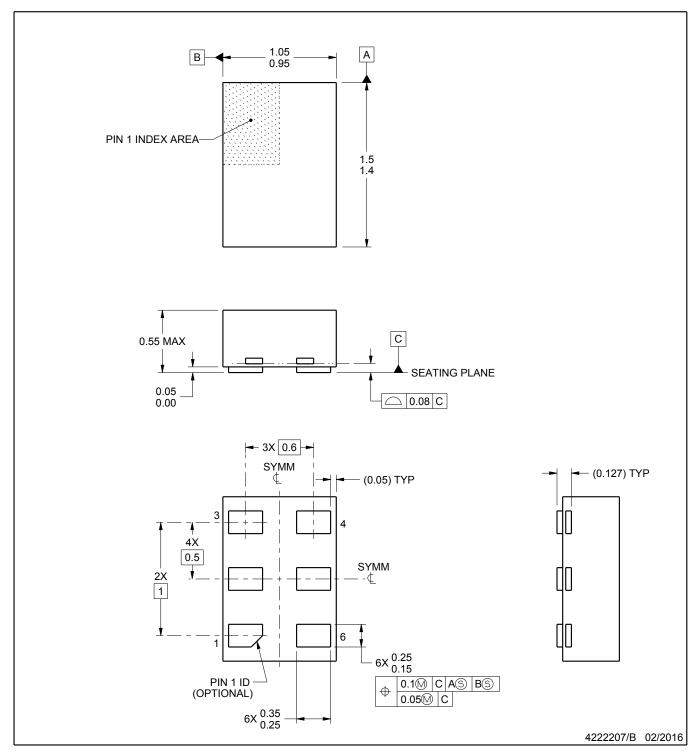


NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





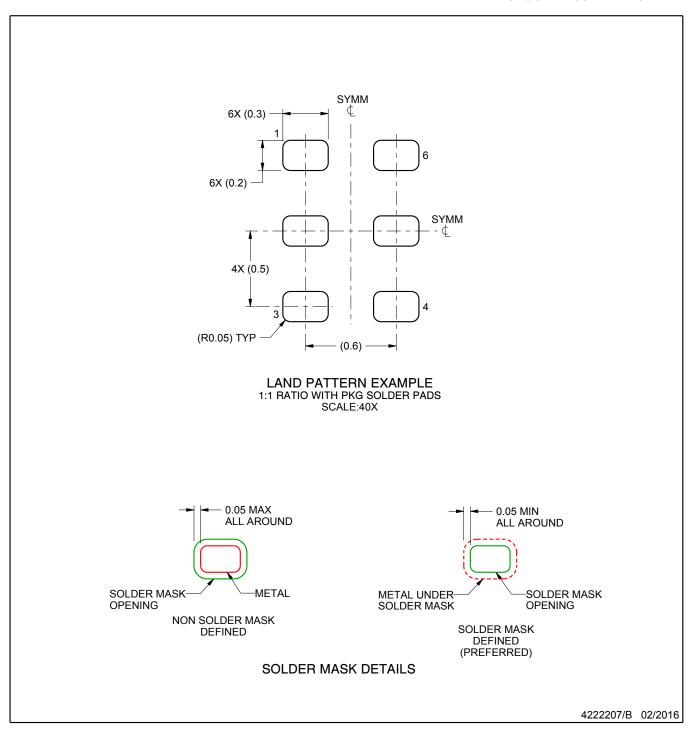


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

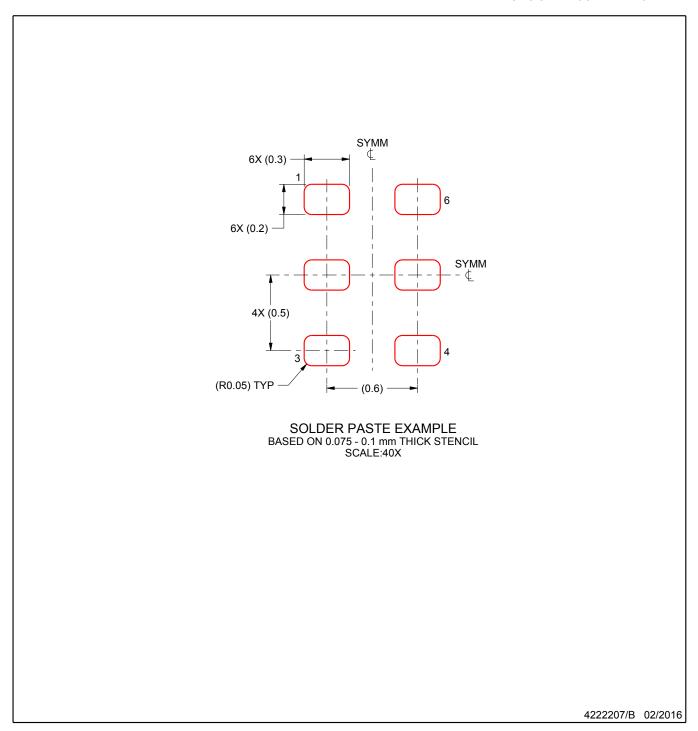




NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-293 Variation UAAD-1



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4211218-3/D







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. The size and shape of this feature may vary.





NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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