

SN74LVC1G07 Single Buffer/Driver With Open-Drain Output

1 Features

- Available in the ultra small 0.64mm² package (DPW) with 0.5mm pitch
- Supports 5V V_{CC} operation
- Input and open-drain output accept voltages up to
- Can translate up or down
- Maximum t_{pd} of 4.2ns at 3.3V
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22
 - 2000V Human-body model (A114-A)
 - 200V Machine model (A115-A)
 - 1000V Charged-device model (C101)

2 Applications

- AV receiver
- Blu-ray player and home theater
- DVD recorder and player
- Desktop or notebook PC
- Digital radio or internet radio player
- Digital Video Camera (DVC)
- Embedded PC
- GPS: personal navigation device
- Mobile internet device
- Network projector front end
- Portable media player
- Pro audio mixer
- Smoke detector
- Solid State Drive (SSD): enterprise
- High-definition (HDTV)
- Tablet: enterprise
- Audio dock: portable
- DLP front projection system
- **DVR and DVS**
- Digital Picture Frame (DPF)
- Digital still camera

3 Description

This single buffer/driver is designed for 1.65V to 5.5V V_{CC} operation.

The output of the SN74LVC1G07 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32mA.

The SN74LVC1G07 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8mm × 0.8mm.

Package Information

DEVICE NAME	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾		
	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm		
	DCK (SC70, 5)	2.0mm × 2.1mm	2.0mm × 1.25mm		
	DPW (X2SON, 5)	0.8mm × 0.8mm	0.8mm × 0.8mm		
	DRY (USON, 6)	1.45mm × 1.0mm	1.45mm × 1.0mm		
SN74LVC1G07	DSF (X2SON, 6)	1.0mm × 1.0mm	1.0mm × 1.0mm		
SN/4EVC1GU/	DRL (SOT-5X3, 5)	1.6mm × 1.6mm	1.6mm × 1.2mm		
	YZP (DSBGA, 6)	1.75mm × 1.25mm	1.38mm × 0.88mm		
	YZV (DSBGA, 4)	1.25mm × 1.25mm	0.88mm × 0.88mm		

- For all available packages, see the orderable addendum at the end of the datasheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.

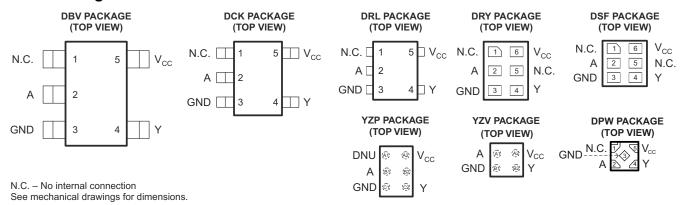




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4 Pin Configuration and Functions



Pin Functions

		PI	N					
NAME	DBV, DCK, DRL	DRY, DSF	DPW	YZP	YZV DESCRIPTION			
NC	1	1, 5	1	A1, B2	-	Not connected		
Α	2	2	2	B1	A1	Input		
GND	3	3	3	C1	B1	Ground		
Y	4	4	4	C2	B2	Output		
V _{CC}	5	6	5	A2	A2	Power pin		



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	CC Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power	r-off state ⁽²⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state ^{(2) (3)}		-0.5	6.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage temperature range		-65	150	°C
Tj	Junction temperature range			150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			MIN	MAX	UNIT
V	Electrostatio discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

The value of V_{CC} is provided in the Recommended Operating Conditions table.



5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
\/	Cupply valtage	Operating	1.65	5.5	V
V_{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
.,	High lavel in motoralia and	V _{CC} = 2.3 V to 2.7 V	1.7		V
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
.,	Lave lavel in motor reliance	V _{CC} = 2.3 V to 2.7 V		0.7	.,
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
VI	Input voltage	,	0	5.5	V
Vo	Output voltage		0	5.5	V
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current			16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		32	
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
Δt/Δν	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		10	ns/V
		V _{CC} = 5 V ± 0.5 V		5	
_	On another force air town and we	DSBGA package	-40	85	°C
T_A	Operating free-air temperature	All other packages	-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

				SN74LVC1G07							
	THERMAL METRIC ⁽¹⁾	DBV	DCK	DRL	DRY	YZP	DPW	UNIT			
		5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	357.1	278	243	439	130	340				
R _{0JC(top)}	Junction-to-case (top) thermal resistance	263.7	93	78	277	54	215				
$R_{\theta JB}$	Junction-to-board thermal resistance	264.4	65	78	271	51	294	°C/W			
ΨЈТ	Junction-to-top characterization parameter	195.6	2	10	84	1	41	- C/VV			
ΨЈВ	Junction-to-board characterization parameter	262.2	64	77	271	50	294				
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	-	_	-	-	_	250				

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	V _{cc}	-40°C TO 85°C	-40°C TO 125°C RECOMMENDED	UNIT	
				TYP ⁽¹⁾ MAX	TYP MAX		
		I _{OL} = 100 μA	1.65 V to 5.5 V	0.1			
I _{OL} = 4 mA		1.65 V	0.45	0.45			
I _{OL} = 8 mA		2.3 V	0.3	0.3	v		
V_{OL} $I_{OL} = 16 \text{ m/s}$		I _{OL} = 16 mA	3 V	0.4	0.4	٧	
		I _{OL} = 24 mA		0.55	0.55		
		I _{OL} = 32 mA	4.5 V	0.55			
I _I	A input	V _I = 5.5 V or GND	0 to 5.5 V	±5	±5	μA	
I _{off}		V_I or $V_O = 5.5 \text{ V}$	0	±10	±10	μA	
I _{CC}		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V	10	10	μA	
ΔI_{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500	500	μA	
C _i		V _I = V _{CC} or GND	3.3 V	4	4	pF	
Co		V _O = V _{CC} or GND	3.3 V	5	5	pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

5.6 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

				−40°C TO 85°C								
	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1 ± 0.1		V _{CC} = ± 0.2		V _{CC} = 3 ± 0.3		V _{CC} = ± 0.5		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
ſ	t _{pd}	A	Y	2.4	8.3	1	5.5	1.5	4.2	1	3.5	ns

5.7 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

DADAMETED	FROM	то		4 0 1/	R	ECOM	O 125°C MENDED	224	V -	5 V	LIMIT
PARAMETER	(INPUT)	(OUTPUT)		V _{CC} = 1.8 V ± 0.15 V		2.5 V 2 V	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.4	8.6	1	6	1.5	4.7	1	4	ns

5.8 Operating Characteristics

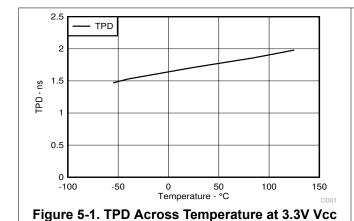
 $T_A = 25^{\circ}C$

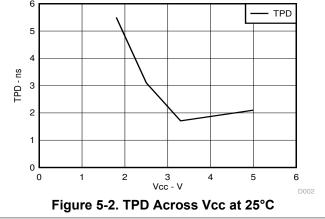
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT	
PARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
C _{pd} Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF	

Product Folder Links: SN74LVC1G07



5.9 Typical Characteristics

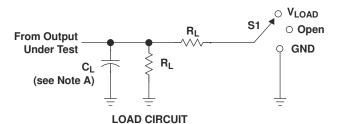






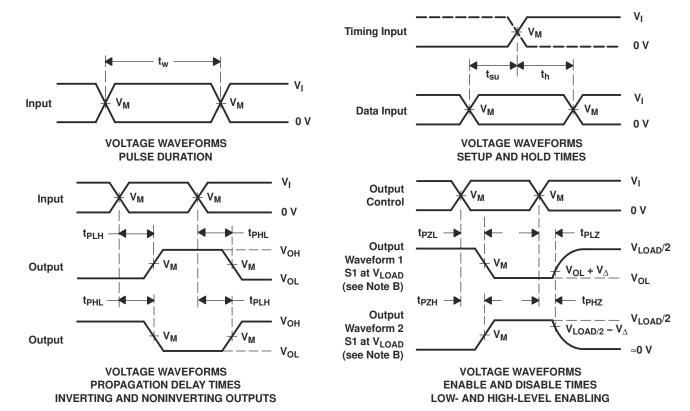
6 Parameter Measurement Information

6.1 (Open Drain)



TEST	S1
t _{PZL} (see Notes E and F)	V_{LOAD}
t _{PLZ} (see Notes E and G)	V_{LOAD}
t _{PHZ} /t _{PZH}	V_{LOAD}

	INPUT						
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	RL	V_Δ
1.8 V ± 0.15 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	Vcc	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{CC}	≤ 2.5 ns	V _{CC} /2	2 × V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{od}.
- F. t_{PZL} is measured at V_M.
- G. t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74LVC1G07 device contains one open-drain buffer with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. The DPW 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

7.2 Functional Block Diagram



7.3 Feature Description

- · Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- · Allows down voltage translation.
- Inputs and outputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

7.4 Device Functional Modes

Function Table

INPUT A	OUTPUT Y
L	L
Н	Z

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8 Application and Implementation

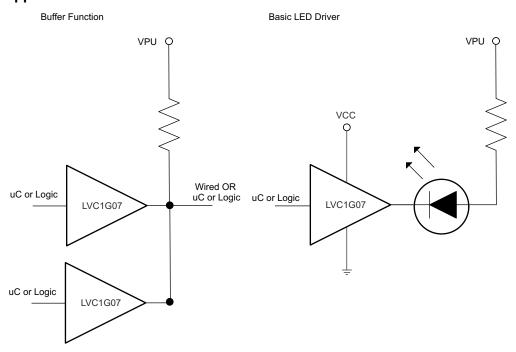
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G07 is a high drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can sink 32 mA of current at 4.5 V making it ideal for high drive and wired-OR/AND functions. It is good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate up/down to $V_{\rm CC}$.

8.2 Typical Application



8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it may drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

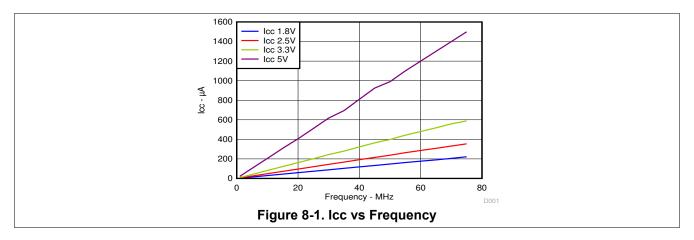
- 1. Recommended Input Conditions
 - Rise time and fall time specs. See (Δt/ΔV) in the Recommended Operating Conditions table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
 - Inputs are over-voltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating
 Conditions table at any valid V_{CC}.
- 2. Recommend Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

Product Folder Links: SN74LVC1G07

Outputs should not be pulled above 5.5 V.

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8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each Vcc pin should have a good bypass capacitor to prevent power disturbance. A $0.1-\mu F$ capacitor is recommended for devices with a single supply. If there are multiple Vcc pins then a $0.01-\mu F$ or $0.022-\mu F$ capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. $0.1-\mu F$ and $1-\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to Gnd or Vcc, whichever is more convenient.

8.4.2 Layout Example



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9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	nanges from Revision AE (September 2020) to Revision AF (June 2025)	Page
•	Changed Device Information table to Package Information	1
•	Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W	5
•	Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/	W 5
•	Changed Junction-to-board thermal resistance value for DBV package from: 62°C/W to: 264.4°C/W	5
•	Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W	5
•	Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W	5
_	· · ·	

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC1G07

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G07DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R, C 07T) (C07H, C07P, C07S)
SN74LVC1G07DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R, C 07T) (C07H, C07P, C07S)
SN74LVC1G07DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R, C 07T) (C07H, C07P, C07S)
SN74LVC1G07DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F
SN74LVC1G07DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F
SN74LVC1G07DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F
SN74LVC1G07DBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F
SN74LVC1G07DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R) (C07H, C07P, C07S)
SN74LVC1G07DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R) (C07H, C07P, C07S)
SN74LVC1G07DBVTE4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F
SN74LVC1G07DBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F
SN74LVC1G07DBVTG4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F
SN74LVC1G07DCK3	Last Time Buy	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CVF, CVZ)
SN74LVC1G07DCK3.B	Last Time Buy	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CVF, CVZ)





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Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G07DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVJ, CV K, CVR, CVT) (CVH, CVP, CVS)
SN74LVC1G07DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVJ, CV K, CVR, CVT) (CVH, CVP, CVS)
SN74LVC1G07DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVJ, CV K, CVR, CVT) (CVH, CVP, CVS)
SN74LVC1G07DCKRE4	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R) (CVH, CVP, CVS)
SN74LVC1G07DCKRE4.B	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R) (CVH, CVP, CVS)
SN74LVC1G07DCKRG4	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV5
SN74LVC1G07DCKRG4.B	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV5
SN74LVC1G07DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVJ, CV K, CVR, CVT) CVH
SN74LVC1G07DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVJ, CV K, CVR, CVT) CVH
SN74LVC1G07DCKTE4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R) CVH
SN74LVC1G07DCKTE4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R) CVH
SN74LVC1G07DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R) CVH
SN74LVC1G07DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R) CVH
SN74LVC1G07DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L4





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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G07DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	(4) NIPDAU	(5) Level-1-260C-UNLIM	-40 to 125	L4
SN74LVC1G07DFWR.B	Active	Production	· · · · · · · · · · · · · · · · · · ·	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CV7, CVR)
			SOT-5X3 (DRL) 5						, ,
SN74LVC1G07DRLR.B	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CV7, CVR)
SN74LVC1G07DRLRG4	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CV7, CVR)
SN74LVC1G07DRY2	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DRY2.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DSF2	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DSF2.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
SN74LVC1G07YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CV7, CVN)
SN74LVC1G07YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CV7, CVN)
SN74LVC1G07YZVR	Active	Production	DSBGA (YZV) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CV N
SN74LVC1G07YZVR.B	Active	Production	DSBGA (YZV) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CV N

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G07:

Automotive: SN74LVC1G07-Q1

Enhanced Product: SN74LVC1G07-EP

NOTE: Qualified Version Definitions:

- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKTE4	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G07DCKTE4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKTE4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKTG4	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G07DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G07DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3
SN74LVC1G07DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G07DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G07DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G07DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G07DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G07DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G07DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKTE4	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G07DCKTE4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKTE4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKTG4	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G07DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G07DRY2	SON	DRY	6	5000	202.0	201.0	28.0



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G07DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G07DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G07DSF2	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G07DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G07DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0



SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



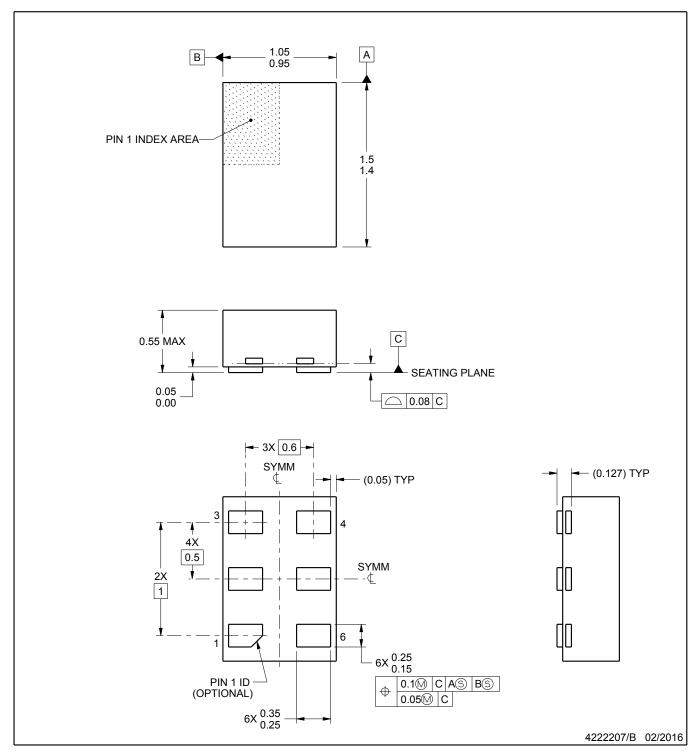


NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





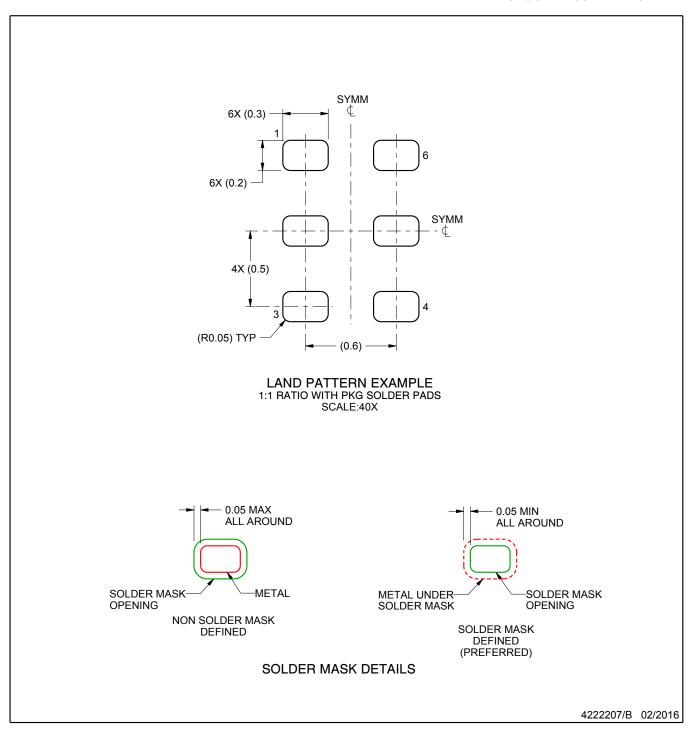


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

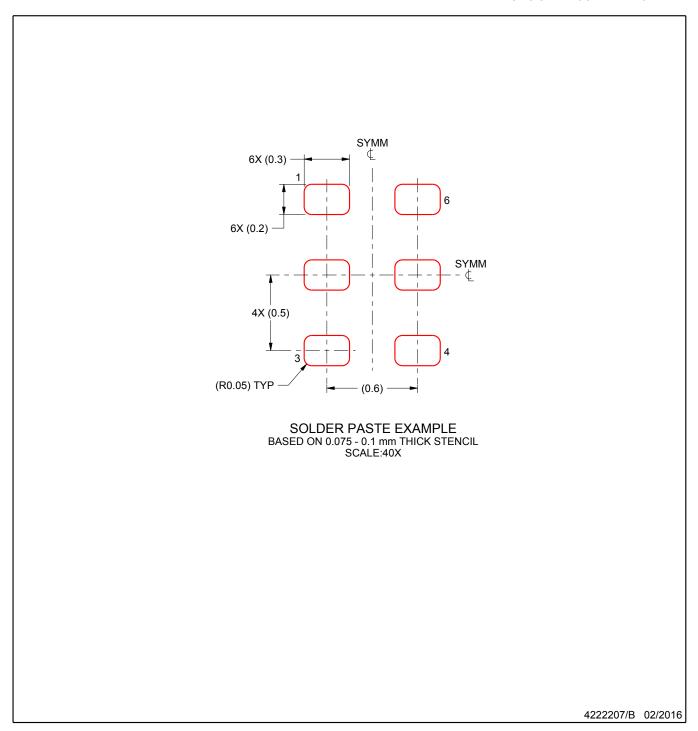




NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-293 Variation UAAD-1



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4211218-3/D





PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. The size and shape of this feature may vary.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



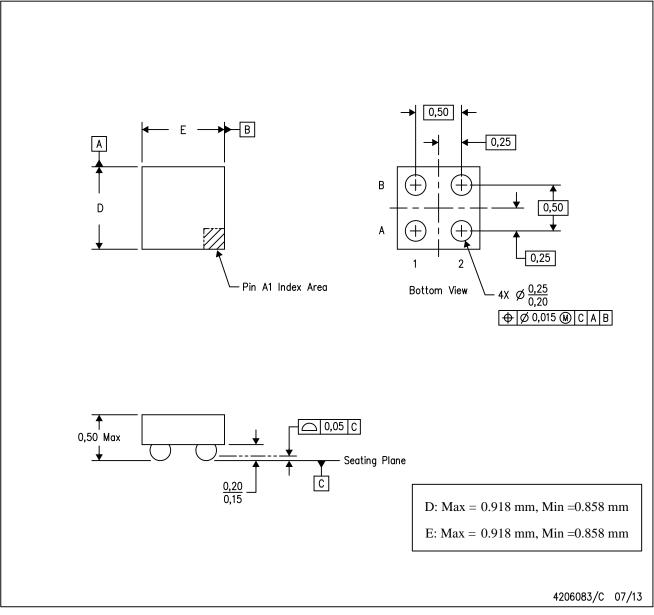
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.





SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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