

SN74LVC1G04-Q1 Single Inverter Gate

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: -40°C to 125°C ambient operating temperature
 - Device HBM ESD classification level H2
 - Device CDM ESG classification level C4B
- ESD protection exceeds 2000V per MIL-STD-883, method 3015; exceeds 200V using machine model (C = 200pF, R = 0)
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 3.3ns at 3.3V
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- Body control modules
- Engine control modules
- Infotainment systems
- **Telematics**

3 Description

This single inverter gate is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G04-Q1 performs Boolean function $Y = \overline{A}$.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when the device is powered down.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74LVC1G04-	DBV (SOT-23, 5)	2.90mm × 2.80mm	2.90mm × 1.60mm
Q1	DCK (SC-70, 5)	2.00mm × 2.10mm	2.00mm × 1.25mm
SN74LVC1G04I- Q1 DCK (SC-70, 5)		2.00mm × 2.10mm	2.00mm × 1.25mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

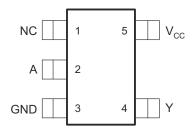
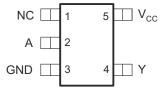


Figure 4-1. DBV 5-pin SOT-23 Top View



NC - no internal connection

For package dimensions see the mechanical drawings at the end of the data sheet.

Figure 4-2. DCK 5-pin SC-70 Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION				
NAME	NO.	1/0	DESCRIPTION				
Α	2	I	Logic input				
GND	3	_	Ground				
NC	1	_	No internal connection				
V _{CC}	5	I	Supply voltage				
Υ	4	0	Inverted logic output				



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the	high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the	high or low state ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	·		±50	mA
	Continuous current through V _{CC} or GND			±100	mA
Δ	Package thermal impedance ⁽⁴⁾	DBV package		206	°C/W
θ_{JA}	Fackage thermal impedance.	DCK package		252	C/VV
T _{stg}	Storage temperature range	orage temperature range		150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- The value of V_{CC} is provided in the recommended operating conditions table. (3)
- The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Ratings

			VALUE	UNIT
SN74LV	C1G04-Q1 in DBV package			
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	
V _(ESD)	V _(ESD) Electrostatic discharge Charged-device model (CDM), per JEDEC specific C101 ⁽²⁾		±750	V
SN74LV	C1G04-Q1 in DCK package			
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	V

Product Folder Links: SN74LVC1G04-Q1

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. (2)

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT					
V	Cumply valtage	Operating	1.65	5.5	\/					
V_{CC}	Supply voltage	Data retention only	1.5		V					
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}							
\/	Lligh lavel input veltage	V_{CC} = 2.3 V to 2.7 V			V					
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V					
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}							
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}						
\/	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	\/					
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V					
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}							
VI	Input voltage		0	5.5	V					
Vo	Output voltage		0	V _{CC}	V					
		V _{CC} = 1.65 V		-4						
		V _{CC} = 2.3 V		-8						
I_{OH}	High-level output current	h-level output current V_{CC} = 3 V		-16	mA					
		V _{CC} – 3 V		-24						
		V _{CC} = 4.5 V		-32						
		V _{CC} = 1.65 V		4						
		V _{CC} = 2.3 V		8						
I_{OL}	Low-level output current	V = 2 V		16	mA					
		V _{CC} = 3 V		24						
		V _{CC} = 4.5 V		32						
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20						
Δt/Δν	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		10	ns/V					
		$V_{CC} = 5 V \pm 0.5 V$		5						
т	Operating free air temperature	Q-suffix device	-40	125	°C					
T_A	Operating free-air temperature	I-suffix device	-40	85	C					

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

		SN74LVC		
	THERMAL METRIC ⁽¹⁾	DBV (SOT-23)	DCK (SC-70)	UNIT
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	357.1	371.0	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	263.7	297.5	°C/W
R _{0JB}	Junction-to-board thermal resistance	264.4	258.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	195.6	195.6	°C/W
ΨЈВ	Junction-to-board characterization parameter	262.2	256.2	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	_	_	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application note.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER	TEST CO	ONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 5.5 V	V _{CC} - 0.1				
		I _{OH} = -4 mA		1.65 V	1.2				
V _{OH}		I _{OH} = -8 mA		2.3 V	1.9			v	
		I _{OH} = -16 mA		3 V	2.4			·	
		I _{OH} = -24 mA		_ 3 v	2.3				
		I _{OH} = -32 mA	4.5 V	3.8					
		I _{OL} = 100 μA		1.65 V to 5.5 V			0.1		
		I _{OL} = 4 mA		1.65 V			0.45	1 5	
.,		I _{OL} = 8 mA	2.3 V			0.3	V		
V _{OL}		I _{OL} = 16 mA		3 V			0.4	v	
		I _{OL} = 24 mA					0.55		
		I _{OL} = 32 mA		4.5 V			0.55		
I _I	A input	V _I = 5.5 V or GND		0 to 5.5 V			±5	μA	
I _{off}		V _I or V _O = 5.5 V		0			±10	μA	
I _{CC}		V _I = 5.5 V or GND,	I _O = 0	1.65 V to 5.5 V		-	10	μA	
ΔI _{CC}		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 5.5 V			500	μA	
C _i		V _I = V _{CC} or GND		3.3 V		3.5		pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.		V _{CC} = ± 0.9		UNIT
	(INFOT)	(OUTFOT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.3		V _{CC} = ± 0.9		UNIT
	(INFOI)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Υ	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

5.8 Operating Characteristics

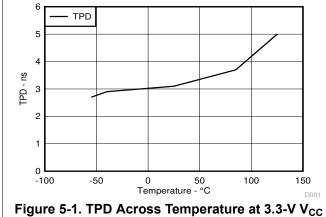
 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS TYP TYP TYP		V_{CC} = 3.3 V	V _{CC} = 5 V	UNIT	
	FANAMETER	1E31 CONDITIONS	TYP	TYP	TYP	TYP	ONII
C_{pd}	Power dissipation capacitance	f = 10 MHz	16	18	18	20	pF

Product Folder Links: SN74LVC1G04-Q1

5.9 Typical Characteristics

 $T_A = 25^{\circ}C$





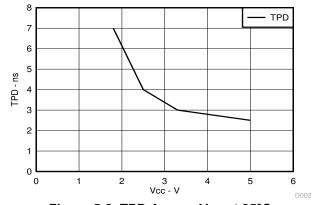
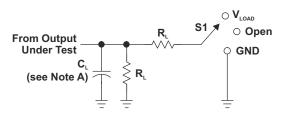


Figure 5-2. TPD Across V_{CC} at 25°C



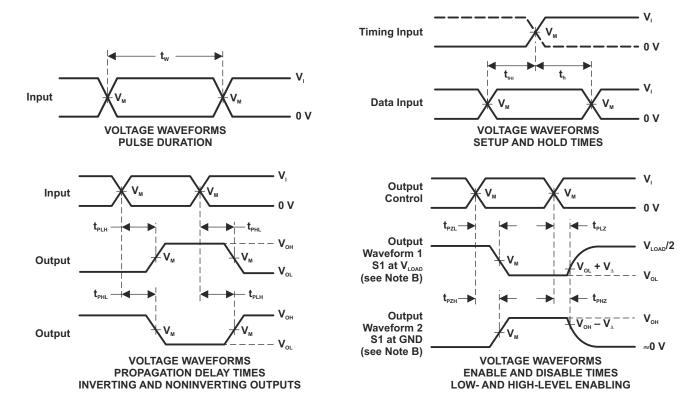
6 Parameter Measurement Information



TEST	S1		
t _{PLH} /t _{PHL}	Open		
t _{PLZ} /t _{PZL}	V _{LOAD}		
t _{PHZ} /t _{PZH}	GND		

LUAD	CIRCUIT

,,	INF	PUTS	.,	V		-	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C	$R_{\scriptscriptstyle L}$	$V_{\scriptscriptstyle{\Delta}}$
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
$2.5~\textrm{V}~\pm~0.2~\textrm{V}$	V_{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 Μ Ω	0.15 V
$3.3~V~\pm~0.3~V$	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 Μ Ω	0.3 V
5 V ± 0.5 V	V_{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

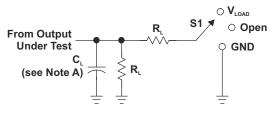
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \,\Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH}^{r2L} and t_{PHL}^{r2H} are the same as t_{pd}^{eff} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms, C_L = 15 pF

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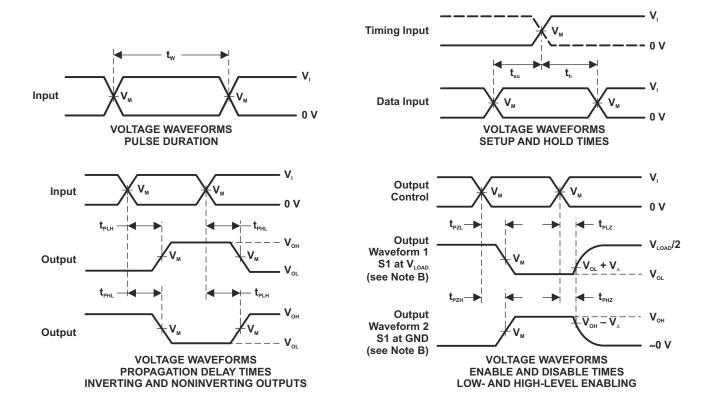




TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INPUTS			V			
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _⊾	V _A
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
$2.5~\textrm{V}~\pm~0.2~\textrm{V}$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{\odot} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}.$
- G. t_{PLH} and t_{PHL} are the same as t_{od} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms, C_L = 30 pF

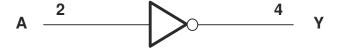
7 Detailed Description

7.1 Overview

The SN74LVC1G04-Q1 device contains inverter gate and performs the Boolean function $Y = \overline{A}$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

7.2 Functional Block Diagram



7.3 Feature Description

- · Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- · Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

7.4 Device Functional Modes

Function Table

INPUT A	OUTPUT Y
Н	L
L	н

Product Folder Links: SN74LVC1G04-Q1

8 Application and Implementation

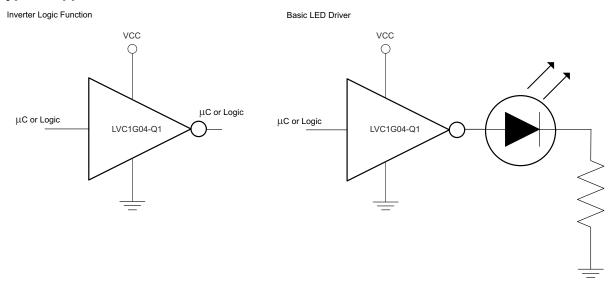
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G04-Q1 is a high drive CMOS device that can be used for implementing inversion logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 Mhz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

8.2 Typical Application



8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs: See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
 - Specified high and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I maximum) in the Recommended
 Operating Conditions table at any valid V_{CC}.
- 2. Recommend Output Conditions
 - Load currents should not exceed (I_O maximum) per output and should not exceed total current
 (continuous current through V_{CC} or GND) for the part. These limits are located in the Absolute Maximum
 Ratings table.
 - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curve

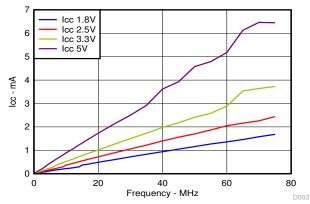


Figure 8-1. I_{CC} vs Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μ F capacitor is recommended. if there are multiple V_{CC} pins, then a 0.01 μ F or 0.022 μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μ F and 1 μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

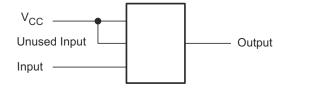
8.4.1 Layout Guidelines

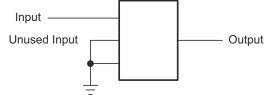
When using multiple bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The rules that must be observed under all circumstances are specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC; whichever makes more sense or is more convenient.

8.4.2 Layout Example





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9 Device and Documentation Support

9.1 Documentation Support

Related Documentation

For related documenation, see the following:

 Texas Instruments, SN74LVC1G04-Q1 Functional Safety FIT Rate and Failure Mode Distribution Functional Safety Information

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision E (June 2025) to Revision F (October 2025)	Page
•	Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371.0°C/W	5
•	Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W	/ <mark>5</mark>
•	Changed Junction-to-board thermal resistance value for DCK package from: 65°C/W to: 258.6°C/W	5
•	Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W	5
•	Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W	5

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SN74LVC1G04-Q1

SCES482F - AUGUST 2003 - REVISED OCTOBER 2025



 Added Application and Implementation section. Added Power Supply Recommendations section. 	
Added Layout section.	
Changes from Revision C (April 2008) to Revision D (January 2013)	Page
Added new list item in Features, second one with sub list items	<u>1</u>

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC1G04-Q1

www.ti.com 14-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LVC1G04QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34Z5, C04O)
SN74LVC1G04QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34Z5, C04O)
SN74LVC1G04QDBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34Z5, C04O)
SN74LVC1G04QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CCJ, CCO)
SN74LVC1G04QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CCJ, CCO)
SN74LVC1G04QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CCJ, CCO)

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF SN74LVC1G04-Q1:

● Catalog : SN74LVC1G04

● Enhanced Product : SN74LVC1G04-EP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	•
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G04QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G04QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G04QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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