

## SN74LVC1G04 Single Inverter Gate

#### 1 Features

- Available in the ultra-small 0.64mm<sup>2</sup> package (DPW) with 0.5mm pitch
- Supports 5V V<sub>CC</sub> operation
- Inputs accept voltages up to 5.5V allowing down translation to V<sub>CC</sub>
- Maximum t<sub>pd</sub> of 3.3ns at 3.3V
- Low power consumption, 10µA maximum I<sub>CC</sub>
- ±24mA output drive at 3.3V
- I<sub>off</sub> supports live-insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114-A)
  - 200V machine model (A115-A)
  - 1000V charged-device model (C101)

## 2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- Embedded PC
- MP3 player/recorder (portable audio)
- Personal Digital Assistant (PDA)
- Power: telecom/server AC/DC supply: single controller: analog and digital
- Solid State Drive (SSD): client and enterprise
- TV: LCD/digital and high-definition (HDTV)
- Tablet: enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

### 3 Description

This single inverter gate is designed for 1.65V to 5.5V V<sub>CC</sub> operation.

The SN74LVC1G04 device performs the Boolean function  $Y = \overline{A}$ .

The CMOS device has high output drive while maintaining low static power dissipation over a broad V<sub>CC</sub> operating range.

The SN74LVC1G04 device is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8mm × 0.8mm.

#### **Package Information**

DEVICE NAME	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE (NOM) <sup>(3)</sup>	
	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm	
	DCK (SC70, 5)	2.0mm × 2.1mm	2.0mm × 1.25mm	
	DPW (X2SON, 5)	0.8mm × 0.8mm	0.8mm × 0.8mm	
	DRL (SOT-5X3, 5)	1.6mm × 1.6mm	1.6mm × 1.2mm	
SN74LVC1G04	DRY (USON, 6)	1.45mm × 1.0mm	1.45mm × 1.0mm	
	DSF (X2SON, 6)	1.0mm × 1.0mm	1.0mm × 1.0mm	
	YZP (DSBGA, 5)	1.75mm × 1.75mm	1.75mm × 1.25mm	
	YZV (DSBGA, 4)	1.25mm × 1.25mm	1.25mm × 1.25mm	

- For all available packages, see the orderable addendum at the end of the datasheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



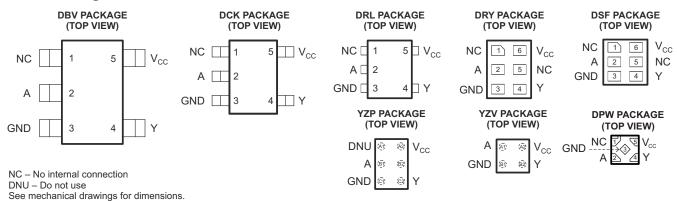


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## **4 Pin Configuration and Functions**



#### **Pin Functions**

	1 III I Unicuona													
		PIN												
NAME	DBV, DCK, DRL	DSF, DRY	YZP	YZV	DPW	DESCRIPTION								
NC	1	1, 5	A1, B2	-	1	No connect								
Α	2	2	B1	A1	2	Input								
GND	3	3	C1	B1	3	Ground								
Y	4	4	C2	B2	4	Output								
V <sub>CC</sub>	V <sub>CC</sub> 5 6		A2	A2	5	Power terminal								



## **5 Specifications**

## **5.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	6.5	V
VI	Input voltage range		-0.5	6.5	V
Vo	Voltage range applied to any output in the hig	h-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
Vo	Voltage range applied to any output in the hig	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current	·		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA	
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: SN74LVC1G04

<sup>(2)</sup> The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.



## **5.3 Recommended Operating Conditions**

(1)			MIN	MAX	UNIT
V <sub>CC</sub> Supply voltage		Operating	1.65	5.5	V
v <sub>CC</sub>	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
\/	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V
$V_{IH}$	riigii-level iriput voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
17	Low level input valtage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	,	0.3 × V <sub>CC</sub>	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V		-4	
	High-level output current	V <sub>CC</sub> = 2.3 V		-8	
$I_{OH}$		V - 2 V	,	-16	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V - 2 V	,	16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>A</sub>	Operating free-air temperature	,	-40	125	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## **5.4 Thermal Information**

		SN74LVC1G04								
	THERMAL METRIC(1)		DCK	DRL	DRY	YZP	DPW	UNIT		
		5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS			
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	357.1	278	243	439	130	340			
R <sub>0JCtop</sub>	Junction-to-case (top) thermal resistance	263.7	93	78	277	54	215	1		
R <sub>0JB</sub>	Junction-to-board thermal resistance	264.4	65	78	271	51	294	°C/W		
ΨЈТ	Junction-to-top characterization parameter	195.6	2	10	84	1	41			
ΨЈВ	Junction-to-board characterization parameter	262.2	64	77	271	50	294	1		
R <sub>0JCbot</sub>	Junction-to-case (bottom) thermal resistance	_	_	_	_	_	250	1		

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note



#### 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	V <sub>cc</sub>	-40°	C to 85°C		MENDED o 125°C	UNIT	
				MIN	TYP <sup>(1)</sup> MAX	MIN	TYP MAX		
		I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1		V <sub>CC</sub> - 0.1			
		I <sub>OH</sub> = -4 mA	1.65 V	1.2		1.2			
,		I <sub>OH</sub> = -8 mA	2.3 V	1.9	1.9			<sub>v</sub>	
V <sub>OH</sub>	$I_{OH} = -16 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$		3 V	2.4		2.4		\ \ \	
			3 V	2.3		2.3			
			4.5 V	3.8		3.8			
	$I_{OL} = 100 \mu A$ $I_{OL} = 4 mA$ $I_{OL} = 8 mA$		1.65 V to 5.5 V		0.1		0.1		
			1.65 V		0.45		0.45		
.,			2.3 V		0.3		0.3	<sub>v</sub>	
V <sub>OL</sub>		I <sub>OL</sub> = 16 mA	3 V		0.4		0.4	\ \ \	
		I <sub>OL</sub> = 24 mA	3 V		0.55		0.55		
		I <sub>OL</sub> = 32 mA	4.5 V		0.55		0.55		
I	A input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±5		±5	μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0		±10		±10	μA	
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND I <sub>O</sub> = 0	1.65 V to 5.5 V		10		10	μA	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500		500	μА	
Ci		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5		3.50	pF	

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

## 5.6 Switching Characteristics, $C_L = 15 pF$

over recommended operating free-air temperature range,  $C_L$  = 15 pF (unless otherwise noted) (see Figure 6-1)

						-40°C	to 85°C				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

## 5.7 Switching Characteristics, $C_L$ = 30 pF or 50 pF, $-40^{\circ}$ C to 85°C

over recommended operating free-air temperature range,  $C_L$  = 30 pF or 50 pF (unless otherwise noted) (see Figure 6-2)

				−40°C to 85°C							
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Y	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

Product Folder Links: SN74LVC1G04

## 5.8 Switching Characteristics, $C_L$ = 15 pF, -40°C to 125°C

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figure 6-1)

			−40°C to 125°C								
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

## 5.9 Switching Characteristics, $C_L = 30 \text{ pF}$ or 50 pF, $-40^{\circ}\text{C}$ to 125°C

over recommended operating free-air temperature range,  $C_L$  = 30 pF or 50 pF (unless otherwise noted) (see Figure 6-2)

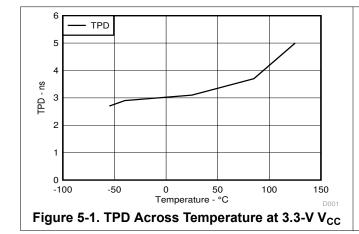
						-40°C t	o 125°C				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

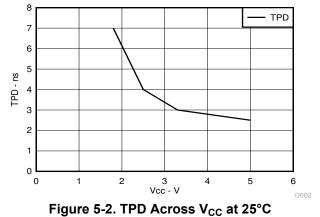
## **5.10 Operating Characteristics**

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5.0 V	UNIT
	FANAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	16	18	18	20	pF

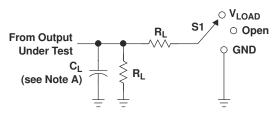
## **5.11 Typical Characteristics**







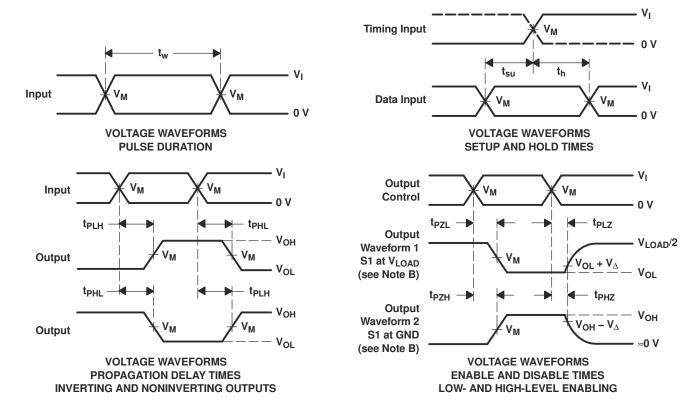
#### **6 Parameter Measurement Information**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

	CIR	

V	$\begin{array}{ c c c }\hline & \text{INPUTS} \\ \hline & V_{\text{I}} & t_{\text{r}}/t_{\text{f}} \\ \hline \end{array}$		.,	V			.,
V <sub>CC</sub>			V <sub>M</sub>	V <sub>LOAD</sub>	CL	RL	$V_{\Delta}$
1.8 V $\pm$ 0.15 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	15 pF	<b>1 Μ</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	$v_{cc}$	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	15 pF	<b>1 Μ</b> Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	<b>1 Μ</b> Ω	0.3 V
5 V $\pm$ 0.5 V	$v_{cc}$	≤2.5 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	15 pF	<b>1 Μ</b> Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

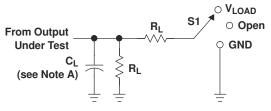
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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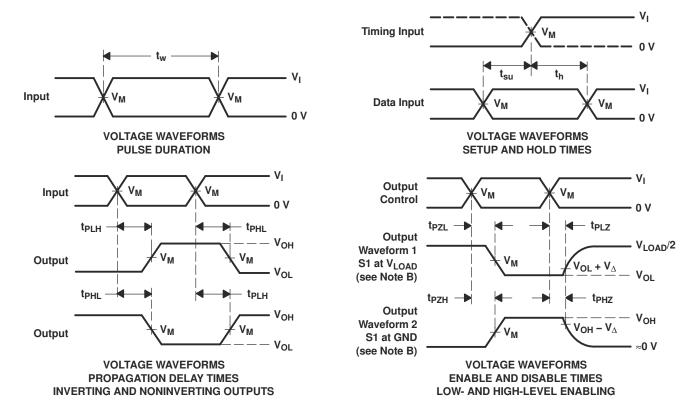




TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

V	INF	PUTS	V	V	_	В	V	
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	R <sub>L</sub>	$V_{\Delta}$	
1.8 V ± 0.15 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V	
2.5 V $\pm$ 0.2 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	500 Ω	0.15 V	
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V $\pm$ 0.5 V	V <sub>CC</sub>	≤2.5 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	50 pF	500 Ω	0.3 V	



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

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## 7 Detailed Description

#### 7.1 Overview

The SN74LVC1G04 device contains inverter gate and performs the Boolean function  $Y = \overline{A}$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

- · Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I<sub>off</sub> feature allows voltages on the inputs and outputs, when V<sub>CC</sub> is 0 V.

#### 7.4 Device Functional Modes

#### **Function Table**

INPUT A	OUTPUT Y
Н	L
L	н

Product Folder Links: SN74LVC1G04



## 8 Application and Implementation

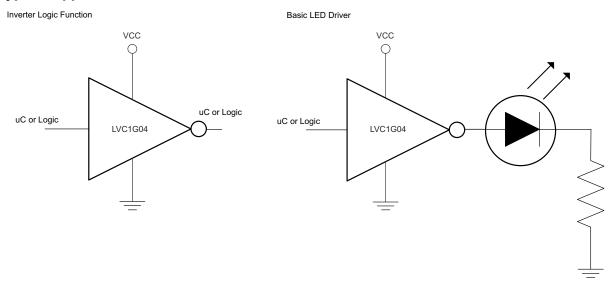
#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74LVC1G04 is a high drive CMOS device that can be used for implementing inversion logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 Mhz. The inputs are 5.5 V tolerant allowing it to translate down to  $V_{\rm CC}$ .

#### 8.2 Typical Application



#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
  - Rise time and fall time specs: See (Δt/ΔV) in the Recommended Operating Conditions table.
  - Specified high and low levels: See (V<sub>IH</sub> and V<sub>IL</sub>) in the Recommended Operating Conditions table.
  - Inputs are overvoltage tolerant allowing them to go as high as (V<sub>I</sub> max) in the Recommended Operating Conditions table at any valid V<sub>CC</sub>.
- 2. Recommend Output Conditions
  - Load currents should not exceed (I<sub>O</sub> max) per output and should not exceed total current (continuous current through V<sub>CC</sub> or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
  - Outputs should not be pulled above V<sub>CC</sub>.

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#### 8.2.3 Application Curves

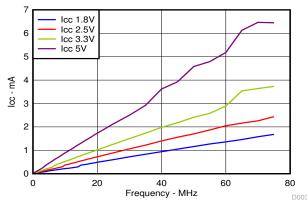


Figure 8-1. I<sub>CC</sub> vs Frequency

#### 8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. if there are multiple VCC pins, then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

#### 8.4 Layout

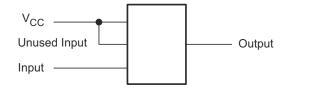
#### 8.4.1 Layout Guidelines

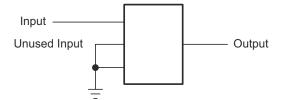
When using multiple bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The rules that must be observed under all circumstances are specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC; whichever makes more sense or is more convenient.

#### 8.4.2 Layout Example





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## 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 9.3 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	changes from Revision AD (April 2014) to Revision AE (June 2025)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Changed Device Information table to Package Information	1
•	Moved T <sub>stq</sub> to Absolute Maximum Ratings table	4
•	Changed Handling Ratings to ESD Ratings	
•	Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W	ا <mark>5</mark>
•	Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/	/W 5
•	Changed Junction-to-board thermal resistance value for DBV package from: 62°C/W to: 264.4°C/W	5
•	Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W	5
•	Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W	5
	· · · · · · · · · · · · · · · · · · ·	

Cha	anges from Revision AC (March 2014) to Revision AD (April 2014)	Page
•	Updated Features, Description, and Device Information table	1
•	Added Pin Functions table	3
•	Added Thermal Information table.	5
•	Added Detailed Description section	10
	Added Application and Implementation section	
	Added Power Supply Recommendations section	
	Added Layout section	
	•	



## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Product Folder Links: SN74LVC1G04

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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G04DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVRE4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVRG4.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVT	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVT.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVTE4	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVTG4	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVTG4.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DCK3	Last Time Buy	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CCF, CCZ)





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Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G04DCK3.B	Last Time Buy	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CCF, CCZ)
SN74LVC1G04DCKR	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKR.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKRE4	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCK, CC R) (CCH, CCP, CCS)
SN74LVC1G04DCKRE4.B	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCK, CC R) (CCH, CCP, CCS)
SN74LVC1G04DCKRG4	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5
SN74LVC1G04DCKRG4.B	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5
SN74LVC1G04DCKT	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC R) (CCH, CCP)
SN74LVC1G04DCKT.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC R) (CCH, CCP)
SN74LVC1G04DCKTE4	Active	Production	SC70 (DCK)   5	250   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTE4.B	Active	Production	SC70 (DCK)   5	250   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTG4	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTG4.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DPWR	Active	Production	X2SON (DPW)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K4
SN74LVC1G04DPWR.B	Active	Production	X2SON (DPW)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K4
SN74LVC1G04DRLR	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CC7, CCR)



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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G04DRLR.B	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CC7, CCR)
SN74LVC1G04DRY2	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRY2.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYR	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYR.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYRG4	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2G4	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2G4.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSFR	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSFR.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04YZPR	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CC7, CCN)
SN74LVC1G04YZPR.B	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CC7, CCN)
SN74LVC1G04YZVR	Active	Production	DSBGA (YZV)   4	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CC 7
SN74LVC1G04YZVR.B	Active	Production	DSBGA (YZV)   4	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CC 7

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

## PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LVC1G04:

Automotive: SN74LVC1G04-Q1

● Enhanced Product: SN74LVC1G04-EP

NOTE: Qualified Version Definitions:

- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications



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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G04DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G04DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G04DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G04DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G04DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3
SN74LVC1G04DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G04DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3



## **PACKAGE MATERIALS INFORMATION**

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G04DSF2G4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G04DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G04DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74LVC1G04YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G04YZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	2.0	8.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G04DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G04DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G04DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G04DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G04DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G04DRY2	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G04DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G04DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04DSF2G4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04DSFR	SON	DSF	6	5000	184.0	184.0	19.0



## **PACKAGE MATERIALS INFORMATION**

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	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN74LVC1G04DSFR	SON	DSF	6	5000	202.0	201.0	28.0
	SN74LVC1G04YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
ĺ	SN74LVC1G04YZVR	DSBGA	YZV	4	3000	182.0	182.0	20.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





PLASTIC SMALL OUTLINE



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.
   This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-293 Variation UAAD-1



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4211218-3/D







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. The size and shape of this feature may vary.





NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





DIE SIZE BALL GRID ARRAY



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



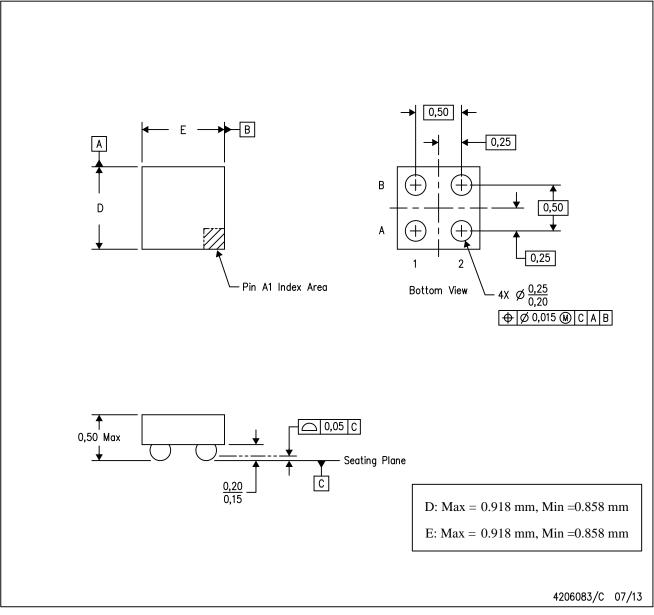
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



# YZV (S-XBGA-N4)

## DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025