









SN54LVC14A, SN74LVC14A

SCAS285AC - MARCH 1993 - REVISED APRIL 2022

SNx4LVC14A Hex Schmitt-Trigger Inverters

1 Features

- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
 - 2000-V human-body model (A114-A)
 - 200-V machine model (A115-A)
 - 1000-V charged-device model (C101)
- Operate from 1.65 V to 3.6 V V_{CC}
- Specified from -40°C to +85°C, -40°C to 125°C, and -55°C to 125°C
- Inputs accept voltages to 5.5 V
- Max t_{pd} of 6.4 ns at 3.3 V
- Typical V_{OLP} (output ground bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Barcode scanner
- Cable solutions
- E-books
- **Embedded PCs**
- Field transmitter: temperature or pressure sensors
- Fingerprint biometrics
- HVAC: heating, ventilating, and air conditioning
- Network attached storage (NAS)
- Server motherboard and PSU
- Software defined radio (SDR)
- TV: High-definition (HDTV), LCD, and digital
- Video communications systems
- Wireless data access cards, headsets, keyboards, mice, and LAN cards

3 Description

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

The devices contain six independent inverters and perform the Boolean function $Y = \overline{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54LVC14AFK	LCCC (20)	8.90 mm × 8.90 mm
SN54LVC14AJ	CDIP (14)	20.00 mm × 7.00 mm
SN54LVC14AW	CFP (14)	9.21 mm × 6.30 mm
SN74LVC14ANS	SO (14)	10.20 mm × 5.30 mm
SN74LVC14AD	SOIC (14)	8.65 mm × 6.00 mm
SN74LVC14ADB	SSOP (14)	6.20 mm × 5.30 mm
SN74LVC14APW	TSSOP (14)	5.00 mm × 4.40 mm
SN74LVC14ADGV	TVSOP (14)	4.40 mm × 3.60 mm
SN74LVC14ARGY	VQFN (14)	3.50 mm × 3.50 mm

For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)



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 Added the CMOS Schmitt-Trigger Inputs section. 			. 11
• Removed $\Delta t/\Delta v$ specifications throughout the da	ta sheet		. 14
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Updated Features1





5 Pin Configuration and Functions

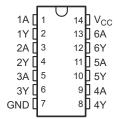


Figure 5-1. D, DB, DGV, NS, J, W, or PW Package, 14-Pin SOIC, SSOP, TVSOP, SO, CDIP, CFP, or TSSOP (Top View)

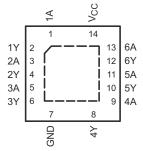


Figure 5-2. RGY Package, 14-Pin VQFN (Top View)

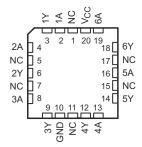


Figure 5-3. FK Package, 20-Pin LCCC (Top View)

Table 5-1. Pin Functions

	PIN						
NAME	SOIC, SSOP, TVSOP, SO, CDIP, CFP, TSSOP, VQFN	LCCC	TYPE ⁽¹⁾	DESCRIPTION			
1A	1	2	ı	Data input			
2A	3	4	I	Data input			
3A	5	8	I	Data input			
4A	9	13	I	Data input			
5A	11	16	I	Data input			
6A	13	19	ı	Data input			
GND	7	10	_	Ground			
V _{CC}	14	20	_	Positive supply			
1Y	2	3	0	Data output			
2Y	4	6	0	Data output			
3Y	6	9	0	Data output			
4Y	8	12	0	Data output			
5Y	10	14	0	Data output			
6Y	12	18	0	Data output			
		1					
		5					
NC		7		No connection			
NC	_	11		No connection			
		15					
		17					

(1) I = input, O = output



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	6.5	V
VI	Input voltage ⁽²⁾		-0.5	6.5	V
Vo	Output voltage ^{(2) (3)}	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
P _{tot}	Power dissipation	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}^{(4)}$ (5)		500	mW
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.
- (4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (5) For the DB, DGV, NS, and PW packages: above 60°C, the value of Ptot derates linearly with 5.5 mW/K.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	+2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	+1000	V
	aleenal ge	Machine Model	200	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions: SN54LVC14A

See (1)

			SN54L	SN54LVC14A		
			-55 TO	+125°C	UNIT	
			MIN	MAX		
,,	Cumply veltage	Operating	2	3.6	V	
V _{CC}		Data retention only	1.5		V	
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
	High lovel output ourrent	V _{CC} = 2.7 V		-12	mA	
I _{OH}	High-level output current	V _{CC} = 3 V		-24] IIIA	
	OL Low-level output current	V _{CC} = 2.7 V		12	mA	
OL		V _{CC} = 3 V		24	1 111/4	

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions: SN74LVC14A

See (1)

					SN74LV	C14A				
			T _A = 25°C		-40 TO +85°C		-40 TO +125°C		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
\/	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V	
V _{CC}	Supply Voltage	Data retention only	1.5		1.5		1.5		V	
VI	Input voltage		0	5.5	0	5.5	0	5.5	V	
Vo	Output voltage		0	V _{CC}	0	V _{CC}	0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		-4		-4	_4 8mA	
	High-level output current	V _{CC} = 2.3 V		-8		-8		-8		
I _{OH}	nigii-level output current	V _{CC} = 2.7 V		-12		-12		-12	ША	
		V _{CC} = 3 V		-24		-24		-24		
		V _{CC} = 1.65 V		4		4		4		
	Law lavel autout aurrent	V _{CC} = 2.3 V		8		8		8	no A	
l _{OL}	Low-level output current	V _{CC} = 2.7 V		12		12		12	mA	
		V _{CC} = 3 V		24		24		24		

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.5 Thermal Information

				SN74L	_VC14A			
	THERMAL METRIC ⁽¹⁾	D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SO)	PW (TSSOP)	RGY (LCCC)	UNIT
				14 PINS			20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.6	131.8	153.5	115.7	145.9	93.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.2	83.9	75.2	72.2	73.4	106.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.9	79.2	86.6	74.4	87.7	69.8	°C/W
ΨЈТ	Junction-to-top characterization parameter	39.3	41.7	19.9	33.7	18.9	22.0	°C/W
ΨЈВ	Junction-to-board characterization parameter	71.6	78.6	85.9	74.1	87.1	70.0	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	_	_	_	_	_	49.4	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics, SN54LVC14A

over operating free-air temperature range (unless otherwise noted)

				SN54		
PARAMETER		TEST CONDITIONS	V _{cc}	-55 TC	UNIT	
				MIN	TYP MAX	
		2.7 V	0.8	2		
V_{T+}	V _{T+} Positive-going threshold		3 V	0.9	2	V
			3.6 V	1.1	2	
			2.7 V	0.4	1.4	
V_{T-}	V _T — Negative-going threshold		3 V	0.6	1.5	V
			3.6 V	0.8	1.7	



6.6 Electrical Characteristics, SN54LVC14A (continued)

over operating free-air temperature range (unless otherwise noted)

			SN54	ILVC14A	UNIT	
PARAMETER	TEST CONDITIONS	V _{cc}	–55 T	O +125°C		
			MIN	TYP MAX		
		2.7 V	0.3	1.1		
ΔV_T Hysteresis $(V_{T+} - V_{T-})$		3 V	0.3	1.2	V	
(*1+ *1-/		3.6 V	0.3	1.2		
	I _{OH} = -100 μA	2.7 V to 3.6 V	V _{CC} - 0.2			
V _{OH}	.,	2.7 V	2.2		V	
	V _{OL}	I _I	2.4			
	Icc	3 V	2.2		7	
	Ι _{ΟL} = 100 μΑ	2.7 V to 3.6 V		0.2		
ΔI _{CC}	Ci	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
	V _I = 5.5 V or GND	3.6 V		±5	μA	
	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μA	
	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V		500	μA	
	V _I = V _{CC} or GND	3.3 V		5 ⁽¹⁾	pF	

⁽¹⁾ $T_A = 25^{\circ}C$

6.7 Electrical Characteristics, SN74LVC14A

over operating free-air temperature range (unless otherwise noted)

							SN74LVC14A						
PA	RAMETER	TEST	Vcc	T _A :	= 25°C		-40 TO +8	5°C	-40 TO +1	25°C	UNIT		
		CONDITIONS		CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
		1.65 V	0.4		1.3	0.4	1.3	0.4	1.3				
			1.95 V	0.6		1.5	0.6	1.5	0.6	1.5			
	Positive-		2.3 V	0.8		1.7	0.8	1.7	0.8	1.7			
V _{T+} going threshold		2.5 V	0.8		1.7	0.8	1.7	0.8	1.7	V			
		2.7 V	0.8		2	0.8	2	0.8	2				
			3 V	0.9		2	0.9	2	0.9	2			
			3.6 V	1.1		2	1.1	2	1.1	2			
			1.65 V	0.15		0.85	0.15	0.85	0.15	0.85			
			1.95 V	0.25		0.95	0.25	0.95	0.25	0.95			
	Negative-		2.3 V	0.4		1.2	0.4	1.2	0.4	1.2			
V _T _	going		2.5 V	0.4		1.2	0.4	1.2	0.4	1.2	V		
threshold		2.7 V	0.4		1.4	0.4	1.4	0.4	1.4				
			3 V	0.6		1.5	0.6	1.5	0.6	1.5			
			3.6 V	0.8		1.7	0.8	1.7	0.8	1.7			



6.7 Electrical Characteristics, SN74LVC14A (continued)

over operating free-air temperature range (unless otherwise noted)

						SN74LVC14A				
PARAMETER	TEST CONDITIONS	V _{CC}	T _A :	= 25°C		-40 TO +8	5°C	-40 TO +1	25°C	UNIT
	00.121110110		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
		1.65 V	0.1		1.15	0.1	1.15	0.1	1.15	
		1.95 V	0.15		1.25	0.15	1.25	0.15	1.25	
		2.3 V	0.25		1.3	0.25	1.3	0.25	1.3	
ΔV_T Hysteresis $(V_{T+} - V_{T-})$		2.5 V	0.25		1.3	0.25	1.3	0.25	1.3	V
(*1+ *1-)		2.7 V	0.3		1.1	0.3	1.1	0.3	1.1	
		3 V	0.3		1.2	0.3	1.2	0.3	1.2	
		3.6 V	0.3		1.2	0.3	1.2	0.3	1.2	
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V _{CC} - 0.2		V _{CC} - 0.3		
V _{OH}	I _{OH} = -4 mA	1.65 V	1.29			1.2		1.05		V
	I _{OH} = -8 mA	2.3 V	1.9			1.7		1.65		
	40 4	2.7 V	2.2			2.2	2.05			
	$I_{OH} = -12 \text{ mA}$	3 V	2.4			2.4		2.25		
	I _{OH} = -24 mA	3 V	2.3			2.2		2		
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.1		0.2		0.3	
	I _{OL} = 4 mA	1.65 V			0.24		0.45		0.6	
V_{OL}	I _{OL} = 8 mA	2.3 V			0.3		0.7		0.75	V
	I _{OL} = 12 mA	2.7 V			0.4		0.4		0.6	
	I _{OL} = 24 mA	3 V			0.55		0.55		0.8	
I _I	V _I = 5.5 V or GND	3.6 V			±1		±5		±20	μA
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			1		10		40	μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500		500		5000	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V		5						pF

6.8 Switching Characteristics, SN54LVC14A

over operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

				SN54LVC	14A	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	-55 TO +1	UNIT	
	(5.)	(55.1.5.)		MIN	MAX	
+	٨	V	2.7 V		7.5	
t _{pd}	A	ī	3.3 V ± 0.3 V	1	6.4	ns



6.9 Switching Characteristics, SN74LVC14A

over operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

. 5	,	TO (OUTPUT)	V _{cc}								
PARAMETER	FROM (INPUT)			T _A = 25°C			-40 TO +85°C		−40 TO +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
		1.8 V ± 0.15 V	1	5	10.5	1	11	1	13		
t .	Α	Y	2.5 V ± 0.2 V	1	3.4	7.3	1	7.8	1	10	ns
t _{pd}	A		2.7 V	1	3.6	7.3	1	7.5	1	9.5	115
			3.3 V ± 0.3 V	1	3.2	6.2	1	6.4	1	8	
t _{sk(o)}			3.3 V ± 0.3 V			1		1		1.5	ns

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	11	12	15	pF

6.11 Typical Characteristics

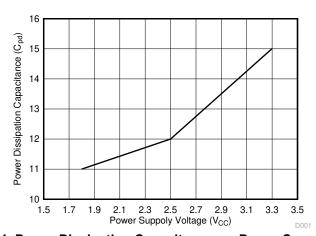
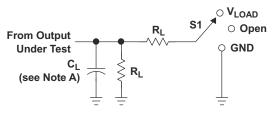


Figure 6-1. Power Dissipation Capacitance vs. Power Supply Voltage



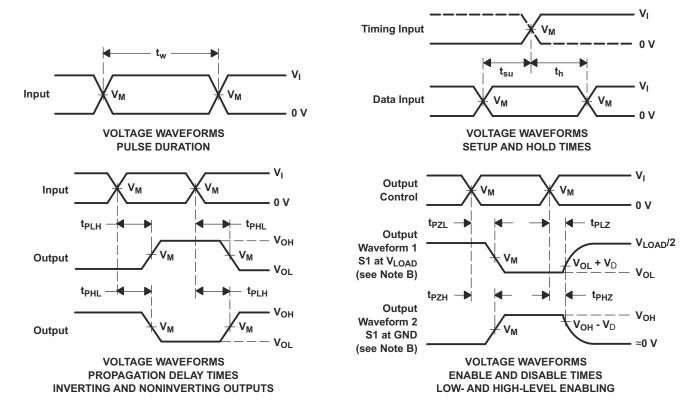
7 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INF	PUTS	.,	V	0		.,
V _{CC}	VI	t _r /t _f	V _M	V_{LOAD}	CL	R_L	V D
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	1 kW	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 W	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 W.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms



8 Detailed Description

8.1 Overview

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

The devices contain six independent inverters and perform the Boolean function $Y = \overline{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

8.2 Functional Block Diagram



Figure 8-1. Logic Diagram, Each Inverter (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* section must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law $(R = V \div I)$.

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

8.3.3 Clamp Diodes

The inputs to this device have negative clamping diodes. The outputs to this device have both positive and negative clamping diodes as shown in Figure 8-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



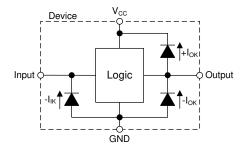


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings table*.

8.4 Device Functional Modes

Table 8-1 lists the functional modes for the SN54LVC14A and SN74LVC14A devices.

Table 8-1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

9 Application and Implementation

Note

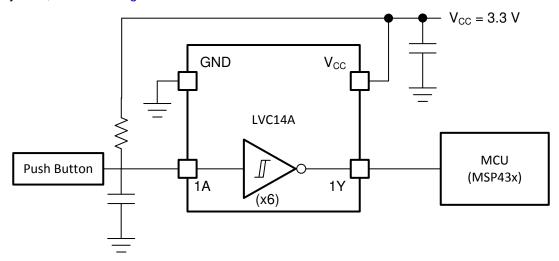
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Physically interactive interface elements like push buttons or rotary knobs offer simple and easy ways to interact with an electronic system. Many of these physical interface elements often have issues with bouncing, or where the physical conductive contact can connect and disconnect multiple times during a button push or release. This bouncing can cause one or more faulty transient signals to be passed during this transitional period. These faulty signals can be observed in many common applications: for example, a television remote with bouncing error can adjust the TV channel multiple times despite the button being pushed only once. To mitigate these faulty signals, use a Schmitt-trigger, or a device with hysteresis, to remove these faulty signals. Hysteresis allows a device to remember its history, and in this case, the LVC14A uses this memory to debounce the physical element's signal, or filter the faulty transient signals and pass only the valid signal each time the element is used. In this example, we show a push button signal passed through an LVC14A that is debounced and inverted to the MCU for push detection.

9.2 Typical Application

The signal effects of the debounce circuit can be seen when comparing Figure 9-2 and Figure 9-3. In Figure 9-2, the input is a very poor quality signal due to the error in the physical push button. If the MCU attempts to sample this input to detect a push, there is high probability that multiple push events will be falsely detected. Once the debounce circuit has been implemented, the input is cleaned up, and the MCU can perform push detection without any error, as seen in Figure 9-3.



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Figure 9-1. Debouncer Application Diagram

9.2.1 Design Requirements

The SN74LVC14A device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

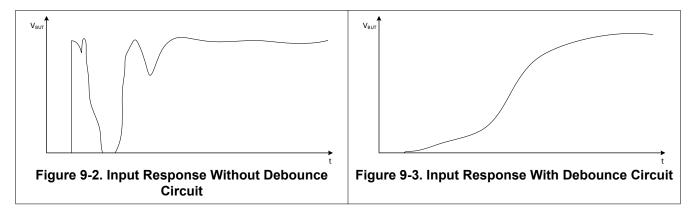
The SN74LVC14A allows for performing logical Boolean functions with hysteresis using digital signals. All input signals should remain as close as possible to either 0 V or V_{CC} for optimal operation.



9.2.2 Detailed Design Procedure

- 1. Recommended input conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in the Recommended Operating Conditions: SN74LVC14A table.
 - Inputs and outputs are overvoltage tolerant and can therefore go as high as 3.6 V at any valid $V_{\rm CC}$.
- 2. Recommended output conditions:
 - Load currents should not exceed ±50 mA.
- 3. Frequency selection criterion:
 - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the Layout section

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Absolute Maximum Ratings* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.



11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. Figure 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

11.2 Layout Examples

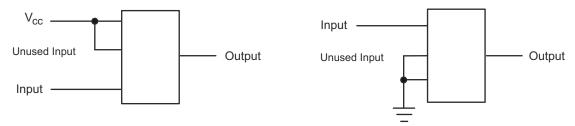


Figure 11-1. Layout Diagrams



12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, Implications of Slow or Floating CMOS Inputs application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossarv

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9761501Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9761501Q2A SNJ54LVC 14AFK
5962-9761501QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761501QC A SNJ54LVC14AJ
5962-9761501QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761501QD A SNJ54LVC14AW
5962-9761501V2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9761501V2A SNV54LVC 14AFK
5962-9761501VCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761501VC A SNV54LVC14AJ
5962-9761501VDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761501VD A SNV54LVC14AW
SN74LVC14AD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14AD.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ADBR.B	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ADBRE4	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ADE4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADG4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ADGVR.B	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ADGVRG4	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ADGVRG4.B	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC14ADRE4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADRG3	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADRG3.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADRG4.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADT	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ADT.B	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ANSR.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ANSRG4	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14ANSRG4.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A
SN74LVC14APW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWG4	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWRE4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWRG3	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWRG3.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWT	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWT.B	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14APWTG4	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A
SN74LVC14ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC14A
SN74LVC14ARGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC14A
SN74LVC14ARGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC14A
SNJ54LVC14AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9761501Q2A SNJ54LVC 14AFK

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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SNJ54LVC14AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761501QC A SNJ54LVC14AJ
SNJ54LVC14AW	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761501QD A SN 1541 VC14AW

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC14A, SN54LVC14A-SP, SN74LVC14A:

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

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• Catalog : SN74LVC14A, SN54LVC14A

• Automotive : SN74LVC14A-Q1, SN74LVC14A-Q1

● Enhanced Product : SN74LVC14A-EP, SN74LVC14A-EP

• Military : SN54LVC14A

• Space : SN54LVC14A-SP

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

• Military - QML certified for Military and Defense Applications

• Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC14ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC14ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC14ADGVRG4	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74LVC14ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ANSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74LVC14ANSRG4	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74LVC14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC14ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVC14ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVC14ADGVRG4	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVC14ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC14ADRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC14ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74LVC14ADT	SOIC	D	14	250	213.0	191.0	35.0
SN74LVC14ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC14ANSRG4	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC14APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC14APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC14APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC14APWT	TSSOP	PW	14	250	353.0	353.0	32.0
SN74LVC14ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9761501Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9761501QDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-9761501V2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9761501VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC14AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC14AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC14ADE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC14ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC14APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC14APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC14APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC14AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC14AW	W	CFP	14	25	506.98	26.16	6220	NA

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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