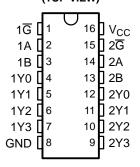
SCAS3410-MARCH 1994-REVISED FEBRUARY 2005

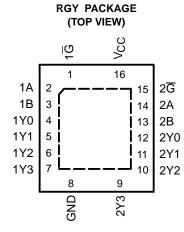
FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.2 ns
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C

D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This dual 2-line to 4-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The device comprises two individual 2-line to 4-line decoders in a single package. The active-low enable (\overline{G}) input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

T _A	PACKAGE	(1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	QFN – RGY	Reel of 1000	SN74LVC139ARGYR	LC139A	
		Tube of 40	SN74LVC139AD		
	SOIC - D	Reel of 2500	SN74LVC139ADR	LVC139A	
		Reel of 250	SN74LVC139ADT		
	SOP - NS	Reel of 2000	SN74LVC139ANSR	LVC139A	
–40°C to 85°C	SSOP - DB	Reel of 2000	SN74LVC139ADBR	LC139A	
-40°C 10 65°C		Tube of 90	SN74LVC139APW	LOTSON	
	TSSOP – PW	Reel of 2000	SN74LVC139APWR	LC139A	
		Reel of 250	SN74LVC139APWT		
	TVSOP - DGV	Reel of 2000	SN74LVC139ADGVR	LC139A	
	VFBGA – GQN	Reel of 1000	SN74LVC139AGQNR	1.04004	
	VFBGA – ZQN (Pb-free)	Reel of 1000	SN74LVC139AZQNR	LC139A	

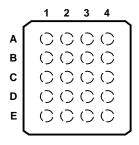
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



GQN OR ZQN PACKAGE (TOP VIEW)



TERMINAL ASSIGNMENTS

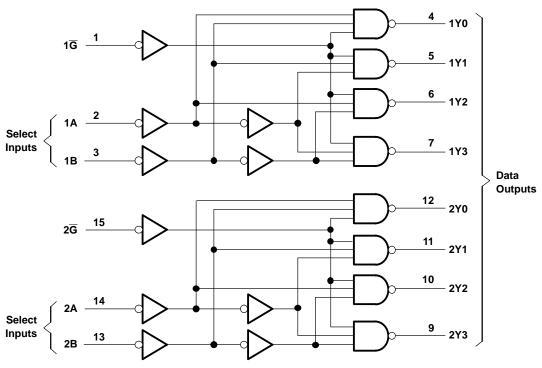
	1	2	3	4
Α	1A	1 G	V_{CC}	2 G
В	1B	NC ⁽¹⁾	NC ⁽¹⁾	2A
С	1Y1	1Y0	2Y0	2B
D	1Y2	NC ⁽¹⁾	NC ⁽¹⁾	2Y1
Е	GND	1Y3	2Y3	2Y2

(1) NC - No internal connection

FUNCTION TABLE (EACH DECODER/DEMULTIPLEXER)

	INPUTS			OUTPUTS				
G	SELECT			0011	-013			
G	В	Α	Y3	Y2	Y1	Y0		
L	L	L	Н	Н	Н	L		
L	L	Н	Н	Н	L	Н		
L	Н	L	Н	L	Н	Н		
L	Н	Н	L	Н	Н	Н		
Н	Х	Χ	Н	Н	Н	Н		

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, DGV, NS, PW, and RGY packages.



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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT		
V_{CC}	Supply voltage range		-0.5	6.5	V		
V_{I}	Input voltage range ⁽²⁾		-0.5	6.5	V		
Vo	Output voltage range (2)(3)		-0.5	V _{CC} + 0.5	V		
I _{IK}	Input clamp current	V _I < 0		-50	mA		
I _{OK}	Output clamp current	V _O < 0		-50	mA		
Io	Continuous output current			±50	mA		
	Continuous current through V _{CC} or GND			±100	mA		
	0 00	D package ⁽⁴⁾		73			
		DB package ⁽⁴⁾		82			
		DGV package ⁽⁴⁾		120			
θ_{JA}	Package thermal impedance	GQN/ZQN package ⁽⁴⁾		78	°C/W		
		NS package ⁽⁴⁾		64			
		PW package ⁽⁴⁾		108			
		RGY package (5)					
T _{stg}	Storage temperature range		-65	150	°C		

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed. The value of V_{CC} is provided in the recommended operating conditions table.
- The package thermal impedance is calculated in accordance with JESD 51-7.
- The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
\/	Cupply valtage	Operating	1.65	3.6	W	
V_{CC}	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V	
		V _{CC} = 2.7 V to 3.6 V	2			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		V _{CC} = 2.7 V to 3.6 V		0.8		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		
	High lavel autout august	V _{CC} = 2.3 V		-8	A	
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
	Lave laval autout august	V _{CC} = 2.3 V		8	A	
l _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN74LVC139A DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER





Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST CONDITI	IONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT	
		$I_{OH} = -100 \mu A$		1.65 V to 3.6 V	$V_{CC} - 0.2$				
	$I_{OH} = -4 \text{ mA}$				1.2				
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		$I_{OH} = -8 \text{ mA}$		2.3 V	1.7			V	
V _{OH}		12 12		2.7 V	2.2			V	
		$I_{OH} = -12 \text{ mA}$		3 V	2.4				
I _{OH} = -24 mA				3 V	2.2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
V _{OL}		I _{OL} = 8 mA		2.3 V			0.7	V	
		I _{OL} = 12 mA		2.7 V			0.4		
		I _{OL} = 24 mA		3 V			0.55		
I	All inputs	V _I = 5.5 V or GND		3.6 V			±5	μΑ	
I _{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	0	3.6 V			10	μΑ	
ΔI_{CC}		One input at V _{CC} – 0.6 V, Othe	r inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μΑ	
C _i		$V_I = V_{CC}$ or GND		3.3 V		5		pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = 1 ± 0.3	3.3 V 3 V	UNIT
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	A or B	V	1	20.6	1	9.3	1	7.3	1	6.2	2
^L pd	G	ľ	1	19.5	1	7.2	1	5.2	1	4.7	ns
t _{sk(o)}										1	ns

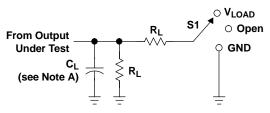
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	28.5	29.5	30.5	pF



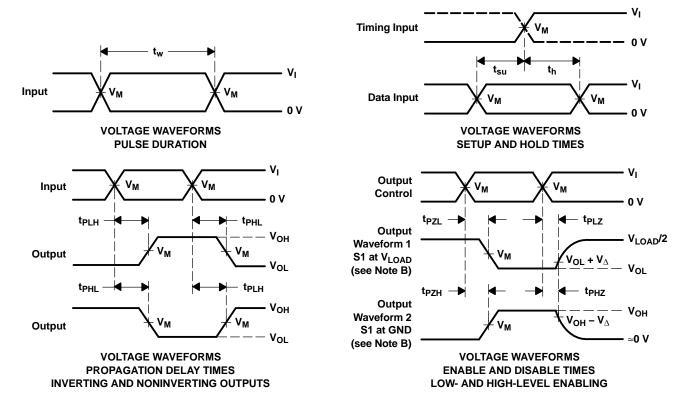
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V	INF	PUTS	.,	W	•		.,	
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	RL	$V_{\!\scriptscriptstyle \Delta}$	
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V	
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V	
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC139AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139AD.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ADBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139ADBR.B	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139ADGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139ADGVR.B	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ADR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ADRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ADT	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ADT.B	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139ANSR.B	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC139A
SN74LVC139APW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APW.B	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWE4	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWRG4.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWT	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139APWT.B	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC139A
SN74LVC139ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC139A
SN74LVC139ARGYR.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC139A
SN74LVC139ARGYRG4	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC139A
SN74LVC139ARGYRG4.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC139A

PACKAGE OPTION ADDENDUM

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- (1) Status: For more details on status, see our product life cycle.
- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC139A:

Automotive: SN74LVC139A-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC139ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC139ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC139ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC139ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC139APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC139APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC139APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC139ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74LVC139ARGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1



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*All dimensions are nominal

All difficultions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC139ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LVC139ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74LVC139ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LVC139ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LVC139APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC139APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC139APWT	TSSOP	PW	16	250	353.0	353.0	32.0
SN74LVC139ARGYR	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74LVC139ARGYRG4	VQFN	RGY	16	3000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC139AD	D	SOIC	16	40	507	8	3940	4.32
SN74LVC139AD.B	D	SOIC	16	40	507	8	3940	4.32
SN74LVC139APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC139APW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC139APWE4	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.





SOP



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025