

# SN74LV8T240-EP Enhanced Product, Octal Inverting Buffers/Drivers with 3-State **Outputs**

#### 1 Features

- Wide operating range of 1.65V to 5.5V
- 5.5V tolerant input pins
- Single-supply voltage translator (refer to LVxT Enhanced Input Voltage):
  - Up translation:
    - 1.2V to 1.8V
    - 1.5V to 2.5V
    - 1.8V to 3.3V
    - 3.3V to 5.0V
  - Down translation:
    - 5.0V, 3.3V, 2.5V to 1.8V
    - 5.0V, 3.3V to 2.5V
    - 5.0V to 3.3V
- Up to 150Mbps with 5V or 3.3V  $V_{CC}$
- Supports standard function pinout
- Latch-up performance exceeds 250mA per JESD 17
- Supports defense and aerospace applications:
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Extended product life cycle
  - Product traceability

### 2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

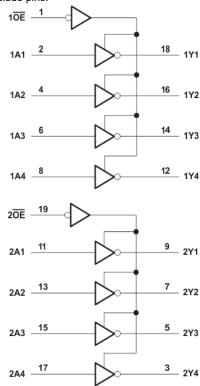
# 3 Description

SN74LV8T240-EP device contains independent inverting line drivers with 3-state outputs. Each channel performs the Boolean function  $Y = \overline{A}$ in positive logic. The channels are grouped in sets of four, with one  $\overline{OE}$  pin controlling each set. The outputs can be put into a hi-Z state by applying a high on the associated OE pin.

**Package Information** 

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LV8T240-EP	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm

- For more information, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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# **4 Pin Configuration and Functions**

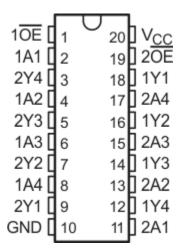


Figure 4-1. SN74LV240A PW Package; 20-Pin TSSOP (Top View)

**Table 4-1. Pin Functions** 

NAME <sup>(1)</sup>	PIN	TYPE	DESCRIPTION
10E	1	I	Output enable 1
1A1	2	I	1A1 input
2Y4	3	0	2Y4 output
1A2	4	ı	1A2 input
2Y3	5	0	2Y3 output
1A3	6	I	1A3 input
2Y2	7	0	2Y2 output
1A4	8	ı	1A4 input
2Y1	9	0	2Y1 output
GND	10	_	Ground pin
2A1	11	I	2A1 input
1Y4	12	0	1Y4 output
2A2	13	I	2A2 input
1Y3	14	0	1Y3 output
2A3	15	I	2A3 input
1Y2	16	0	1Y2 output
2A4	17	I	2A4 input
1Y1	18	0	1Y1 output
20E	19	I	Output enable 2
VCC	20	_	Power pin

<sup>(1)</sup> Signal Types: I = Input, O = Output, I/O = Input or Output



# **5 Specifications**

# 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
VI	Input voltage range <sup>(2)</sup>		-0.5	7	V
Vo	Voltage range applied to any outp	out in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
Vo	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < -0.5V		-20	mA
I <sub>OK</sub>	Output clamp current	$V_{O}$ < -0.5V or $V_{O}$ > $V_{CC}$ + 0.5V		±20	mA
Io	Continuous output current	$V_O = 0$ to $V_{CC}$		±25	mA
	Continuous output current through	n V <sub>CC</sub> or GND		±50	mA
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

# 5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
V <sub>(ESD)</sub>	discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

# **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.8	5.5	V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65V to 2V	1.1		
V	High lovel input voltage	V <sub>CC</sub> = 2.25V to 2.75V	1.28		V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3V to 3.6V	1.45		V
		V <sub>CC</sub> = 4.5V to 5.5V	2		
		V <sub>CC</sub> = 1.65V to 2V		0.5	
V	Low-Level input voltage	V <sub>CC</sub> = 2.25V to 2.75V		0.65	V
V <sub>IL</sub>		V <sub>CC</sub> = 3V to 3.6V		0.75	V
		V <sub>CC</sub> = 4.5V to 5.5V		0.85	
		V <sub>CC</sub> = 1.6V to 2V		±3	
$I_{O}$	Output current	V <sub>CC</sub> = 2.25V to 2.75V		±7	mA
		V <sub>CC</sub> = 3.3V to 5.0V		±15	
Io	Output Current	V <sub>CC</sub> = 4.5V to 5.5V		±25	mA
Δt/Δν	Input transition rise or fall rate	V <sub>CC</sub> = 1.6V to 5.0V		20	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	°C

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<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.



### **5.4 Thermal Information**

PACKAGE PINS THERMAL METRIC(1)							UNIT	
FACRAGE	FINS	$R_{\theta JA}$ $R_{\theta JC(top)}$ $R_{\theta JB}$ $\Psi_{JT}$ $\Psi_{JB}$ $R_{\theta JC(bot)}$						ONIT
PW (TSSOP)	20	101.7	42.9	63.4	3.7	62.7	-	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application (1) note.

### 5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at  $T_A$  = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
	I <sub>OH</sub> = -50μA	1.2V to 5.5V	V <sub>CC</sub> -0.2			
	I <sub>OH</sub> = -1mA	1.2V	0.8			
	I <sub>OH</sub> = -2mA	1.65V to 2V	1.21	1.7 <sup>(1)</sup>		
V <sub>OH</sub>	I <sub>OH</sub> = -3mA	2.25V to 2.75V	1.93	2.4 <sup>(1)</sup>		V
	I <sub>OH</sub> = -5.5mA	3V to 3.6V	2.49	3.08(1)		
	I <sub>OH</sub> = -8mA	4.5V to 5.5V	3.95	4.65 <sup>(1)</sup>		
	I <sub>OH</sub> = –24mA	4.5V to 5.5V	3.15			
	I <sub>OL</sub> = 50μA	1.2V to 5.5V			0.1	
	I <sub>OL</sub> = 1mA	1.2V			0.2	
	I <sub>OL</sub> = 2mA	1.65V to 2V		0.1(1)	0.25	V
V <sub>OL</sub>	I <sub>OL</sub> = 3mA	2.25V to 2.75V		0.1 <sup>(1)</sup>	0.2	
	I <sub>OL</sub> = 5.5mA	3V to 3.6V		0.2(1)	0.25	
	I <sub>OL</sub> = 8mA	4.5V to 5.5V		0.3 <sup>(1)</sup>	0.35	
	I <sub>OL</sub> = 24mA	4.5V to 5.5V			0.75	
I <sub>I</sub>	V <sub>I</sub> = 0V or V <sub>CC</sub>	0V to 5.5V		±0.1	±1	μA
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	1.8V to 5.5V		2	20	μA
	One input at 0.3V or 3.4V, other inputs at 0 or $V_{CC}$ , $I_{O}$ = 0	5.5V		1.35	1.5	mA
Δlcc	One input at 0.3V or 1.1V, other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	1.8V			68	μА
Cı	V <sub>I</sub> = V <sub>CC</sub> or GND	5V		3	5	pF
Co	V <sub>O</sub> = V <sub>CC</sub> or GND	5V		5	8	pF
loz	$V_O = V_{CC}$ or GND and $V_{CC} = 5.5V$	5.5V			±2.5	μΑ
C <sub>PD</sub> (2) (3)	C <sub>L</sub> = 50pF, F = 10MHz	1.8V to 5.5V			200	pF

- Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)  $C_{PD}$  is used to determine the dynamic power consumption, per channel.  $P_D = V_{CC}^2 x F_I x (C_{PD} + C_L)$  where  $F_I =$  input frequency,  $C_L =$  output load capacitance,  $V_{CC} =$  supply voltage.

# 5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25$ °C (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT) Load Cap	Lood Consoitance	oad Capacitance V <sub>CC</sub>	-55°C to 125°C			UNIT
PARAMETER	PROW (INPUT)		Load Capacitance		MIN	TYP	MAX	ONT
t <sub>PHL</sub>	A	Υ	C <sub>L</sub> = 15pF	1.8		15.5	18.0	nS
t <sub>PHL</sub>	A	Υ	C <sub>L</sub> = 50pF	1.8		20	22.5	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 15pF	1.8		27.4	31.0	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 50pF	1.8		34	37.5	nS
t <sub>PLH</sub>	A	Υ	C <sub>L</sub> = 15pF	1.8		16.6	19.0	nS



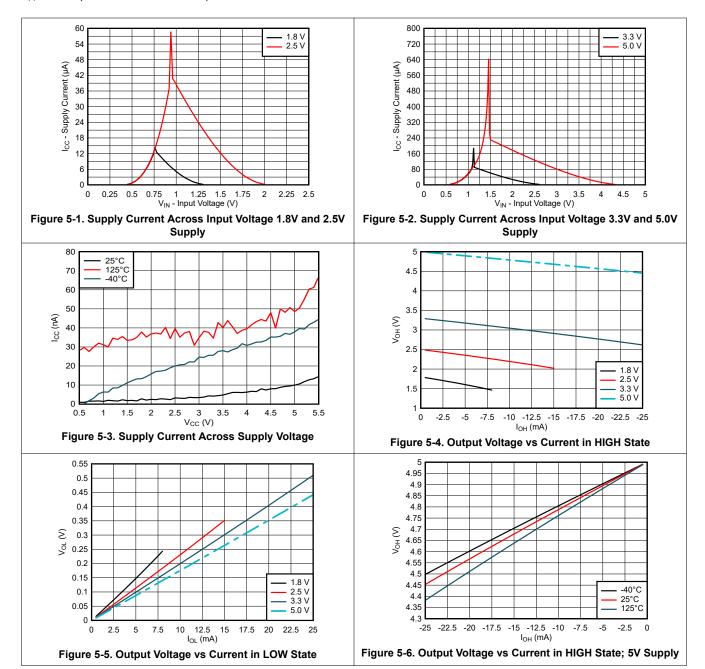
over operating free-air temperature range; typical values measured at  $T_A$  = 25°C (unless otherwise noted)

		ange; typical values measured at $I_A = $ TO (OUTPUT) Load Capacitance		-55°C to 125°C				
PARAMETER	FROM (INPUT)		Load Capacitance	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	А	Υ	C <sub>L</sub> = 50pF	1.8		19.7	22.8	nS
t <sub>PLZ</sub>	OE	Υ	C <sub>L</sub> = 15pF	1.8		24.5	27.5	nS
t <sub>PLZ</sub>	OE	Υ	C <sub>L</sub> = 50pF	1.8		31.2	34.5	nS
t <sub>PZH</sub>	OE	Υ	C <sub>L</sub> = 15pF	1.8		26.8	31.5	nS
t <sub>PZH</sub>	OE	Υ	C <sub>L</sub> = 50pF	1.8		30.6	35.5	nS
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 15pF	1.8		27.8	32.0	nS
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 50pF	1.8		32.6	37.0	nS
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 15pF	2.5		8.59	14	nS
t <sub>PHL</sub>	А	Υ	C <sub>L</sub> = 50pF	2.5		11.7	17	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 15pF	2.5		15.4	18.0	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 50pF	2.5		20	23.0	nS
t <sub>PLH</sub>	Α	Υ	C <sub>L</sub> = 15pF	2.5		9.59	14	nS
t <sub>PLH</sub>	Α	Υ	C <sub>L</sub> = 50pF	2.5		11.7	17	nS
t <sub>PLZ</sub>	OE	Υ	C <sub>L</sub> = 15pF	2.5		13.8	16.5	nS
t <sub>PLZ</sub>	OE	Υ	C <sub>L</sub> = 50pF	2.5		18.5	21	nS
t <sub>PZH</sub>	OE	Υ	C <sub>L</sub> = 15pF	2.5		15.3	19.0	nS
t <sub>PZH</sub>	OE	Υ	C <sub>L</sub> = 50pF	2.5		17.6	21.5	nS
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 15pF	2.5		15.6	19.5	nS
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 50pF	2.5		18.8	23.0	nS
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 15pF	3.3		6.09	9	nS
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 50pF	3.3		8.47	12.5	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 15pF	3.3		10.8	13	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 50pF	3.3		14.2	17	nS
t <sub>PLH</sub>	Α	Υ	C <sub>L</sub> = 15pF	3.3		6.88	9	nS
t <sub>PLH</sub>	Α	Υ	C <sub>L</sub> = 50pF	3.3		8.59	12.5	nS
t <sub>PLZ</sub>	OE	Υ	C <sub>L</sub> = 15pF	3.3		9.56	13	nS
t <sub>PLZ</sub>	OE	Υ	C <sub>L</sub> = 50pF	3.3		13.2	17	nS
t <sub>PZH</sub>	OE	Υ	C <sub>L</sub> = 15pF	3.3		11.1	13.8	nS
t <sub>PZH</sub>	OE	Υ	C <sub>L</sub> = 50pF	3.3		13	16	nS
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 15pF	3.3		11.2	14.0	nS
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 50pF	3.3		13.7	16.8	nS
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 15pF	5		4.73	6.5	nS
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 50pF	5		6.53	8.5	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 15pF	5		7.99	9.8	nS
t <sub>PHZ</sub>	OE	Υ	C <sub>L</sub> = 50pF	5		9.92	11.5	nS
t <sub>PLH</sub>	Α	Υ	C <sub>L</sub> = 15pF	5		4.64	6.5	nS
t <sub>PLH</sub>	Α	Υ	C <sub>L</sub> = 50pF	5		6	8.5	nS
t <sub>PLZ</sub>	OE	Y	C <sub>L</sub> = 15pF	5		7.01	9	nS
t <sub>PLZ</sub>	OE	Y	C <sub>L</sub> = 50pF	5		9.39	11	nS
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 15pF	5		7.79	9.5	nS
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 50pF	5		9.39	11.5	nS
t <sub>PZL</sub>	OE	Y	C <sub>L</sub> = 15pF	5		7.82	9.8	nS
	OE	Y	C <sub>L</sub> = 50pF	5		9.66	11.9	nS
t <sub>PZL</sub>	OE	1	OL - Joht	3		9.00	11.9	113



# **5.7 Typical Characteristics**

T<sub>A</sub> = 25°C (unless otherwise noted)





# 5.7 Typical Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise noted)

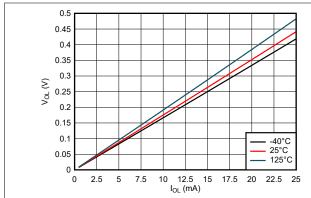


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

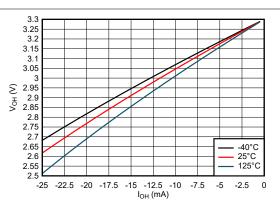


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

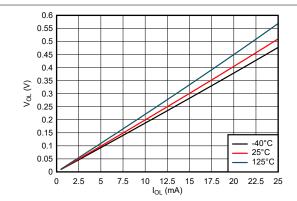


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

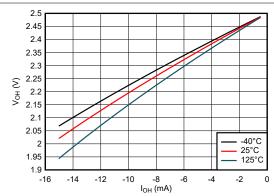


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

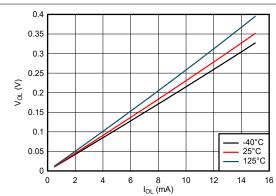


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

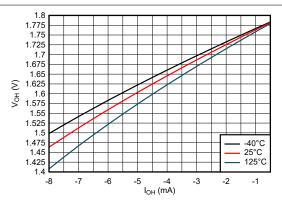
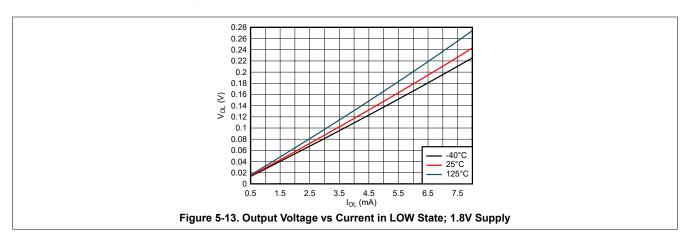


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply



# **5.7 Typical Characteristics (continued)**

T<sub>A</sub> = 25°C (unless otherwise noted)

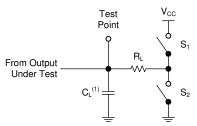


## **6 Parameter Measurement Information**

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1MHz,  $Z_O = 50\Omega$ ,  $t_t < 2.5$ ns.

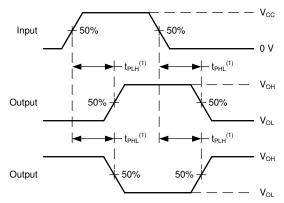
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R <sub>L</sub>	CL	ΔV	V <sub>cc</sub>
t <sub>PLH</sub> , t <sub>PHL</sub>	OPEN	OPEN	_	15pF, 50pF	_	ALL
t <sub>PLZ</sub> , t <sub>PZL</sub>	CLOSED	OPEN	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t <sub>PHZ</sub> , t <sub>PZH</sub>	OPEN	CLOSED	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t <sub>PLZ</sub> , t <sub>PZL</sub>	CLOSED	OPEN	1kΩ	15pF, 50pF	0.3V	> 2.5V
t <sub>PHZ</sub> , t <sub>PZH</sub>	OPEN	CLOSED	1kΩ	15pF, 50pF	0.3V	> 2.5V



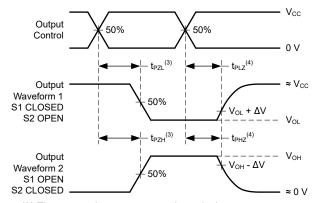
(1) C<sub>L</sub> includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



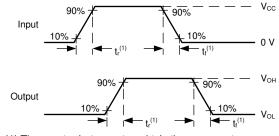
(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}.$ 

Figure 6-2. Voltage Waveforms Propagation Delays



- (3) The greater between  $t_{\mbox{\scriptsize PZL}}$  and  $t_{\mbox{\scriptsize PZH}}$  is the same as  $t_{\mbox{\scriptsize en}}$ .
- (4) The greater between  $t_{\mbox{\scriptsize PLZ}}$  and  $t_{\mbox{\scriptsize PHZ}}$  is the same as  $t_{\mbox{\scriptsize dis}}.$

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_f$ .

Figure 6-4. Voltage Waveforms, Input and Output Transition Times



# 7 Detailed Description

### 7.1 Overview

The SN74LV8T240-EP devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

# 7.2 Functional Block Diagram

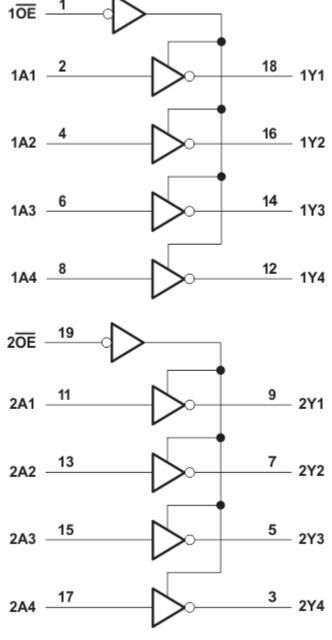


Figure 7-1. Logic Diagram (Positive Logic)



### 7.3 Feature Description

### 7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a  $10k\Omega$  resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.



### 7.3.2 LVxT Enhanced Input Voltage

The SN74LV8T240-EP belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified  $V_{IH(MIN)}$  level for a HIGH input state, and at or below the specified  $V_{IL(MAX)}$  for a LOW input state. Figure 7-2 shows the typical  $V_{IH}$  and  $V_{IL}$  levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the Electrical Characteristics. The worst case resistance is calculated with the maximum input voltage, given in the Absolute Maximum Ratings, and the maximum input leakage current, given in the Electrical Characteristics, using Ohm's law (R = V ÷ I).

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the Recommended Operating Conditions table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the Implications of Slow or Floating CMOS Inputs application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a  $10k\Omega$  resistor is recommended and will typically meet all requirements.

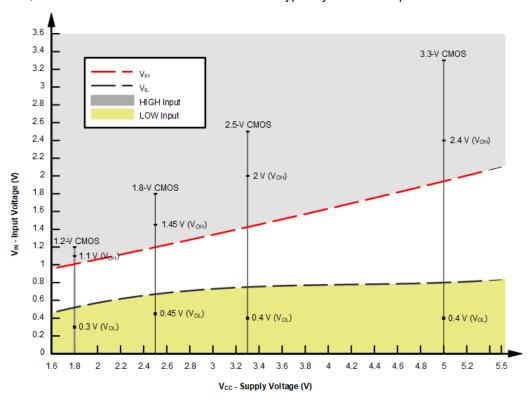


Figure 7-2. LVxT Input Voltage Levels



#### 7.3.2.1 Up Translation

Input signals can be up translated using the SN74LV8T240-EP. The voltage applied at V<sub>CC</sub> will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables. When connected to a high-impedance input, the output voltage will be approximately V<sub>CC</sub> in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a V<sub>IH(MIN)</sub> of 3.5V. For the SN74LV8T240-EP, VIH(MIN) with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

Ensure that the input signals in the HIGH state are above V<sub>IH(MIN)</sub> and input signals in the LOW state are lower than  $V_{IL(MAX)}$  as shown in Figure 7-3.

Up Translation Combinations are as follows:

- 1.8V V<sub>CC</sub> Inputs from 1.2V
- 2.5V V<sub>CC</sub> Inputs from 1.8V
- $3.3 \mbox{V}_{CC}$  Inputs from 1.8V and 2.5V  $5.0 \mbox{V}_{CC}$  Inputs from 2.5V and 3.3V

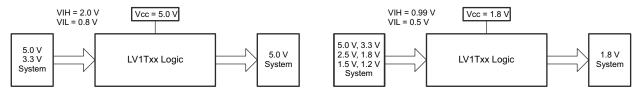


Figure 7-3. LVxT Up and Down Translation Example

#### 7.3.2.2 Down Translation

Signals can be translated down using the SN74LV8T240-EP. The voltage applied at the V<sub>CC</sub> will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables.

When connected to a high-impedance input, the output voltage will be approximately V<sub>CC</sub> in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between  $V_{IH(MIN)}$  and 5.5V, and input signals in the LOW state are lower than V<sub>IL(MAX)</sub> as shown in Figure 7-2.

For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V  $V_{CC}$ . See Figure 7-3.

Down Translation Combinations are as follows:

- 1.8V V<sub>CC</sub> Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V V<sub>CC</sub> Inputs from 3.3V and 5.0V
- $3.3V V_{CC}$  Inputs from 5.0V

#### 7.3.3 Clamp Diode Structure

As Figure 7-4 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

#### CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clampcurrent ratings are observed.

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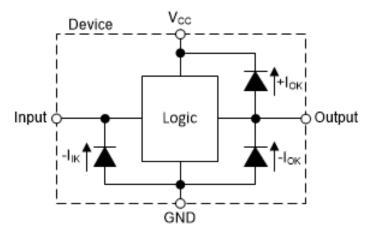


Figure 7-4. Electrical Placement of Clamping Diodes for Each Input and Output

# 7.4 Device Functional Modes

Table 7-1. Function Table (Each Buffer)

INPU	OUTPUT (2)	
ŌĒ	Α	Y
L	Н	L
L	L	Н
Н	Х	Z

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

# 8 Application and Implementation

#### **Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

# **8.1 Application Information**

The SN74LV8T240-EP can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

# 8.2 Typical Application

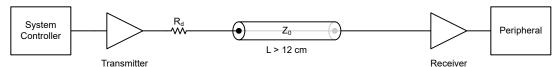


Figure 8-1. Typical Application Schematic



### 8.2.1 Design Requirements

### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV8T240-EP plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV8T240-EP plus the maximum supply current, I<sub>CC</sub>, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV8T240-EP can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV8T240-EP can drive a load with total resistance described by  $R_L \ge V_O$  /  $I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear* and Logic (SLL) Packages and Devices.

#### **CAUTION**

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.



#### 8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV8T240-EP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A  $10k\Omega$  resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V<sub>CC</sub> or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.



### 8.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V<sub>CC</sub> to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V<sub>CC</sub> and GND pins. An example layout is shown in the *Layout* section.
- Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will
  optimize performance. This can be accomplished by providing short, appropriately sized traces from the
  SN74LV8T240-EP to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

## 8.2.3 Application Curve

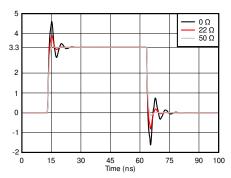


Figure 8-2. Switching Characteristics Comparison

#### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu F$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu F$  and  $1\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 8.4 Layout

### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - · Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - · Avoid branches; buffer signals that must branch separately



### 8.4.2 Layout Example

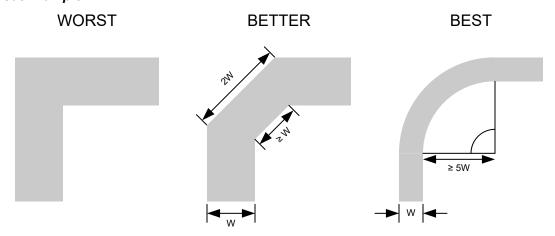


Figure 8-3. Example Trace Corners for Improved Signal Integrity

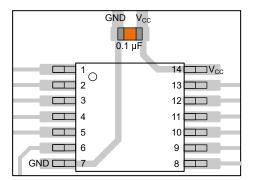


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

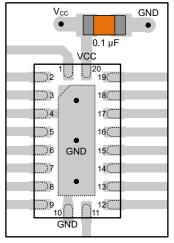


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

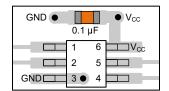


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

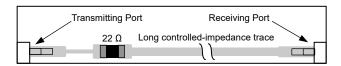


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity



# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application report

# 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

DATE	REVISION	NOTES
January 2025	*	Initial Release

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 7-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LV8T240MPWREP	Active	Production	TSSOP (PW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV240EP
SN74LV8T240MPWREP.A	Active	Production	TSSOP (PW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV240EP

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LV8T240-EP:

Catalog: SN74LV8T240

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# PACKAGE OPTION ADDENDUM

www.ti.com 7-Nov-2025

• Automotive : SN74LV8T240-Q1

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 15-Feb-2025

# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8T240MPWREP	TSSOP	PW	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

www.ti.com 15-Feb-2025



### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8T240MPWREP	TSSOP	PW	20	3000	353.0	353.0	32.0



SMALL OUTLINE PACKAGE



### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025