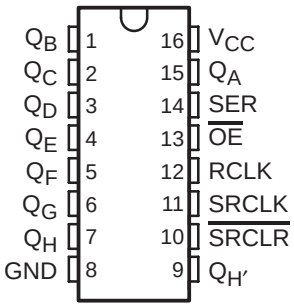
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 7.4 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Supports Mixed-Mode Voltage Operation on All Ports**
- **8-Bit Serial-In, Parallel-Out Shift**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Shift Register Has Direct Clear**

PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74LV595A is an 8-bit shift register designed for 2-V to 5.5-V V_{CC} operation.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs except $Q_{H'}$ are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Reel of 2000	SN74LV595AIPWREP	LV595EP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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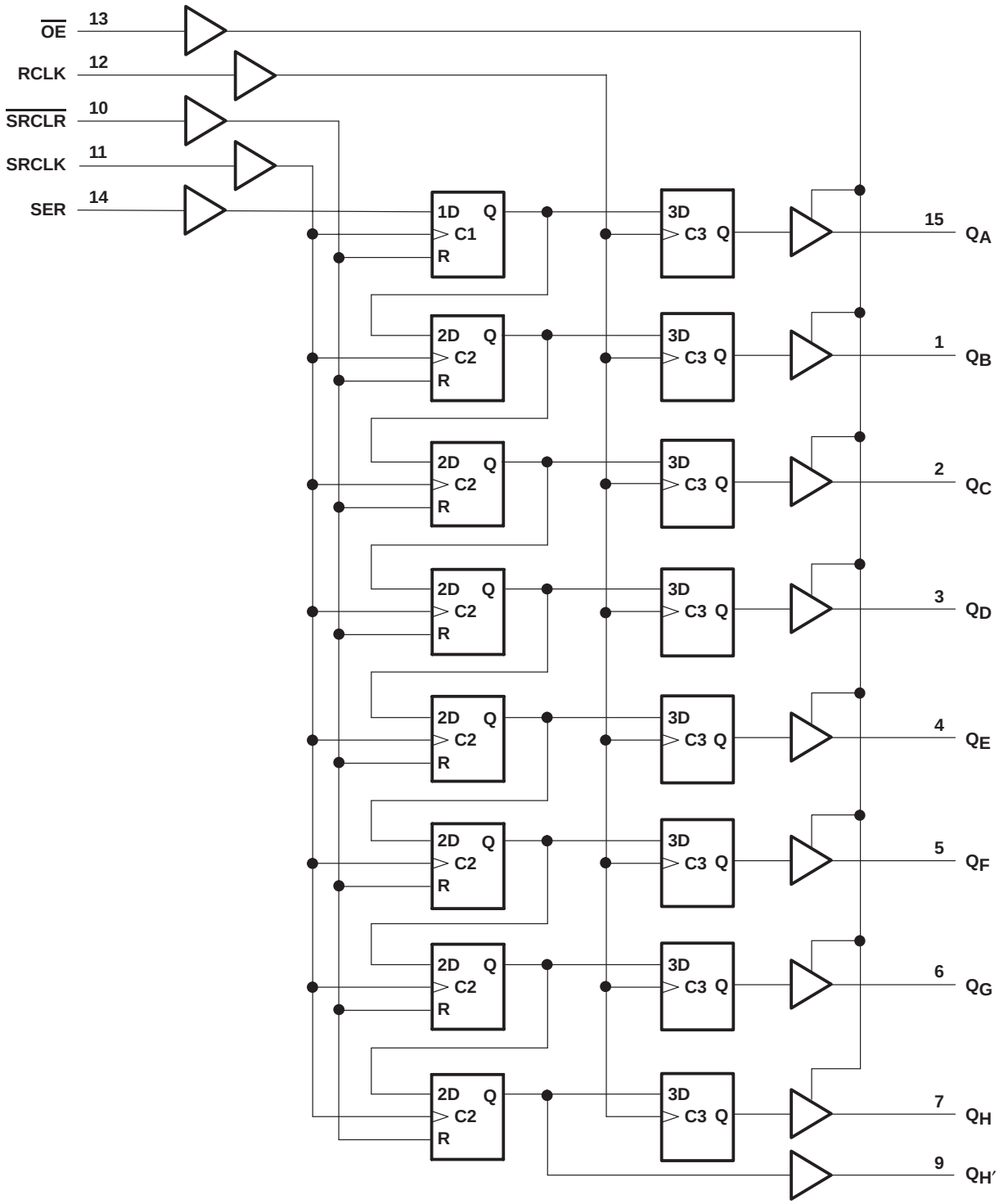
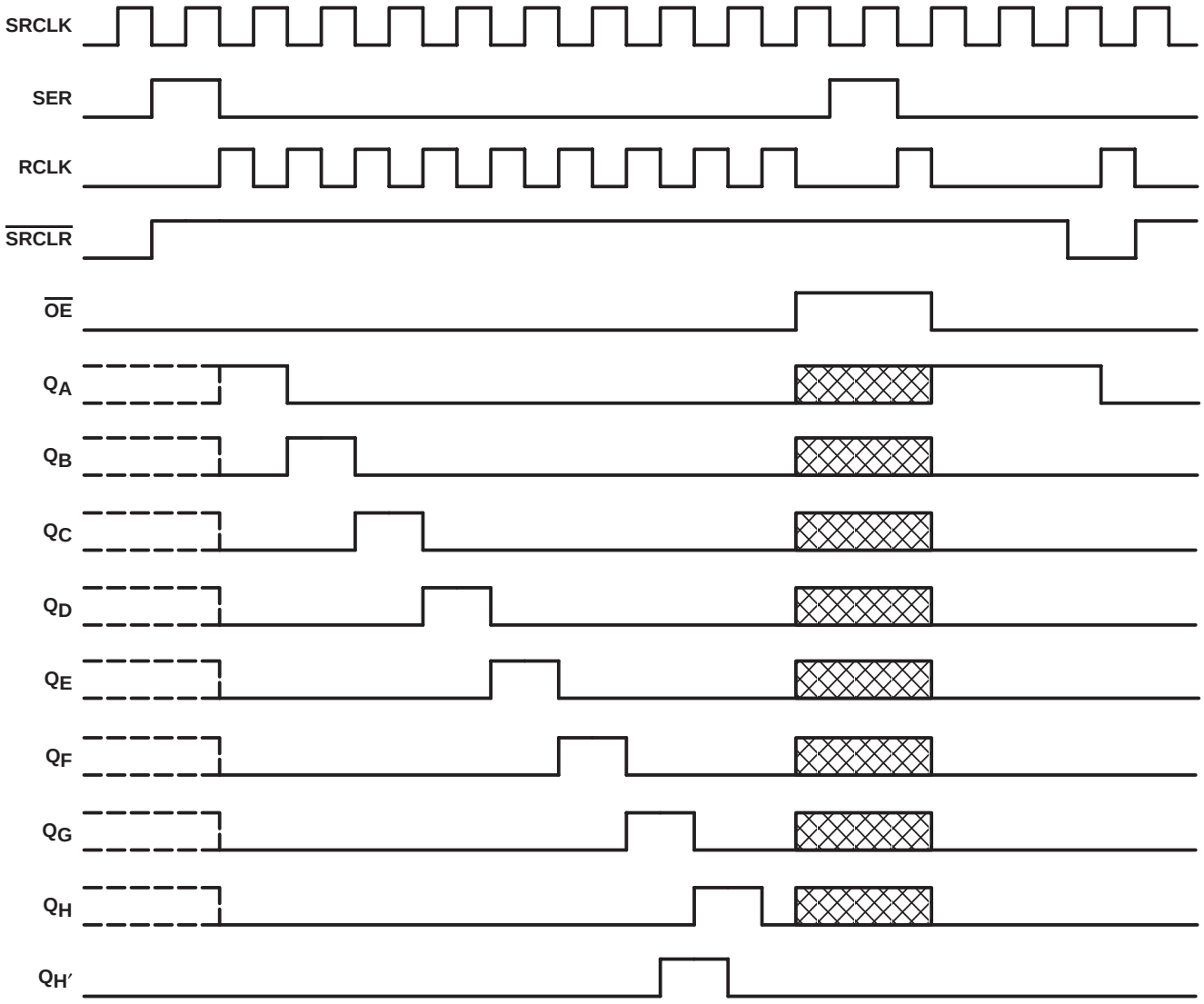
FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A–Q_H are disabled.
X	X	X	X	L	Outputs Q_A–Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	↓	H	X	X	Shift-register state is not changed.
X	X	X	↑	X	Shift-register data is stored in the storage register.
X	X	X	↓	X	Storage-register state is not changed.

logic diagram (positive logic)



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 2.3 V to 2.7 V		−2	mA
		V_{CC} = 3 V to 3.6 V		−8	
		V_{CC} = 4.5 V to 5.5 V		−16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = −50 μA		2 V to 5.5 V	V_{CC}−0.1			V
		I_{OH} = −2 mA		2.3 V	2			
	$Q_{H'}$	I_{OH} = −6 mA		3 V	2.48			
	Q_A−Q_H	I_{OH} = −8 mA			2.48			
	$Q_{H'}$	I_{OH} = −12 mA		4.5 V	3.8			
	Q_A−Q_H	I_{OH} = −16 mA			3.8			
V_{OL}		I_{OL} = 50 μA		2 V to 5.5 V			0.1	V
		I_{OL} = 2 mA		2.3 V			0.4	
	$Q_{H'}$	I_{OL} = 6 mA		3 V			0.44	
	Q_A−Q_H	I_{OL} = 8 mA					0.44	
	$Q_{H'}$	I_{OL} = 12 mA		4.5 V			0.55	
	Q_A−Q_H	I_{OL} = 16 mA					0.55	
I_I		V_I = 5.5 V or GND		0 to 5.5 V			±1	μA
I_{OZ}		V_O = V_{CC} or GND		5.5 V			±5	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	5.5 V			20	μA
I_{off}		V_I or V_O = 0 to 5.5 V		0			5	μA
C_i		V_I = V_{CC} or GND		3.3 V		3.5		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	SRCLK high or low	7		7.5		ns
		RCLK high or low	7		7.5		
		$\overline{\text{SRCLR}}$ low	6		6.5		
t_{su}	Setup time	SER before SRCLK↑	5.5		5.5		ns
		SRCLK↑ before RCLK↑†	8		9		
		$\overline{\text{SRCLR}}$ low before RCLK↑	8.5		9.5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	4		4		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	SRCLK high or low	5.5		5.5		ns
		RCLK high or low	5.5		5.5		
		$\overline{\text{SRCLR}}$ low	5		5		
t_{su}	Setup time	SER before SRCLK↑	3.5		3.5		ns
		SRCLK↑ before RCLK↑†	8		8.5		
		$\overline{\text{SRCLR}}$ low before RCLK↑	8		9		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	3		3		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	SRCLK high or low	5		5		ns
		RCLK high or low	5		5		
		$\overline{\text{SRCLR}}$ low	5.2		5.2		
t_{su}	Setup time	SER before SRCLK↑	3		3		ns
		SRCLK↑ before RCLK↑†	5		5		
		$\overline{\text{SRCLR}}$ low before RCLK↑	5		5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2.5		2.5		
t_h	Hold time	SER after SRCLK↑	2		2		ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	65	80		45		MHz
			C_L = 50 pF	60	70		40		
t_{PLH}	RCLK	Q_A–Q_H	C_L = 15 pF		8.4	14.2	1	15.8	ns
t_{PHL}					8.4	14.2	1	15.8	
t_{PLH}	SRCLK	$Q_{H'}$			9.4	19.6	1	22.2	
t_{PHL}					9.4	19.6	1	22.2	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			8.7	14.6	1	16.3	
t_{PZH}	$\overline{OE}$	Q_A–Q_H			8.2	13.9	1	15	
t_{PZL}					10.9	18.1	1	20.3	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H			8.3	13.7	1	15.6	
t_{PLZ}					9.2	15.2	1	16.7	
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		11.2	17.2	1	19.3	ns
t_{PHL}					11.2	17.2	1	19.3	
t_{PLH}	SRCLK	$Q_{H'}$			13.1	22.5	1	25.5	
t_{PHL}					13.1	22.5	1	25.5	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			12.4	18.8	1	21.1	
t_{PZH}	$\overline{OE}$	Q_A–Q_H			10.8	17	1	18.3	
t_{PZL}					13.4	21	1	23	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H			12.2	18.3	1	19.5	
t_{PLZ}					14	20.9	1	22.6	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	120		70		MHz
			C_L = 50 pF	55	105		50		
t_{PLH}	RCLK	Q_A–Q_H	C_L = 15 pF		6	11.9	1	13.5	ns
t_{PHL}					6	11.9	1	13.5	
t_{PLH}	SRCLK	$Q_{H'}$			6.6	13	1	15	
t_{PHL}					6.6	13	1	15	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			6.2	12.8	1	13.7	
t_{PZH}	$\overline{OE}$	Q_A–Q_H			6	11.5	1	13.5	
t_{PZL}					7.8	11.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H			6.1	14.7	1	15.2	
t_{PLZ}					6.3	14.7	1	15.2	
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		7.9	15.4	1	17	ns
t_{PHL}					7.9	15.4	1	17	
t_{PLH}	SRCLK	$Q_{H'}$			9.2	16.5	1	18.5	
t_{PHL}					9.2	16.5	1	18.5	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			9	16.3	1	17.2	
t_{PZH}	$\overline{OE}$	Q_A–Q_H			7.8	15	1	17	
t_{PZL}					9.6	15	1	17	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H			8.1	15.7	1	16.2	
t_{PLZ}					9.3	15.7	1	16.2	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	135	170		115		MHz
			C_L = 50 pF	120	140		95		
t_{PLH}	RCLK	Q_A–Q_H	C_L = 15 pF		4.3	7.4	1	8.5	ns
t_{PHL}					4.3	7.4	1	8.5	
t_{PLH}	SRCLK	$Q_{H'}$			4.5	8.2	1	9.4	
t_{PHL}					4.5	8.2	1	9.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			4.5	8	1	9.1	
t_{PZH}	$\overline{OE}$	Q_A–Q_H			4.3	8.6	1	10	
t_{PZL}					5.4	8.6	1	10	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H			2.4	6	1	7.1	
t_{PLZ}					2.7	5.1	1	7.2	
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		5.6	9.4	1	10.5	ns
t_{PHL}					5.6	9.4	1	10.5	
t_{PLH}	SRCLK	$Q_{H'}$			6.4	10.2	1	11.4	
t_{PHL}					6.4	10.2	1	11.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			6.4	10	1	11.1	
t_{PZH}	$\overline{OE}$	Q_A–Q_H			5.7	10.6	1	12	
t_{PZL}					6.8	10.6	1	12	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H			3.5	10.3	1	11	
t_{PLZ}					3.4	10.3	1	11	

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

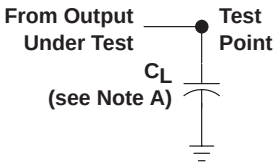
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

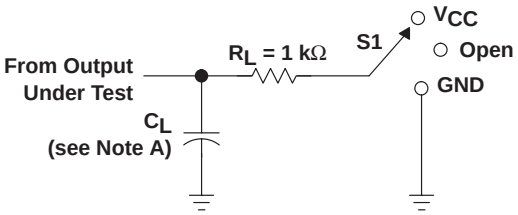
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	111	pF
			5 V	114	

PARAMETER MEASUREMENT INFORMATION

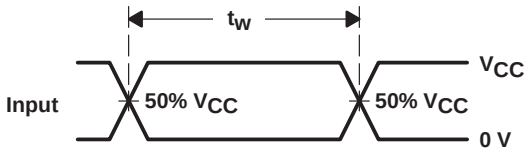


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

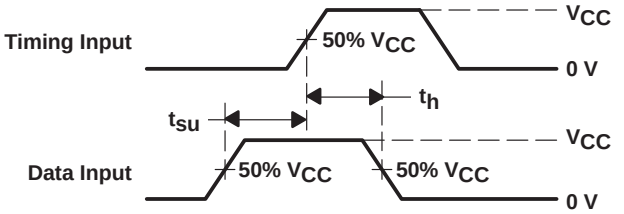


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

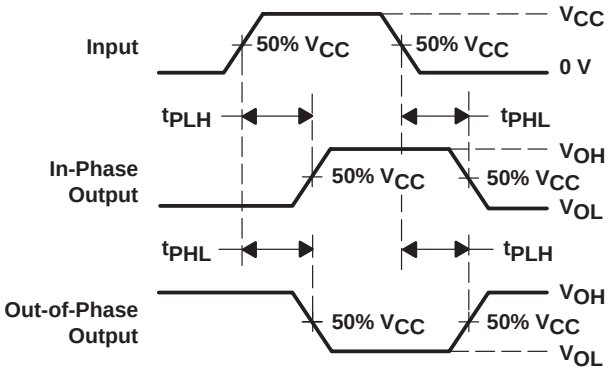
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



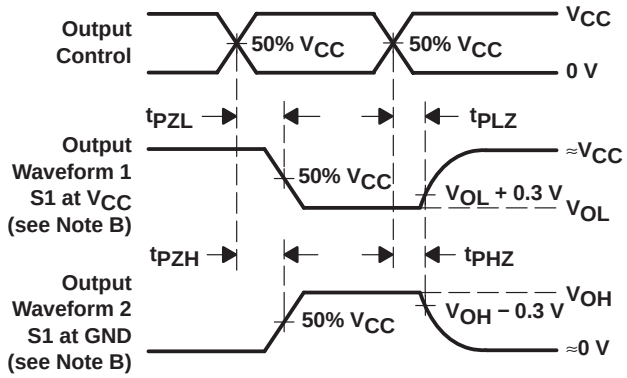
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV595AIPWREP	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	LV595EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV595A-EP :

- Catalog : SN74LV595A
- Automotive : SN74LV595A-Q1

NOTE: Qualified Version Definitions:

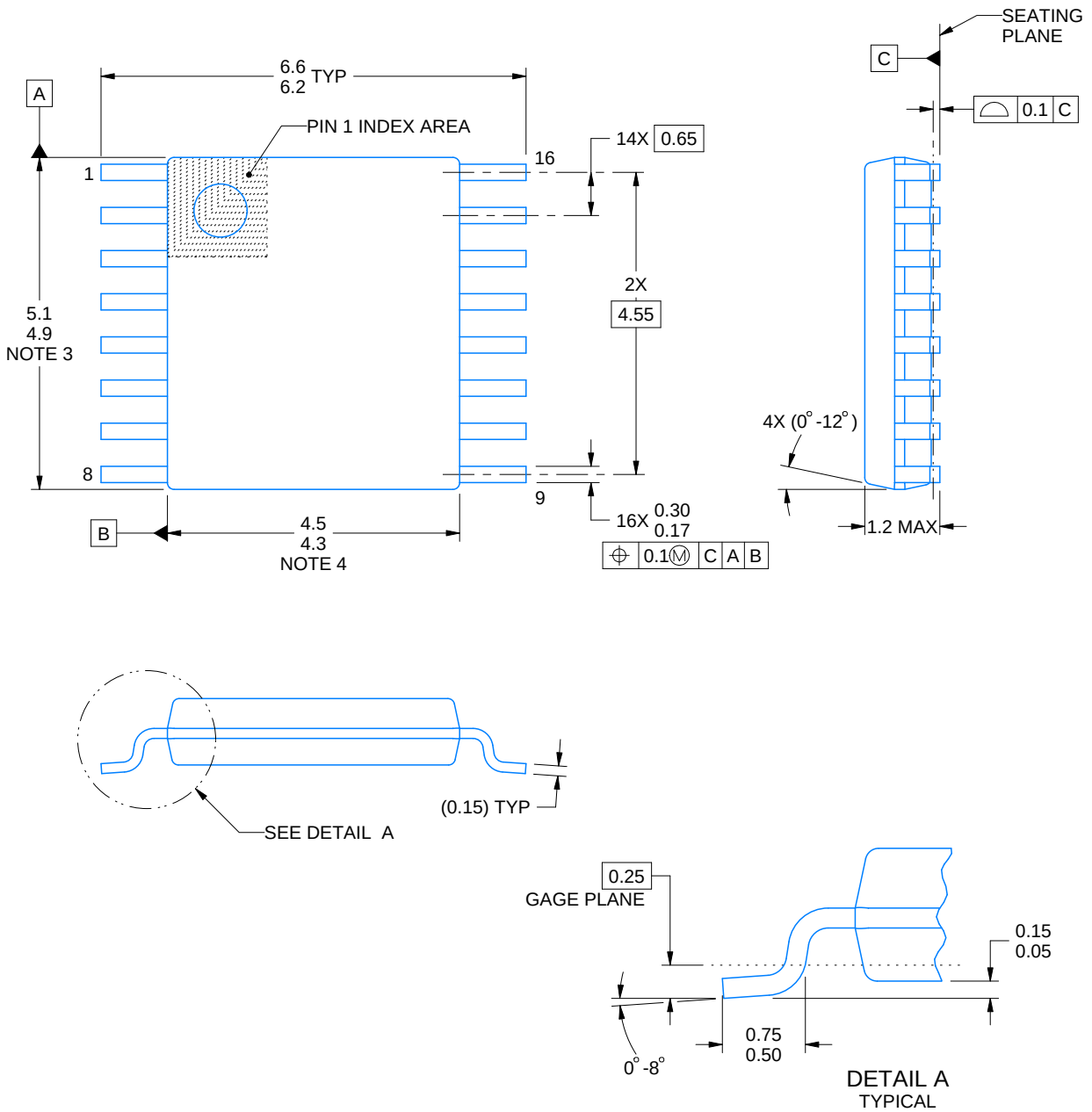
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

PW0016A

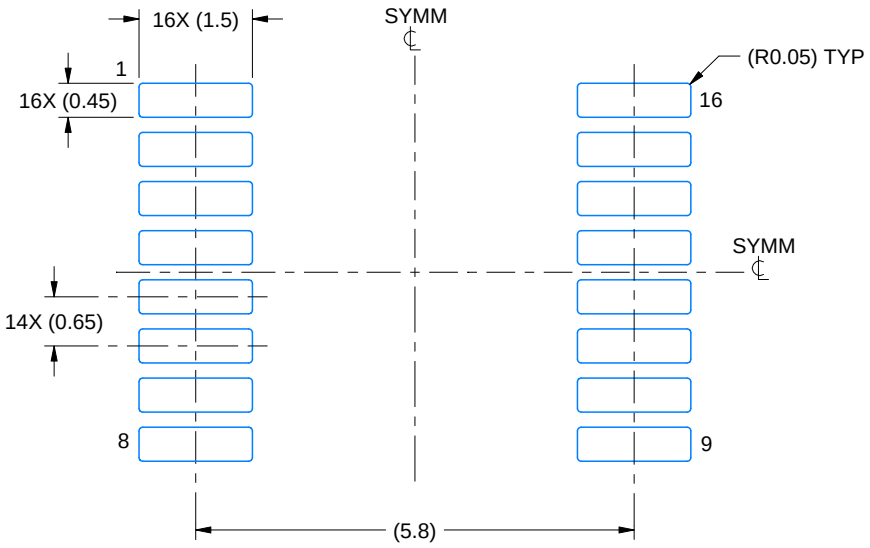
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

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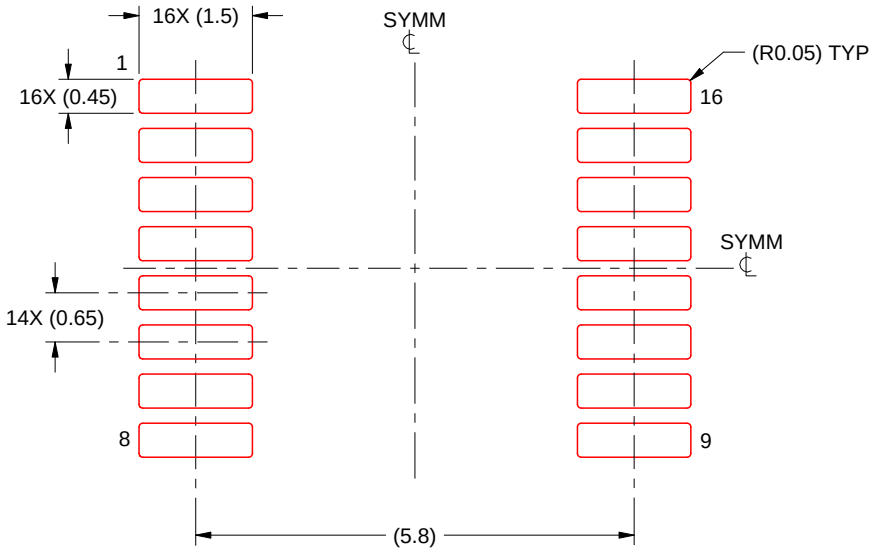
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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