









SN74LV573A SCLS411J - APRIL 1998 - REVISED MARCH 2023

SN74LV573A Octal Transparent D-Type Latches With 3-State Outputs

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Max t_{pd} of 8 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) latch-up performance exceeds 250 mA per <0.8 V at V_{CC} = 3.3 V, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Support mixed-mode voltage operation on all ports
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD

2 Applications

- **Buffer Registers**
- **Bidirectional Bus Drivers**
- Working Registers

To seven other channels

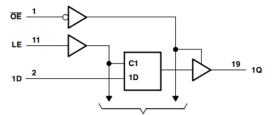
3 Description

The 'LV573A devices are octal transparent D-type latches designed for 2 V to 5.5 V V_{CC} operation.

Package Information(1)

• •	aonago iiiioiiiiaa	•
PART NUMBER	PACKAGE	BODY SIZE (NOM)
	NS (SO, 20)	12.6 mm × 5.3 mm
	DW (SOIC, 20)	12.8 mm × 7.5 mm
SN74LV573A	DB (SSOP, 20)	7.2 mm × 5.3 mm
SINTALVOTOA	PW (TSSOP, 20)	6.5 mm × 4.4 mm
	DGV (TVSOP, 20)	5 mm × 4.4 mm
	RGY (VQFN, 20)	4.5 mm × 3.5 mm

For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

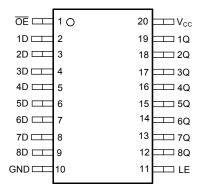
Changes from Revision I (April 2005) to Revision J (March 2023)

Page

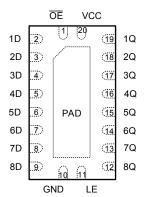
- Added Applications, Package Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.
- Updated thermal values for PW package from RθJA = 131.8 to 128.2, all values in °C/W.......



5 Pin Configuration and Functions







RGY Package Top View

Table 5-1. Pin Functions

	PIN		Table 3-1.1 III I unctions
NO.	NAME	I/O ¹	DESCRIPTION
1	ŌĒ	I	Output enable
2	1D	I	1D input
3	2D	I	2D input
4	3D	I	3D input
5	4D	I	4D input
6	5D	I	5D input
7	6D	I	6D input
8	7D	I	7D input
9	8D	I	8D input
10	GND	_	Ground
11	LE	I	Latch enable input
12	8Q	0	8Q output
13	7Q	0	7Q output
14	6Q	0	6Q output
15	5Q	0	5Q output
16	4Q	0	4Q output
17	3Q	0	3Q output
18	2Q	0	2Q output
19	1Q	0	1Q output
20	V _{CC}	_	Power pin

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		·	MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
VI	Input voltage ⁽¹⁾		-0.5	7	V
Vo	Voltage range applied to any output in the high-impedance or power-off state ⁽¹⁾		-0.5	7	V
Vo	Output voltage range applied in the high or low state ⁽¹⁾ (2)		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0		-50	mA
Io	Continuous output current	$V_{O} = 0$ to V_{CC}		±35	mA
	Continuous current through V _{CC} or GND			±70	mA
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human-Body Model (A114-A) ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged-Device Model (C101) ⁽²⁾	±1000	V
		Machine Model (A115-A)	±200	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		2	5.5	V	
		V _{CC} = 2 V	1.5			
	High level input voltage	V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V	
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7			
		V _{CC} = 2 V		0.5		
,,	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	.,	
V _{IL}		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	V	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		
VI	Input voltage	<u> </u>	0	5.5	V	
.,	Outrost valle as	High or low state	0	V _{CC}	V	
Vo	Output voltage	3-state	0	5.5	V	
		V _{CC} = 2 V		- 50		
	Library Lavid and an arrange	V _{CC} = 2.3 V to 2.7 V		- 2		
I _{OH}	High-level output current	V _{CC} = 3 V to 3.6 V		- 8	ns	
		V _{CC} = 4.5 V to 5.5 V		- 16		

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⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

over operating free-air temperature range (unless otherwise noted)(1)

		·	MIN	MAX	UNIT
		V _{CC} = 2 V		50	
	Law level cutout current	V _{CC} = 2.3 V to 2.7 V		2	no
I _{OL} Low-le	Low-level output current	V _{CC} = 3 V to 3.6 V		8	ns
	\	V _{CC} = 4.5 V to 5.5 V		16	
		V _{CC} = 2.3 V to 2.7 V		200	
Δt/Δν	Input transition rise or fall rate	V _{CC} = 3 V to 3.6 V		100	ns
	V _{CC} = 4.5 V to 5.5 V			20	
T _A	Operating free-air temperature		- 40	85	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report (SCBA004).

6.4 Thermal Information

			SN74LV573A					
		DGV (TVSOP)	DW (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	UNIT
THERMAL METRIC		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	92	109.1	122.7	84.6	128.2	37	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the <u>Semiconductor and IC Package Thermal Metrics</u> application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
V	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1				
	I _{OH} = −2 mA	2.3 V	2			V	
V _{OH}	$I_{OH} = -8 \text{ mA}$	3 V	2.48			V	
	I _{OH} = −16 mA	4.5 V	3.8				
	I _{OL} = 50 μA	2 V to 5.5 V			0.1		
	I _{OL} = 2 mA	2.3 V			0.4	V	
V _{OL}	I _{OL} = 8 mA	3 V			0.44	V	
	I _{OL} = 16 mA	4.5 V			0.55		
II	V _I = 5.5 V or GND	0 to 5.5 V			± 1	μΑ	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±5	μA	
Icc	$V_1 = V_{CC}$ or $I_O = 0$	5.5 V			20	μΑ	
I _{off}	V _I or V _O = 0 to 5.5 V	0			5	μA	
Ci	V _I = V _{CC} or GND	3.3 V		1.8		pF	



6.6 Timing Requirements, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T _A = 25°C MIN MAX		UNIT
	PARAIVIETER	TEST CONDITIONS	MIN MAX	IVIIN IVIAA	UNII
t _w	Pulse duration	LE high	5	5	ns
t _{su}	Setup time	Data before LE↓	3.5	3.5	ns
t _h	Hold time	Data after LE↓	1.5	1.5	ns

6.7 Timing Requirements, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T _A = 25°C		MINI	MINI MAY	
PARAINETER		TEST CONDITIONS	MIN			MIN MAX	
t _w	Pulse duration	LE high	5		5		ns
t _{su}	Setup time	Data before LE↓	3.5		3.5		ns
t _h	Hold time	Data after LE↓	1.5		1.5		ns

6.8 Timing Requirements, V_{CC} =5 V ± 0.5 V

over operating free-air temperature range, V_{CC} = 5 V ± 0.5 V(unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T _A = 25°C	MIN MAX	UNIT
	PARAIVIETER	TEST CONDITIONS	MIN MAX	IVIIN IVIAA	UNIT
t _w	Pulse duration	LE high	5	5	ns
t _{su}	Setup time	Data before LE↓	3.5	3.5	ns
t _h	Hold time	Data after LE↓	1.5	1.5	ns

Product Folder Links: SN74LV573A

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6.9 Switching Characteristics, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	то	LOAD	TA	= 25°C		SN74LV	573A	UNIT
PARAMETER	PROW (INFOT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNII
t _{pd}	D	Q			8.9 ¹	15.8 ¹	1	18	
t _{pd}	LE	Q	C _L = 15 pF		9.6 <mark>1</mark>	16.2 ¹	1	19	no
t _{en}	ŌĒ	Q			9.3 ¹	16.2 ¹	1	19	ns
t _{dis}	ŌĒ	Q			6.7 ¹	12.6 ¹	1	15	
t _{pd}	D	Q			10.9	18.7	1	21	
t _{pd}	LE	Q			11.6	19.1	1	23	ns
t _{en}	ŌĒ	Q	C _L = 50 pF		11.4	19	1	22	
t _{dis}	ŌĒ	Q			8.6	17.3	1	19	
t _{sk(o)}						2		2	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM TO		LOAD CAPACITANCE		T _A = 25°C		SN74LV	UNIT	
PARAMETER	(INPUT)	(INPUT) (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNII
t _{pd}	D	Q			6.2 ¹	11 ¹	1	13	
t _{pd}	LE	Q	C _L = 15 pF		6.8 ¹	11.9 ¹	1	14	
t _{en}	ŌĒ	Q			6.6 ¹	11.5 ¹	1	13.5	ns
t _{dis}	ŌĒ	Q			4.9 ¹	11 ¹	1	13	
t _{pd}	D	Q			7.7	14.5	1	16.5	
t _{pd}	LE	Q			8.2	15.4	1	17.5	
t _{en}	ŌĒ	Q	C _L = 50 pF		8	15	1	17	ns
t _{dis}	ŌĒ	Q			6.2	14.5	1	16.5	
t _{sk(o)}						1.5		1.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.



6.11 Switching Characteristics, 5 V ± 0.5 V

over operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	LOAD CAPACITANCE	T,		SN74LV	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNII
t _{pd}	D	Q			4.3 ¹	6.8 ¹	1	8	
t _{pd}	LE	Q	C _L = 15 pF		4.7 ¹	7.7 ¹	1	9	no
t _{en}	ŌĒ	Q			4.7 ¹	7.7 ¹	1	9	ns
t _{dis}	ŌĒ	Q			3.5 ¹	7.7 ¹	1	9	
t _{pd}	D	Q			5.3	8.8	1	10	
t _{pd}	LE	Q			5.7	9.7	1	11	
t _{en}	ŌĒ	Q	C _L = 50 pF		5.7	9.7	1	11	ns
t _{dis}	ŌĒ	Q			4.2	9.7	1	11	
t _{sk(o)}						1		1	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.12 Noise Characteristics

 V_{CC} = 3.3 V, C_{L} = 50 pF, T_{A} = 25°C

	PARAMETER	SN74LV573A					
	PARAMETER	MIN	TYP	MAX	UNIT		
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.6	0.8	V		
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		- 0.5	-0.8	V		
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		2.9		V		
V _{IH(D)}	High-level dynamic input voltage	2.31			V		
V _{IL(D)}	Low-level dynamic input voltage			0.99	V		

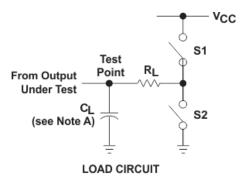
6.13 Operating Characteristics

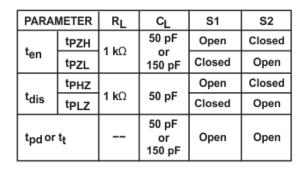
T_A = 25°C

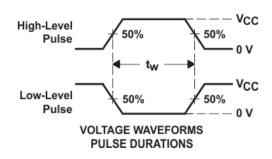
1A - Z	3 0							
	PARAMETER	TEST (CONDITIONS	V _{CC}	TYP	UNIT		
C. Davis dissination considers					3.3 V	16		
	Dower dissinction consistence	Outputs enabled	D to Q	C = 50 pF	f = 10 MH=	5 V	18	
Cpd	C _{pd} Power dissipation capacitance			$C_L = 50 \text{ pF},$	f = 10 MHz	3.3 V	18.2	pF
			LE to Q	1		5 V	21.3	

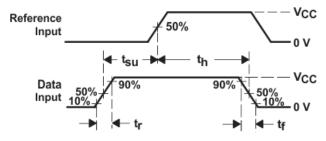


7 Parameter Measurement Information

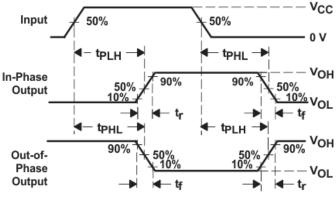


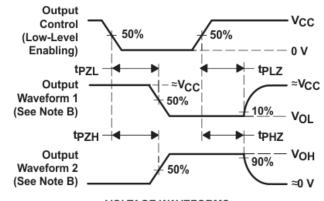






VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES





VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The 'LV573A devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram

To seven other channels

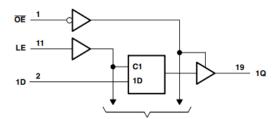


Figure 8-1. Logic Diagram (Positive Logic)



8.3 Device Functional Modes

Table 8-1 lists the functional modes of the SN74LV573A.

Table 8-1. Function Table (Each Latch)

	INPUTS		OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q ₀
Н	Х	Х	Z

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 6.3 table. The total current through Ground or V_{CC} must not exceed ± 70 mA as per Section 6.1 table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1- μ F capacitor; if there are multiple V_{CC} pins, then TI recommends 0.01- μ F or 0.022- μ F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- μ F and 1- μ F capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Layout Diagram specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

9.2.1.1 Layout Example

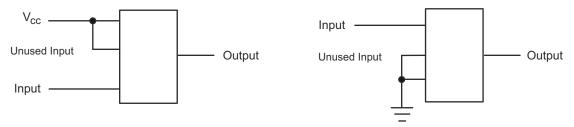


Figure 9-1. Layout Diagram

Submit Document Feedback



10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV573A	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LV573ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADBRG4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	LV573A
SN74LV573ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV573A
SN74LV573ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV573A
SN74LV573APW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	LV573A
SN74LV573APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ARGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A
SN74LV573ARGYR.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A
SN74LV573ARGYRG4	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV573ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV573ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV573ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV573ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV573APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV573ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV573ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV573ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LV573ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV573ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV573APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV573ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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