









SN74LV374A

SCLS408L - MAY 1998 - REVISED MARCH 2023

SN74LV374A Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Maximum t_{pd} of 9.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Support Mixed-Mode Voltage Operation on All
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-up Performance Exceeds 250 mA Per JESD

2 Applications

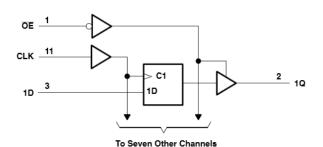
- Programmable Logic Controller (PLC)
- DCS and PAC: Analog Input Module
- Trains, Trams, and Subway Carriages
- **AC Inverter Drives**
- **Printers**

3 Description

The SN74LV374A devices are octal edge-triggered Dtype flip-flops designed for 2 V to 5.5 V V_{CC} operation.

Package Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)				
	DB (SSOP, 20)	7.20 mm × 5.30 mm				
SN74LV374A	DW (SOIC, 20)	12.80 mm × 7.50 mm				
SIN/4LV3/4A	NS (SO, 20)	12.60 mm × 5.30 mm				
	PW (TSSOP, 20)	6.50 mm × 4.40 mm				



Pin numbers shown are for the DB, DW, NS, PW, and RGY packages

Logic Diagram (Positive Logic)



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4 Revision History NOTE: Page numbers for previous revisions may differ	from page numbers in the current version.
Changes from Revision K (December 2022) to Revis	
 Updated structural layout of document and format or 	f tables
 Updated thermal values for DW package from RθJA 	a = 79.2 to 102.3, RθJC(top) = 43.7 to 69.9, RθJB = 47 to ues in °C/W

Changes from Revision J (March 2015) to Revision K (December 2022)

Changes from Revision I (March 2015) to Revision J (October 2016)

Changes from Revision H (April 2005) to Revision I (March 2015)

Page

Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device
Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout
section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information
section

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5 Pin Configuration and Functions

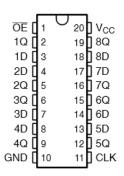


Figure 5-1. DB, DW, NS, or PW Package 20-PIN SSOP, SOIC, SO, or TSSOP (Top View)

Table 5-1. Pin Functions

	PIN	TVDE	DESCRIPTION
NAME	NO.	TYPE	DESCRIPTION
ŌĒ	1	I	Enable pin
1Q	2	0	Output 1
1D	3	I	Input 1
2D	4	I	Input 2
2Q	5	0	Output 2
3Q	6	0	Output 3
3D	7	I	Input 3
4D	8	I	Input 4
4Q	9	0	Output 4
GND	10	_	Ground pin
CLK	11	I	Clock pin
5Q	12	0	Output 5
5D	13	I	Input 5
6D	14	I	Input 6
6Q	15	0	Output 6
7Q	16	0	Output 7
7D	17	I	Input 7
8D	18	I	Input 8
8Q	19	0	Output 8
V _{CC}	20	_	Power pin



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
VI	Input voltage ⁽²⁾		-0.5	7	V
Vo	Voltage applied to any output in	n the high-impedance or power-off state ⁽²⁾	-0.5	7	V
Vo	Output voltage ⁽²⁾ (3)		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)		-20	mA
I _{OK}	Output clamp current	(V _O < 0)		-50	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±35	mA
	Continuous current through V _C	_C or GND		±70	mA
T _J	Junction temperature	nction temperature			
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V
		Machine Model (A115-A)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ This value is limited to 5.5 V maximum.



6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			SN74LV3	74A	UNIT	
			MIN	MAX	UNII	
V _{CC}	Supply voltage		2	5.5	V	
		V _{CC} = 2 V	1.5			
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V	
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.77			
		V _{CC} = 2 V		0.5		
.,	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	V	
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		
V _I	Input voltage	,	0	5.5	V	
.,	Output voltage	High or low state	0	V _{CC}	V	
Vo	Output voltage	3-state	0	5.5	V	
		V _{CC} = 2 V		-50	μA	
1	High level output ourrent	V _{CC} = 2.3 V to 2.7 V		-2		
l _{OH}	High-level output current	V _{CC} = 3 V to 3.6 V		-8	mA	
		V _{CC} = 4.5 V to 5.5 V		-16		
		V _{CC} = 2 V		50	μA	
	I am land autom and	V _{CC} = 2.3 V to 2.7 V		2		
l _{OL}	Low-level output current	V _{CC} = 3 V to 3.6 V		8	mA	
	$V_{CC} = 3$	V _{CC} = 4.5 V to 5.5 V		16		
		V _{CC} = 2.3 V to 2.7 V		200		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3 V to 3.6 V		100	ns/V	
		V _{CC} = 4.5 V to 5.5 V		20		
T _A	Operating free-air temperature		-40	125	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

			SN74LV374A							
	THERMAL METRIC ⁽¹⁾	DB (SSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)	UNIT				
			20 PINS	20 PINS	20 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.5	102.3	76.7	102.4	°C/W				
R _{0JC(top)}	Junction-to-case (top) thermal resistance	56.4	69.9	43.2	36.5	°C/W				
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	70.8	44.2	53.6	°C/W				
ΨЈТ	Junction-to-top characterization parameter	18.5	46.4	16.8	2.4	°C/W				
ΨЈВ	Junction-to-board characterization parameter	49.3	70.4	43.8	52.9	°C/W				
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W				

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}		LV374A to +85°C	SN -40°0	UNIT		
			MIN	TYP MAX	MIN	TYP	MAX	
	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1		V _{CC} -0.1			
V _{OH}	I _{OH} = −2 mA	2.3 V	2		2	'		V
	I _{OH} = -8 mA	3 V	2.48		2.48			V
	I _{OH} = -16 mA	4.5 V	3.8		3.8			
	I _{OL} = 50 μA	2 V to 5.5 V		0.1			0.1	
\	I _{OL} = 2 mA	2.3 V		0.4			0.4	V
V _{OL}	I _{OL} = 8 mA	3 V		0.44			0.44	V
	I _{OL} = 16 mA	4.5 V		0.55			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1			±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±5			±5	μA
I _{CC}	V _I = V _{CC} or GND , I _O = 0	5.5 V		20			20	μA
I _{off}	$V_1 \text{ or } V_0 = 0 \text{ to } 5.5 \text{ V}$	0		5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		2.9		2.9		pF

6.6 Switching Characteristics, V_{CC} = 2.5 V \pm 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM TO (INPUT) (OUTPUT)		LOAD CAPACITANCE	T _A = 25°C			SN74LV374A -40°C to +85°C		SN74LV374A -40°C to +125°C		UNIT
	(INFOT) (OOTE	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
•			C _L = 15 pF	60 ⁽¹⁾	105 ⁽¹⁾		50		50		MHz
f _{max}			C _L = 50 pF	50	85		40		40		IVITZ
t _{pd}	CLK	Q			9.7(1)	16.3 ⁽¹⁾	1	19	1	20.5	
t _{en}	ŌĒ	Q	$C_L = 15 pF$		8.9(1)	15.9 ⁽¹⁾	1	19	1	20.5	ns
t _{dis}	ŌĒ	Q			6.3 ⁽¹⁾	12.6 ⁽¹⁾	1	15	1	16.5	
t _{pd}	CLK	Q			11.8	19.3	1	23	1	24.5	
t _{en}	ŌĒ	Q	0 - 50 - 5		10.9	18.8	1	22	1	23.5	
t _{dis}	ŌĒ	Q	C _L = 50 pF		8.2	17.3	1	19	1	20.5	ns
t _{sk(o)}						2		2			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)			T _A = 25°C			SN74LV374A -40°C to +85°C		SN74LV374A -40°C to +125°C		UNIT	
	(111 01)	(OUTFUT)	CAFACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f			C _L = 15 pF	80 ⁽¹⁾	150 ⁽¹⁾		70		70		MHz	
f _{max}			C _L = 50 pF	55	110		50		50			
t _{pd}	CLK	Q			6.8 ⁽¹⁾	12.7 ⁽¹⁾	1	15	1	16		
t _{en}	ŌĒ	Q	C _L = 15 pF		6.3 ⁽¹⁾	11 ⁽¹⁾	1	13	1	14	ns	
t _{dis}	ŌĒ	Q			4.7(1)	10.5 ⁽¹⁾	1	12.5	1	13.5		
t _{pd}	CLK	Q			8.3	16.2	1	18.5	1	19.5		
t _{en}	ŌĒ	Q	0 - 50 - 5		7.7	14.5	1	16.5	1	17.5		
t _{dis}	ŌĒ	Q	C _L = 50 pF		5.9	14	1	16	1	17	ns	
t _{sk(o)}						1.5		1.5				

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER	FROM TO (INPUT)		LOAD CAPACITANCE	T _A = 25°C			SN74LV374A -40°C to +85°C		SN74LV374A -40°C to +125°C		UNIT	
	(INFOT) (COTFO	(001701)	(OUTPUT) CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
			C _L = 15 pF	130 ⁽¹⁾	205 ⁽¹⁾		110		110		MHz	
f _{max}			C _L = 50 pF	85	1705		75		75		IVITZ	
t _{pd}	CLK	Q			4.9 ⁽¹⁾	8.1 ⁽¹⁾	1	9.5	1	10.5		
t _{en}	ŌĒ	Q	C _L = 15 pF		4.6 ⁽¹⁾	7.6 ⁽¹⁾	1	9	1	10	ns	
t _{dis}	ŌĒ	Q			3.4 ⁽¹⁾	6.8 ⁽¹⁾	1	8	1	9		
t _{pd}	CLK	Q			5.9	10.1	1	11.5	1	12.5		
t _{en}	ŌĒ	Q	0 - 50 - 5		5.5	9.6	1	11	1	12		
t _{dis}	ŌĒ	Q	$C_L = 50 \text{ pF}$		4	8.8	1	10	1	11	ns	
t _{sk(o)}						1		1				

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Timing Requirements

over recommended operating free-air temperature range, (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

	·	T _A = 25°	С	SN74LV374A -40°C to +85°C	_	SN74LV374A -40°C to +125°C		UNIT
		MIN	MAX	MIN M	AX	MIN	MAX	
V _{CC} =	2.5 V ± 0.2 V	'	•					
t _w	Pulse duration, CLK high or low	6		7		7		ns
t _{su}	Setup time, data before CLK↑	5		5.5		6		ns
t _h	Hold time, data after CLK↑	2.5		2.5		3		ns
V _{cc} =	3.3 V ± 0.3 V	-						
t _w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t _{su}	Setup time, data before CLK↑	4.5		4.5		5		ns
t _h	Hold time, data after CLK↑	2		2		2.5		ns
V _{cc} =	5 V ± 0.5 V							
t _w	Pulse duration, CLK high or low	5		5		5		ns
t _{su}	Setup time, data before CLK↑	3		3		3.5		ns
t _h	Hold time, data after CLK↑	2		2		2.5		ns



6.10 Noise Characteristics

 $V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$ (1)

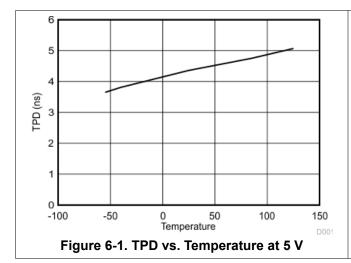
	PARAMETER	SN74LV374A			UNIT
	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.6	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.5	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	2.9	2.9		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

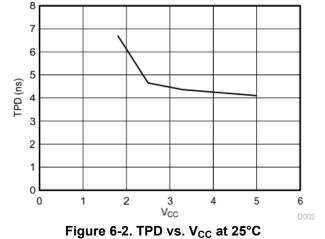
⁽¹⁾ Characteristics are for surface-mount packages only.

6.11 Operating Characteristics, T_A = 25°C

	PARAMETER		TEST CON	DITIONS	V _{cc}	TYP	UNIT
C .	Power dissipation	Outputs enabled	$C_1 = 50 \text{ pF},$	f = 10 MHz	3.3 V	21.1	рĒ
C _{nd}	capacitance		OL – 50 pr,	1 – 10 WIHZ	5 V	22.8	þΓ

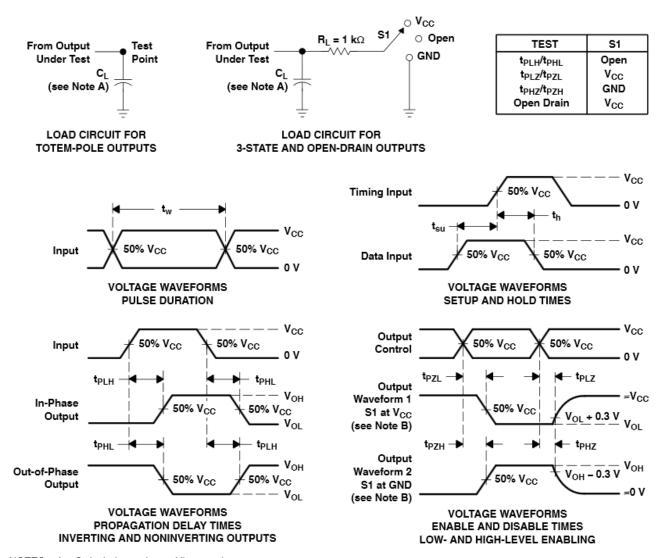
6.12 Typical Characteristics







7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LV374A devices are octal edge-triggered D-type flip-flops designed for 2 V to 5.5 V V_{CC} operation. These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs. A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the latch.

Old data can be retained or new data can be entered while the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using loff. The loff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The output of the device is unknown until the first valid rising clock edge occurs while V_{CC} is within the Section 6.3 range.

8.2 Functional Block Diagram

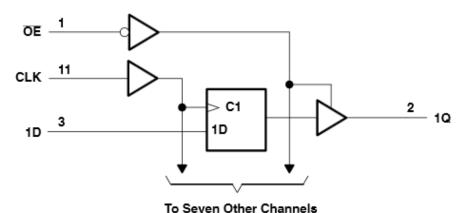


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device's wide operating range allows it to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74LV374A devices.

INPUTS OUTPUT OE CLK Q D L Н Н **↑** L 1 L L L L Χ Q_0 Н Х Χ Ζ

Table 8-1. Function Table (Each Flip-Flop)



9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV374A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V allowing down translation to the V_{CC} level.

9.2 Typical Application

Figure 9-1 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

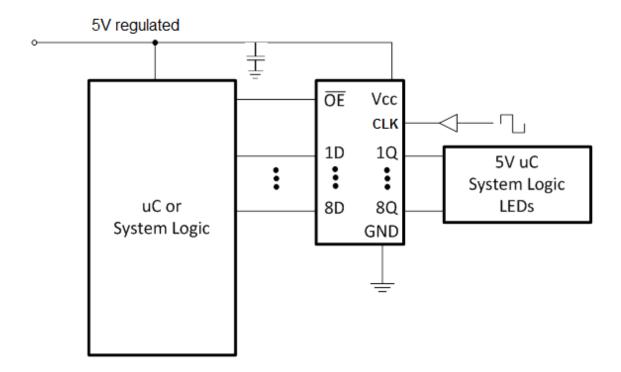


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- · Recommended Input conditions:
 - Rise time and fall time specs see ($\Delta t/\Delta V$) in Section 6.3.
 - Specified High and low levels. See (V_{IH} and V_{IL}) in Section 6.3.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{\rm CC}$.
- · Recommended output conditions:
 - Load currents should not exceed 35 mA per output and 70 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curve

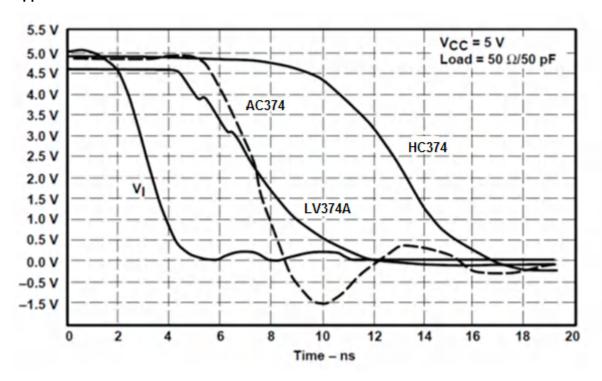


Figure 9-2. Switching Characteristics Comparison

9.3 Power Supply Recommendations

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.



9.4.1.1 Layout Example



Figure 9-3. Layout Example



10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LV374ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ADBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	LV374A
SN74LV374ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV374A
SN74LV374ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV374A
SN74LV374APW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 125	LV374A
SN74LV374APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV374A:

Automotive : SN74LV374A-Q1

● Enhanced Product: SN74LV374A-EP

NOTE: Qualified Version Definitions:

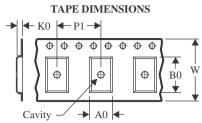
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV374ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV374ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LV374ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV374APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



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*All dimensions are nominal

7 111 41111011010110 410 11011111141							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV374ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV374ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV374ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV374ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV374APWR	TSSOP	PW	20	2000	353.0	353.0	32.0



SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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