

# SN74LV1T08 Single Power Supply 2-Input Positive AND Gate CMOS Logic Level **Shifter**

#### 1 Features

- Single-supply voltage translator at 5.0V, 3.3V, 2.5V, and 1.8V  $V_{CC}$
- Operating range of 1.8V to 5.5V
- Up translation:
  - 1.2V<sup>(1)</sup> to 1.8V at 1.8V V<sub>CC</sub>
  - 1.5V<sup>(1)</sup> to 2.5V at 2.5V V<sub>CC</sub>
  - 1.8V<sup>(1)</sup> to 3.3V at 3.3V V<sub>CC</sub>
  - 3.3V to 5.0V at 5.0V V<sub>CC</sub>
- Down translation:
  - 3.3V to 1.8V at 1.8V V<sub>CC</sub>
  - 3.3V to 2.5V at 2.5V V<sub>CC</sub>
  - 5.0V to 3.3V at 3.3V V<sub>CC</sub>
- Logic output is referenced to V<sub>CC</sub>
- Output drive:
  - 8mA Output Drive at 5V
  - 7mA Output Drive at 3.3V
  - 3mA Output Drive at 1.8V
- Characterized up to 50MHz at 3.3V V<sub>CC</sub>
- 5V tolerance on input pins
- -40°C to 125°C operating temperature range
- Pb-free packages available: SC-70 (DCK)
  - $-2 \times 2.1 \times 0.65$ mm (height 1.1mm)
- Latch-up performance exceeds 250mA per JESD 17
- Supports standard logic pinouts
- CMOS output B compatible with AUP1G and LVC1G families 1

# 2 Applications

- **Telecom**
- Portable applications
- Servers
- PC and notebooks

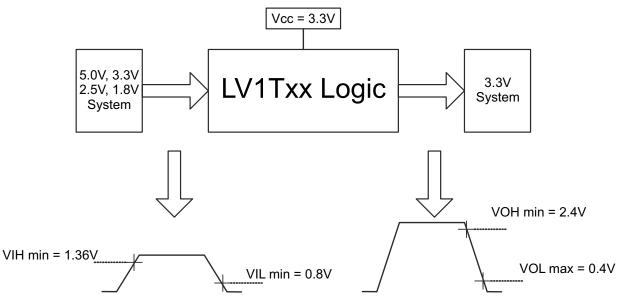
# 3 Description

The SN74LV1T08 is a single 2-input AND gate with reduced input thresholds to support voltage translation applications.

### **Package Information**

PART NUMBER	PART NUMBER PACKAGE SIZ		BODY SIZE(3)
SN74LV1T08	DBV (SOT-23, 5)	2.90mm × 2.8mm	2.9mm x 1.6mm
3N/4LV1100	DCK (SC70, 5)	2.00mm × 2.1mm	2mm × 1.25mm

- For more information, see Section 12.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length x width) is a nominal value and does not include pins.



Refer to the V<sub>IH</sub>/V<sub>IL</sub> and output drive for lower V<sub>CC</sub> condition.

Switching Thresholds for 1.8V to 3.3V Translation



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# **4 Related Products**

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T17	DCK, DBV	Single Schmitt-Trigger Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T34	DCK, DBV	Single Buffer Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV1T126	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs



# **5 Pin Configuration and Functions**

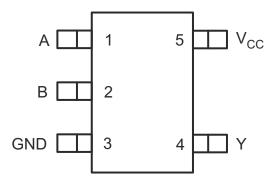


Figure 5-1. DCK or DBV Package, 5-Pin SC70 or SOT-23 (Top View)

**Table 5-1. Pin Functions** 

Р	IN	TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.	ITPE\''	DESCRIPTION
Α	1	I	Input A
В	2	I	Input B
GND	3	G	Ground
Υ	4	0	Output Y
V <sub>CC</sub>	5	Р	Positive supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

# 6 Specifications

# 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7.0	V
VI	Input voltage range <sup>(2)</sup>		-0.5	7.0	V
Vo	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		-0.5	4.6	V
V <sub>O</sub>	Voltage range applied to a	Voltage range applied to any output in the high or low state <sup>(2)</sup>			
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-20	mA
lok	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output curren	t i		±25	mA
	Continuous current throug	gh V <sub>CC</sub> or GND		±50	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

	-		VALUE	UNIT
V	V <sub>(FCD)</sub> Flectrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
V(ESD)		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	'

<sup>(1)</sup> JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.6	5.5	V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.8V		-3	
I <sub>OH</sub>	High level output ourrent	V <sub>CC</sub> = 2.5V		<b>–</b> 5	mA
	High-level output current	V <sub>CC</sub> = 3.3V		-7	ША
		V <sub>CC</sub> = 5.0V		-8	
		V <sub>CC</sub> = 1.8V		3	
	Low lovel output ourrent	V <sub>CC</sub> = 2.5V		5	A
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3.3V		7	mA
		V <sub>CC</sub> = 5.0V		8	
		V <sub>CC</sub> = 1.8V		20	
Δt/Δν	Input transition rise or fall rate	V <sub>CC</sub> = 3.3V or 2.5V		20	ns/V
		V <sub>CC</sub> = 5.0V		20	
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

<sup>2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.



# **6.4 Thermal Information**

	THERMAL METRIC <sup>(1)</sup>	DBV	DCK	UNIT	
	THERWAL WETRIC	5 PINS 5 PINS		ONII	
F	R <sub>0JA</sub> Junction-to-ambient thermal resistance	278	289.2	°C/W	

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COMPLETIONS	V	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to 1	25°C	1150-	
PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP MAX	MIN	MAX	UNIT	
			V <sub>CC</sub> = 1.65V to 1.8V	0.94		1.0			
			V <sub>CC</sub> = 2.0V	1.02		1.03			
			V <sub>CC</sub> = 2.25V to 2.5V	1.135		1.18			
V <sub>IH</sub> High-level inpu voltage	High-level input		V <sub>CC</sub> = 2.75V	1.21		1.23		V	
	voltage		V <sub>CC</sub> = 3V to 3.3V	1.35		1.37		V	
			V <sub>CC</sub> = 3.6V	1.47		1.48			
			V <sub>CC</sub> = 4.5V to 5.0V	2.02		2.03			
			V <sub>CC</sub> = 5.5V	2.1		2.11			
			V <sub>CC</sub> = 1.65V to 2.0V		0.58		0.55		
,	Low-level input		V <sub>CC</sub> = 2.25V to 2.75V		0.75		0.71	.,	
′ı∟	voltage		V <sub>CC</sub> = 3V to 3.6V		0.8		0.65	V	
			V <sub>CC</sub> = 4.5V to 5.5V		0.8		0.8		
		I <sub>OH</sub> = -20μA	1.65V to 5.5V	V <sub>CC</sub> - 0.1		V <sub>CC</sub> - 0.1			
			1.65V	1.28	·	1.21			
		$I_{OH} = -2.0$ mA	1.8V	1.5	·	1.45			
		I <sub>OH</sub> = -2.3mA	201	2.0	·	2.0			
		$I_{OH} = -3\text{mA}$		2.0		1.93			
		I <sub>OH</sub> = -3mA	2.5V	2.25		2.15			
′он		I <sub>OH</sub> = -3.0mA		2.78		2.7		V	
		I <sub>OH</sub> = -5.5mA	3.0V	2.6		2.49		-	
		I <sub>OH</sub> = -5.5mA	3.3V	2.9		2.8			
		I <sub>OH</sub> = -4mA	1 -11	4.2		4.1			
		I <sub>OH</sub> = -8mA	4.5V	4.1		3.95			
		I <sub>OH</sub> = -8mA	5.0V	4.6		4.5			
		I <sub>OL</sub> = 20μA	1.65V to 5.5V		0.1		0.1		
		I <sub>OL</sub> = 1.9mA	1.65V		0.2		0.25		
		I <sub>OH</sub> = 2.3mA			0.1		0.15		
		I <sub>OH</sub> = 3mA	2.3V		0.15		0.2		
OL.		I <sub>OL</sub> = 3mA			0.1		0.15	V	
		I <sub>OL</sub> = 5.5mA	3.0V		0.2		0.252		
		I <sub>OL</sub> = 4mA			0.15		0.2		
		I <sub>OL</sub> = 8mA	4.5V		0.3		0.35		
1	A input	V <sub>I</sub> = 0V or V <sub>CC</sub>	0V, 1.8V, 2.5V, 3.3V, 5.5V		0.12		±1	μA	
			5.0V		1		10		
		$V_I = 0V \text{ or } V_{CC}$	3.3V		1		10		
CC		I <sub>O</sub> = 0; open on loading	2.5V		1		10	μA	
			1.8V		1				

Product Folder Links: SN74LV1T08

# **6.5 Electrical Characteristics (continued)**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to	UNIT	
PARAMETER	TEST CONDITIONS	<b>V</b> CC	MIN	TYP	MAX	MIN	MAX	UNIT
AL.	One input at 0.3V or 3.4V, Other inputs at 0 or $V_{CC}$ , $I_{O} = 0$	5.5V		1.35		1.5	mA	
Δl <sub>CC</sub>	One input at 0.3V or 1.1V Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	1.8V			10		10	μА
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3V		2	10	2	10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3V		2.5		2.5		pF

# **6.6 Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	FREQUENCY	V	CL	T	= 25°	С	T <sub>A</sub> = -6	5°C to 1	25°C	UNIT							
PARAMETER	(INPUT)	(OUTPUT)	(TYP)	V <sub>CC</sub>	CL	MIN	TYP	MAX	MIN	TYP	MAX	UNIT							
				5.0V	15pF		4	5		4	5	no							
			DC to 50MHz	5.00	30pF		5.5	7.0		5.5	7.0	ns							
		Y	DC to SOME	DC to Solvil iz	DC to 30WII 12	DC to Joini iz	DC to Solvinz	DC to Solvil 12	DC to Joini iz	DC to Solvii iz	DC to Solvil 12	3.3V	15pF		4.8	5		5	5.5
	Anyla					3.34	30pF		5	5.5		5.5	6.5	ns					
t <sub>pd</sub>	Any In	Ţ	DC to 25MHz	2.5V	15pF		6	6.5		7	7.5	no							
				DC to 25MH2	2.50	30pF		6.5	7.5		7.5	8.5	ns						
			DO: 451411	DC to 15MHz 1	DC to 15MHz 1.8	1 0\/	15pF		10.5	11		11	12	no					
						DC to 15MHZ	DC to 15MHZ	DC to TSMHZ	DC to TSIMHZ	DC to TSIVIES	DC to 15MHZ	DC to TSIVIES	DC to 15MHZ	DC to TOWNEY 1.8	1.8V	30pF		12	13

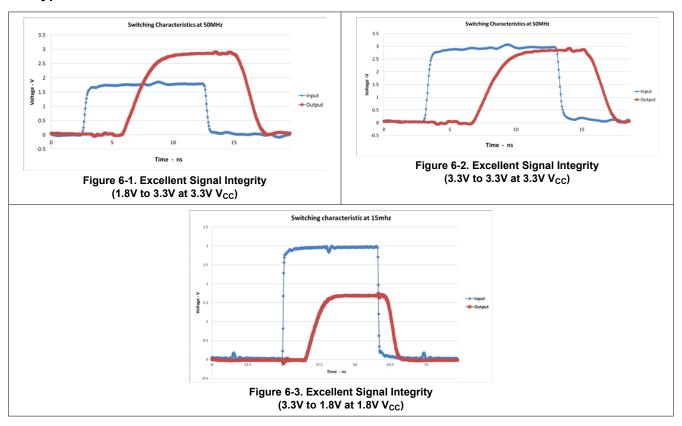
# **6.7 Operating Characteristics**

T<sub>A</sub> = 25°C

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
			1.8V ± 0.15V	10	
C <sub>pd</sub>	Dower dissination consistence	f = 1MHz and 10MHz	2.5V ± 0.2V	10	
	Power dissipation capacitance	I – IMINZ AND IDMINZ	3.3V ± 0.3V	10	- pF
			5.5V ± 0.5V	10	

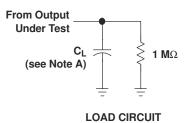


# **6.8 Typical Characteristics**

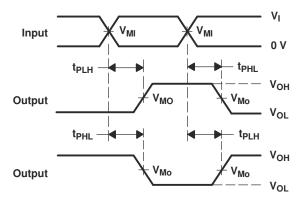




# 7 Parameter Measurement Information



	V <sub>CC</sub> = 2.5 V ± 0.2 V	$V_{CC}$ = 3.3 V $\pm$ 0.3 V
C <sub>L</sub>	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V <sub>MI</sub>	V <sub>I</sub> /2	V <sub>I</sub> /2
V <sub>MO</sub>	V <sub>CC</sub> /2	V <sub>CC</sub> /2



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 7-1. Load Circuit and Voltage Waveforms

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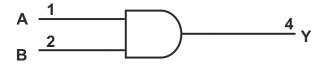
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# 8 Detailed Description

### 8.1 Overview

The SN74LV1T08 device is a low-voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, telecom, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8V, 2.5V, 3.3V, and 5V CMOS levels. The input is designed with a lower threshold circuit to match 1.8V input logic at  $V_{CC} = 3.3V$  and can be used in 1.8V to 3.3V level-up translation. In addition, the 5V tolerant input pins enable down translation (that is, 3.3V to 2.5V output at  $V_{CC} = 2.5V$ ). The wide  $V_{CC}$  range of 1.8V to 5.5V allows generation of desired output levels to connect to controllers or processors. The SN74LV1T08 device is designed with current-drive capability of 8mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

## 8.2 Functional Block Diagram



### 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

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### 8.3.2 LVxT Enhanced Input Voltage

The SN74LV1T08 belongs to Tl's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified  $V_{IH(MIN)}$  level for a HIGH input state, and at or below the specified  $V_{IL(MAX)}$  for a LOW input state. Figure 8-1 shows the typical  $V_{IH}$  and  $V_{IL}$  levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law  $(R = V \div I)$ .

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a  $10k\Omega$  resistor is recommended and will typically meet all requirements.

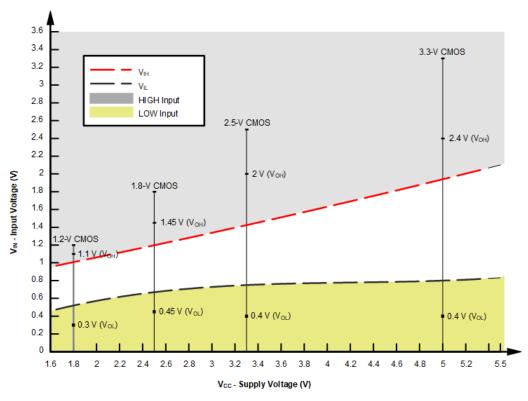


Figure 8-1. LVxT Input Voltage Levels

#### 8.3.2.1 Up Translation

Input signals can be up translated using the SN74LV1T08. The voltage applied at  $V_{CC}$  will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables. When connected to a high-impedance input, the output voltage will be approximately V<sub>CC</sub> in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a V<sub>IH(MIN)</sub> of 3.5V. For the SN74LV1T08, V<sub>IH(MIN)</sub> with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

Ensure that the input signals in the HIGH state are above V<sub>IH(MIN)</sub> and input signals in the LOW state are lower than  $V_{IL(MAX)}$  as shown in Figure 8-2.

Up Translation Combinations are as follows:

- 1.8V V<sub>CC</sub> Inputs from 1.2V
- 2.5V V<sub>CC</sub> Inputs from 1.8V
- $3.3V\ V_{CC}$  Inputs from 1.8V and 2.5V
- 5.0V V<sub>CC</sub> Inputs from 2.5V and 3.3V

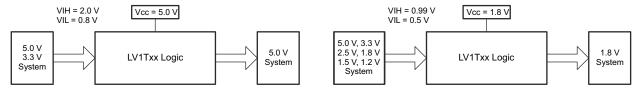


Figure 8-2. LVxT Up and Down Translation Example

#### 8.3.2.2 Down Translation

Signals can be translated down using the SN74LV1T08. The voltage applied at the  $V_{CC}$  will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables.

When connected to a high-impedance input, the output voltage will be approximately V<sub>CC</sub> in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between  $V_{H(MIN)}$  and 5.5V, and input signals in the LOW state are lower than  $V_{IL(MAX)}$  as shown in Figure 8-1.

For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V V<sub>CC</sub>. See Figure 8-2.

Product Folder Links: SN74LV1T08

Down Translation Combinations are as follows:

- 1.8V V<sub>CC</sub> Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V V<sub>CC</sub> Inputs from 3.3V and 5.0V
- 3.3V V<sub>CC</sub> Inputs from 5.0V

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## 8.3.3 Clamp Diode Structure

As Figure 8-3 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

#### **CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

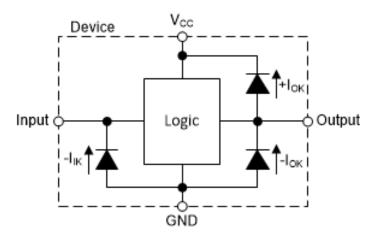


Figure 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

### **Function Table**

	UT <sup>(1)</sup> VEL INPUT)	OUTPUT <sup>(2)</sup> (V <sub>CC</sub> CMOS)							
Α	В	Υ							
Н	Н	Н							
L	Х	L							
X	L	L							
	SUPPLY V <sub>CC</sub> = 3.3V								
А	В	Y							
	) = 1.35V = 0.08 V	$V_{OH}(min) = 2.9V$ $V_{OL}(max) = 0.2V$							

- (1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

# 9 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

# 9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu F$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The  $0.1\mu F$  and  $1\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 9.2 Layout

### 9.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 9.2.2 Layout Example

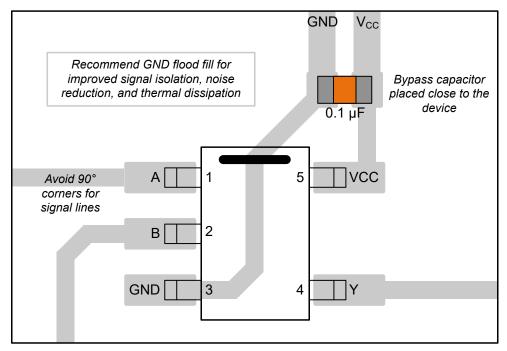


Figure 9-1. Example Layout for the SN74LV1T08

Product Folder Links: SN74LV1T08

# 10 Device and Documentation Support

# 10.1 Documentation Support (Analog)

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, Designing With Logic application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices
  application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

# 10.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 10.4 Trademarks

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## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2024) to Revision F (October 2025)	Page		
Updated Functional Block Diagram	10		
Changes from Revision D (October 2023) to Revision E (March 2024)	Page		
• Updated RθJA values: DBV = 206 to 278, all values in °C/W			
Changes from Revision C (June 2022) to Revision D (October 2023)	Page		
Updated Package Information table			

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Removed machine model from ESD Ratings table......5



• Updated RθJA values: DCK = 252 to 289.2, all values in °C/W......6

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	(.)	(-)			(0)	(4)	(5)		(0)
SN74LV1T08DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39RH, 3CGF, NEE3, NEEJ, NEES)
SN74LV1T08DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39RH, 3CGF, NEE3, NEEJ, NEES)
SN74LV1T08DBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NEE3
SN74LV1T08DBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NEE3
SN74LV1T08DCKR	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QZ, WE3, WEJ, WE S)
SN74LV1T08DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QZ, WE3, WEJ, WE S)
SN74LV1T08DCKRG4	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	WE3
SN74LV1T08DCKRG4.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE3

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 7-Oct-2025

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#### OTHER QUALIFIED VERSIONS OF SN74LV1T08:

Automotive: SN74LV1T08-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 1-Nov-2025

# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T08DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LV1T08DBVRG4	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LV1T08DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LV1T08DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

www.ti.com 1-Nov-2025



### \*All dimensions are nominal

7 111 41111011010110 41 0 11011111141							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T08DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LV1T08DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T08DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LV1T08DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0





### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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