





SN74LV165A SCLS402R - APRIL 1998 - REVISED MARCH 2023

SN74LV165A Parallel-Load 8-Bit Shift Registers

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Maximum t_{pd} of 10.5 ns at 5 V
- Support mixed-mode voltage operation on all ports
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

Increase the Number of Inputs on a Microcontroller

3 Description

The SN74LV165A device is a parallel-load, 8-bit shift registers designed for 2 V to 5.5 V V_{CC} operation.

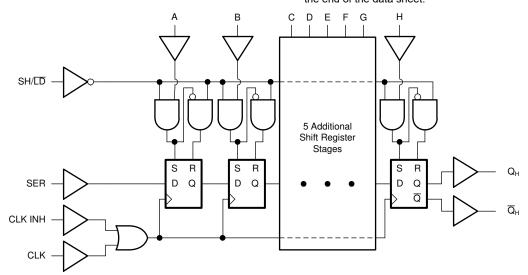
When the device is clocked, data is shifted toward the serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/ LD) input. The 'LV165A devices feature a clock-inhibit function and a complemented serial output, Q H.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

Package Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	D (SOIC, 16)	9.90 mm × 3.90 mm
	DB (SSOP, 16)	6.20 mm × 5.30 mm
	NS (SO, 16)	10.20 mm × 5.30 mm
SN74LV165A	PW (TSSOP, 16)	5.00 mm × 4.40 mm
	DGV (TVSOP, 16)	3.60 mm × 4.40 mm
	RGY (VQFN, 16)	4.00 mm × 3.50 mm
	BQB (WQFN, 16)	3.60 mm × 2.60 mm

For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)



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Changes from Revision Q (December 2022) to Revi	
 Updated structural layout of document and formatte 	d tables to current standard1
Changes from Revision P (June 2022) to Revision (Q (December 2022) Page
 Changed data sheet status from Advanced Information 	tion to Production Data1
Changes from Revision O (November 2016) to Revi	sion P (June 2022) Page
, , , , ,	e Information, Pin Configuration and Thermal Information
	nd cross-references throughout the document1
Updated specifications table formatting	6
Changes from Revision N (July 2013) to Revision C	(November 2016) Page
· Added Applications section, Device Information table	e, Table of Contents, Pin Configuration and Functions

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section, Specifications section, ESD Ratings table, Thermal Information table, Typical Characteristics section, Detailed Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and



5 Pin Configuration and Functions

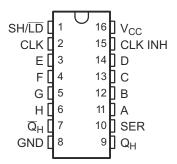


Figure 5-1. D, DB, DGV, N or PW Package, 16-Pin SOIC, SSOP, TVSOP, SOP or TSSOP (Top View)

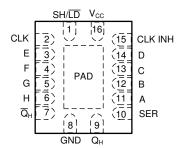


Figure 5-2. RGY or BQB Package, 16-Pin VQFN or WQFN (Top View)

Table 5-1. Pin Functions

F	PIN	TYPE (1)	DESCRIPTION
NAME	NO.	I TPE ('')	DESCRIPTION
Α	11	I	Serial input A
В	12	I	Serial input B
С	13	I	Serial input C
CLK	2	I	Storage clock
CLK INH	15	I	Storage clock
D	14	I	Serial input D
E	3	I	Serial input E
F	4	I	Serial input F
G	5	I	Serial input G
GND	8	G	Ground pin
Н	6	I	Serial input H
Q _H	7	0	Output H, inverted
Q _H	9	0	Output H
SH/ LD	1	1	Load Input
SER	10	I	Serial input
V _{CC}	16	Р	Power pin
PAD		_	Thermal Pad ⁽²⁾

⁽¹⁾ I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

⁽²⁾ RGY and BQB Package Only



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
VI	Input voltage ⁽²⁾		-0.5	7	V
Vo	Voltage range applied to any output in the high-impedance or	power-off state ⁽²⁾	-0.5	7	V
Vo	Output voltage (2) (3)				
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _{jmax}	Maximum virtual junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
	/ _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
V _(ESD)		Machine Model (MM), per JEDEC specification	±200	v
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		2	5.5	V	
		V _{CC} = 2 V	1.5			
.,	High level input valtege	V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V	
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	1.5 V _{CC} × 0.7 V _{CC} × 0.7		
		V _{CC} = 2 V		0.5		
.,	Low level input veltage	V _{CC} = 2.3 V to 2.7 V	,	$V_{CC} \times 0.3$ $V_{CC} \times 0.3$ $V_{CC} \times 0.3$ 5.5 $V_{CC} -50$	V	
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V	,	V _{CC} × 0.3	V	
		V _{CC} = 4.5 V to 5.5 V	,	V _{CC} × 0.3		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 2 V		-50	μA	
	High lavel autout august	V _{CC} = 2.3 V to 2.7 V		-2		
I _{OH}	High-level output current	V _{CC} = 3 V to 3.6 V		5.5 V _{CC} × 0.3 V _{CC} × 0.3 V _{CC} × 0.3 5.5 V _{CC} -50 -2 -6 -12 50 2 6 12 200	mA	
		V _{CC} = 4.5 V to 5.5 V		-12		
		V _{CC} = 2 V		50	μΑ	
	Lave lavel autout aumant	V _{CC} = 2.3 V to 2.7 V		2		
OL	Low-level output current	V _{CC} = 3 V to 3.6 V		6	mA	
		V _{CC} = 4.5 V to 5.5 V		12		
		V _{CC} = 2.3 V to 2.7 V		200		
Δt/Δν	Input transition rise or fall rate	V _{CC} = 3 V to 3.6 V		100	ns/V	
		V _{CC} = 4.5 V to 5.5 V		20		
T _A	Operating free-air temperature	·	-40	125	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs

6.4 Thermal Information

				5	SN74LV165	4			
	THERMAL METRIC ⁽¹⁾	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	DGV (TVSOP)	RGY (VQFN)	BQB (WQFN)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.2	102.8	89.4	113.3	125.9	48.8	85.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	46.1	53.3	47.9	48.3	51	46.7	82.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.8	53.5	49.8	58.4	57.7	24.9	55.6	°C/W
Ψлт	Junction-to-top characterization parameter	13.2	16.6	16.6	6.4	5.7	2	9.4	°C/W
ΨЈВ	Junction-to-board characterization parameter	43.5	52.9	49.5	57.8	57.2	24.9	55.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	11.7	33.3	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	v	-40°0	C to 85°C		-40°	C to 125°	,C	UNIT
	PARAWETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN	TYP	MAX	UNII
		I _{OH} = –50 mA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			
V _{OH}	High-level output voltage	I _{OH} = -2 mA	2.3 V	2			2			V
		I _{OH} = -6 mA	3 V	2.48			2.48			
		I _{OH} = -12 mA	4.5 V	3.8			3.8			
		I _{OL} = 50 mA	2 V to 5.5 V			0.1			0.1	
V	Low-level output voltage	I _{OL} = 2 mA	2.3 V			0.4			0.4	· /
V _{OL}	Low-level output voltage	I _{OL} = 6 mA	3 V			0.44			0.44	v
		I _{OL} = 12 mA	4.5 V			0.55			0.1 0.4	
I	Input leakage current	V _I = 5.5 V or GND	0 V to 5.5 V			±1			±1	μΑ
I _{CC}	Static supply current	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			20	μΑ
I _{off}	Partial power down current	V_{I} or $V_{O} = 0$ to 5.5 V	0			5			5	μA
Ci	Input capacitance	V _I = V _{CC} or GND	3.3 V		1.7			1.7		pF

6.6 Timing Requirements, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

	PARAMETER	TEST CONDITION	25°C	;	-40°C to	85°C	-40°C to 1	125°C	UNIT	
	PARAMETER	TEST CONDITION	MIN	MAX	MIN	MAX	MIN	MAX	UNII	
	Pulse duration	CLK high or low	8.5		9		9		no	
t _w	Fuise duration	SH/ LD low	11		13		13		ns	
		SH/ LD high before CLK↑	7		8.5		8.5			
	Catum tima	SER before CLK↑	8.5		9.5		9.5		no	
t _{su}	Setup time	CLK INH before CLK↑	7		7		7		ns	
		Data before SH/ LD↑	11.5		12		12			
		SER data after CLK↑	-1		0		0			
t _h	Hold time	Parallel data after SH/ LD↑	0		0		0		ns	
		SH/ LD high after CLK↑	0		0		0			

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted (see Figure 7-1)

	PARAMETER	TEST CONDITION	25°C	;	−40°C to	85°C	-40°C to 1	25°C	UNIT	
	PARAMETER	TEST CONDITION	MIN	MAX	MIN	MAX	MIN	MAX	UNII	
	Pulse duration	CLK high or low	6		7		7		no	
ιw	Puise duration	SH/ LD low	7.5		9		9		ns	
		SH/ LD high before CLK↑	5		6		6			
	Catum times	SER before CLK↑	5		6		6		ns	
t _{su}	Setup time	CLK INH before CLK↑	5		5		5			
		Data before SH/ LD ↑	7.5		8.5		8.5			
		SER data after CLK↑	0		0		0			
t _h	Hold time	Parallel data after SH/ ID ↑	0.5		0.5		0.5		ns	
		SH/ LD high after CLK↑	0		0		0			

Product Folder Links: SN74LV165A



6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

	PARAMETER	TEST CONDITION	25°C		–40°C to	85°C	-40°C to 1	25°C	UNIT
	FARAMETER	TEST CONDITION	MIN	MAX	MIN	MAX	MIN	MAX	UNII
	Pulse duration	CLK high or low	4		4		4		ns
ι _w	Fuise duration	SH/ $\overline{\text{LD}}$ low	5		6		6		115
		SH/ LD high before CLK↑	4		4		4		
	Setup time	SER before CLK↑	4		4		4		ns
t _{su}	Setup time	CLK INH before CLK↑	3.5		3.5		3.5		115
		Data before SH/ LD↑	5		5		5		
		SER data after CLK↑	0.5		0.5		0.5		
t _h	t _h Hold time	Parallel data after SH/ LD ↑	1		1		1		ns
		SH/ LD high after CLK↑	0.5		0.5		0.5		

6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over operating free-air temperature range (unless otherwise noted), (see Figure 7-1)

PARAMET	FROM	то	LOAD		25°C		-40°C to 85°C		-40°	UNIT																																
ER	(INPUT) (OUTPUT	(OUTPUT)	CAP	MIN	TYP	MAX	MIN	TYP MAX	MIN	TYP MAX																																
f			C _L = 15 pF	50	80		45		45		MHz																															
f _{max}			C _L = 50 pF	40	65		35		35	35	IVITIZ																															
	CLK				12.2	19.8	1	22	1	22																																
t _{pd}	SH/ LD	Q_H or \overline{Q}	C _L = 15 pF		13.1	21.5	1	23.5	1	23.5	ns																															
	Н																																			12.9	21.7	1	24	1	24	
	CLK				15.3	23.3	1	26	1	26																																
t _{pd}	SH/ LD	Q_H or \overline{Q}	C _L = 50 pF		16.1	25.1	1	28	1	28	ns																															
	Н	1			15.9	25.3	1	28	1	28	1																															

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted), (see Figure 7-1)

PARAMETER	FROM TO		LOAD		25°C		–40°	C to 85°C	-40°	C to 125°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAP	MIN	TYP	MAX	MIN	TYP MAX	MIN	TYP MAX	ONIT
f _{max}			C _L = 15 pF	65	115		55		55		MHz
			C _L = 50 pF	60	90		50		50		IVITIZ
	CLK		C _L = 15 pF		8.6	15.4	1	18	1	18	
t _{pd}	SH/ LD	Q_H or \overline{Q}			9.1	15.8	1	18.5	1	18.5	ns
	Н				8.9	14.1	1	16.5	1	16.5	
	CLK				10.9	14.9	1	16.9	1	16.9	
t _{pd}	SH/ LD	Q_H or \overline{Q}	C _L = 50 pF		11.3	19.3	1	22	1	22	ns
	Н		F		11.1	17.6	1	20	1	20	



6.11 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (see Figure 7-1)

PARAMETER	FROM	то	LOAD		25°C		-40°	°C to 85°C	-40°	C to 125°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAP	MIN	TYP	MAX	MIN	TYP MAX	MIN	TYP MAX	UNIT
			C _L = 15 pF	110	165		90		90		- MHz
f _{max}			C _L = 50 pF	95	125		85		85		- IVITZ
	CLK				6	9.9	1	11.	5 1	11.5	
t _{pd}	SH/ LD	Q_H or \overline{Q}	C _L = 15 pF		6	9.9	1	11.	5 1	11.5	ns
	Н				6	9.9	1	10.	5 1	10.5	
	CLK		0 -0		7.7	11.9	1	13.	5 1	13.5	
t _{pd}	SH/ LD	Q_H or \overline{Q}	$C_L = 50$ pF		7.7	11.9	1	13.	5 1	13.5	ns
	Н		μ.		7.6	11	1	12.	5 1	12.5	

6.12 Timing Diagrams

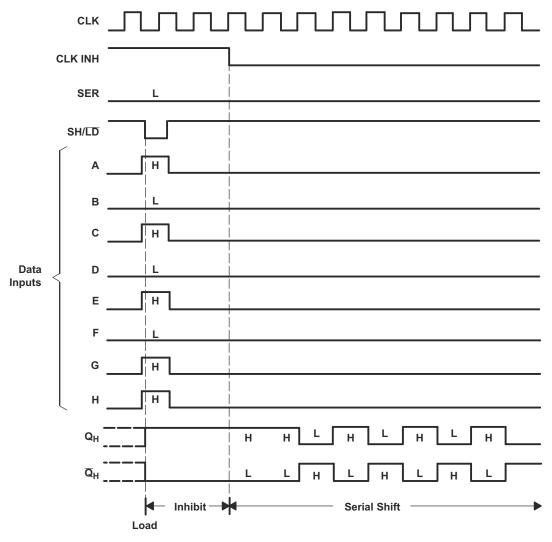


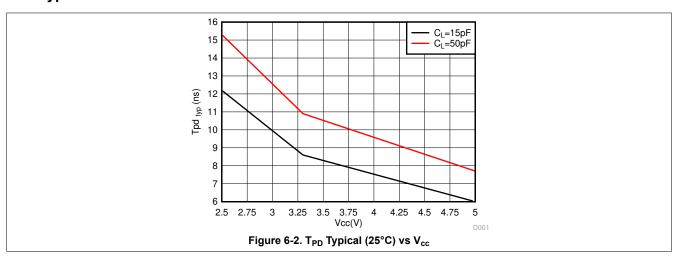
Figure 6-1. Typical Shift, Load, and Inhibit Sequences

6.13 Operating Characteristics

 $T_A = 25^{\circ}C$

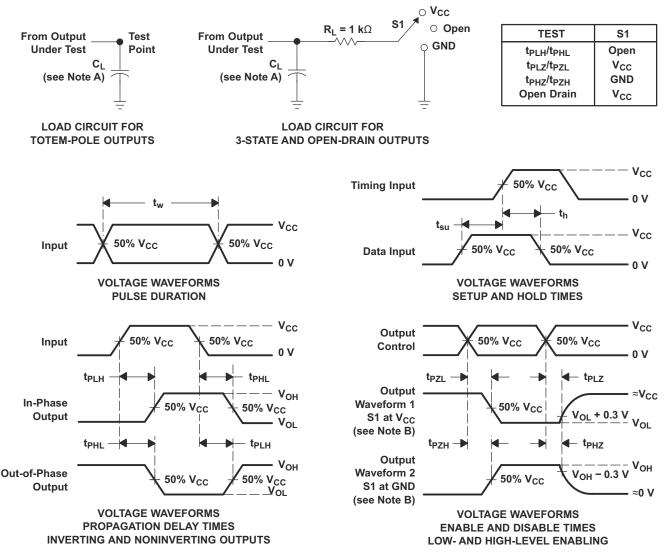
	PARAMETER	TEST CO	ONDITIONS	V _{CC}	TYP	UNIT
_	Power dissipation capacitance	$C_1 = 50 pF$	f = 10 MHz	3.3 V	36.1	nE
Opd	rower dissipation capacitance	C _L = 50 pF	1 – 10 WHZ	5 V	37.5	p⊦

6.14 Typical Characteristics





7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

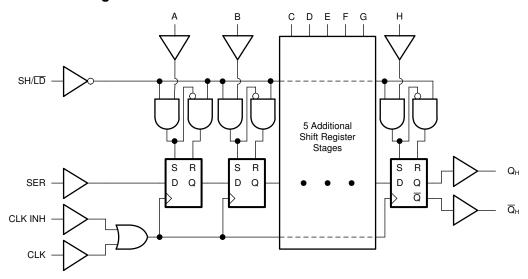
The SN74LV165A device is a parallel-load, 8-bit shift registers designed for 2 V to 5.5 V V_{CC} operation.

When the device is clocked, data is shifted toward the serial output Q_H . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/ \overline{LD}) input. The 'LV165A devices feature a clock-inhibit function and a complemented serial output, \overline{Q}_H .

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/ $\overline{\text{LD}}$ is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH must be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/ $\overline{\text{LD}}$ is held high. The parallel inputs to the register are enabled while SH/ $\overline{\text{LD}}$ is held low, independently of the levels of CLK, CLK INH, or SER.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

8.3.4 Clamp Diode Structure

Figure 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

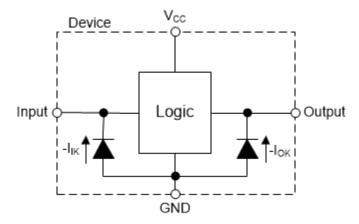


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

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8.4 Device Functional Modes

The Operating Mode Table and the Output Function Table list the functional modes of the SN74LV165A.

Table 8-1. Operating Mode Table

	rabio o ir operaniig meae rabio									
INPUTS ⁽¹⁾	NPUTS ⁽¹⁾									
SH/LD	CLK	CLK INH	FUNCTION							
L	X	Х	Parallel load							
Н	Н	Х	No change							
Н	X	Н	No change							
Н	L	1	Shift ⁽²⁾							
Н	1	L	Shift ⁽²⁾							

- (1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, ↑ = Low to High transition
- (2) Shift: Content of each internal register shifts towards serial output Q_H. Data at SER is shifted into the first register.

Table 8-2. Output Function Table

INTERNAL REG	ISTERS(1) (2)	OUTPUTS(2)			
A — G	н	Q Q			
Х	L	L	Н		
X	Н	Н	L		

- (1) Internal registers refer to the shift registers inside the device. These values are set by either loading data from the parallel inputs, or by clocking data in from the serial input.
- (2) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV165A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates minimize overshoot and undershoot on the outputs.

9.2 Typical Application

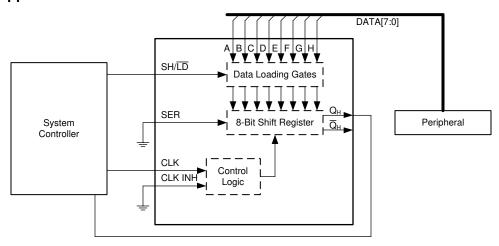


Figure 9-1. Input Expansion with Shift Registers

9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV165A plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV165A plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV165A can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV165A can drive a load with total resistance described by $R_L \ge V_O$ / I_O , with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear* and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV165A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV165A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the Feature Description section for additional information regarding the inputs for this device.

9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

9.2.4 Detailed Design Procedure

- Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the
 device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the Layout
 section.
- 2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV165A to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

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9.2.5 Application Curve

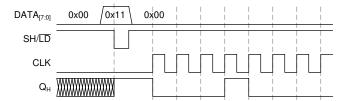


Figure 9-2. Application Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 6.1 section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01- μ F or 0.022- μ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

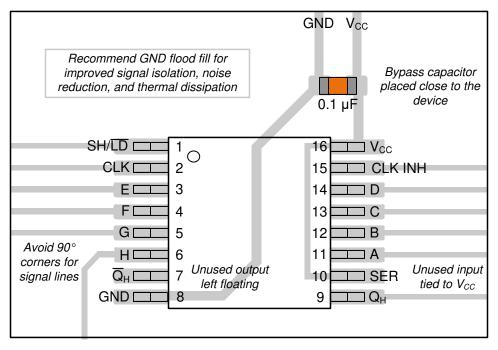


Figure 9-3. Example Layout for the SN74LV165A in the PW Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV165A	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

10.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LV165ABQBR	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ABQBR.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 125	LV165A
SN74LV165ADBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADGVR.A	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADRG3	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADRG3.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ADRG4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV165A
SN74LV165ANSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV165A
SN74LV165APW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 125	LV165A
SN74LV165APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165APWRG3	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165APWRG3.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165APWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ARGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A
SN74LV165ARGYRG4	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV165A:

Automotive: SN74LV165A-Q1

Enhanced Product: SN74LV165A-EP

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications



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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV165ABQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74LV165ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV165ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV165ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV165APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG3	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74LV165APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74LV165ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
Device	i ackage Type	i ackage Diawing	1 1113	31-W	Length (IIIII)	width (IIIII)	rieigiit (iiiii)
SN74LV165ABQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74LV165ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LV165ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74LV165ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LV165ADRG3	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV165ADRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV165ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LV165APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV165APWRG3	TSSOP	PW	16	2000	366.0	364.0	50.0
SN74LV165APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV165APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV165APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV165ARGYR	VQFN	RGY	16	3000	360.0	360.0	36.0



SOP



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



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Last updated 10/2025