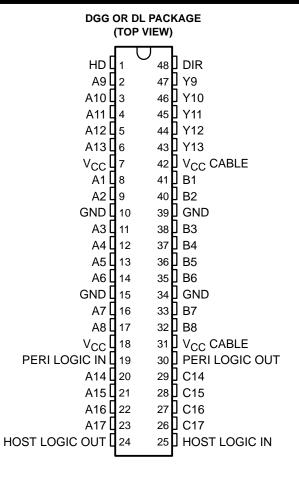
- 4.5-V to 5.5-V V_{CC} Operation
- 1.4-kΩ Pullup Resistors Integrated on All Open-Drain Outputs Eliminate the Need for Discrete Resistors
- Designed for IEEE Std 1284-I (Level-1 Type) and IEEE Std 1284-II (Level-2 Type) Electrical Specifications
- Flow-Through Architecture Optimizes PCB Lavout
- Latch-Up Performance Exceeds 250 mA Per JEDEC 17
- ESD Protection Exceeds JESD 22
 - 4000-V Human-Body Model (A114-A)
 - 300-V Machine Model (A115-A)
 - 2000-V Charged-Device Model (C101)

description/ordering information

The SN74LV161284 is designed for 4.5-V to 5.5-V V_{CC} operation. This device provides asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

This device has eight bidirectional bits; data can flow in the A-to-B direction when DIR is high, and in the B-to-A direction when DIR is low. This device also has five drivers, which drive the cable side, and four receivers. The SN74LV161284 has one receiver dedicated to the HOST LOGIC line and a driver to drive the PERI LOGIC line.



The output drive mode is determined by the high-drive (HD) control pin. When HD is high, the B, Y, and PERI LOGIC OUT outputs are in a totem-pole configuration, and in an open-drain configuration when HD is low. This meets the drive requirements as specified in the IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) parallel peripheral-interface specifications. Except for HOST LOGIC IN and PERI LOGIC OUT, all cable-side pins have a 1.4-k Ω integrated pullup resistor. The pullup resistor is switched off if the associated output driver is in the low state or if the output voltage is above V_{CC} CABLE. If V_{CC} CABLE is off, PERI LOGIC OUT is set to low.

The device has two supply voltages. V_{CC} is designed for 4.5-V to 5.5-V operation. V_{CC} CABLE supplies the output buffers of the cable side only and is designed for 4.5-V to 5.5-V operation.

ORDERING INFORMATION

TA	PACKAGI	ʆ	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
-40°C to 85°C	SSOP – DL	Tube	SN74LV161284DL	LV161284		
	330F - DL	Tape and reel	SN74LV161284DLR	LV 101204		
	TSSOP - DGG	Tape and reel	SN74LV161284DGGR	LV161284		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



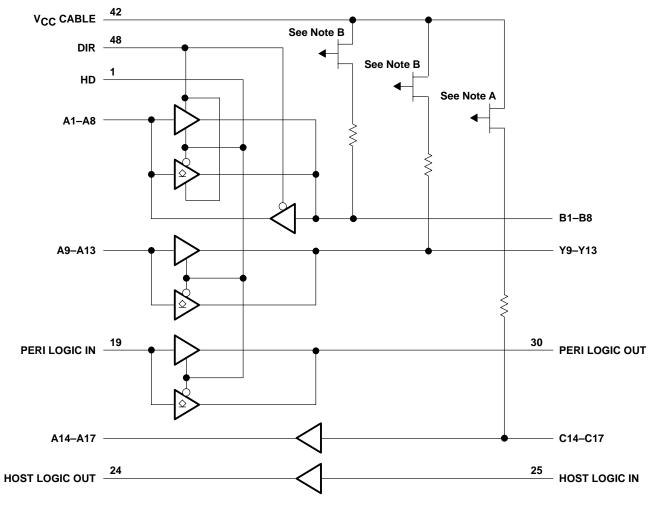
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FUNCTION TABLE

INP	UTS	OUTDUT	Mont
DIR	HD	OUTPUT	MODE
		Open drain	A9-A13 to Y9-Y13 and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	B1-B8 to A1-A8 and C14-C17 to A14-A17
L	Н	Totem pole	B1-B8 to A1-A8, A9-A13 to Y9-Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14-C17 to A14-A17
Н		Open drain	A1-A8 to B1-B8, A9-A13 to Y9-Y13, and PERI LOGIC IN to PERI LOGIC OUT
"	L	Totem pole	C14-C17 to A14-A17
Н	Н	Totem pole	A1-A8 to B1-B8, A9-A13 to Y9-Y13, C14-C17 to A14-A17, and PERI LOGIC IN to PERI LOGIC OUT

logic diagram (positive logic)



NOTES: A. The PMOS prevents backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND.

B. The PMOS prevents backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND. The PMOS is turned off when the associated driver is in the low state.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: V _{CC} CABLE	0.5 V to 7 V
V _{CC}	
Input and output voltage range, V _I and V _O : Cable side (see Notes 1 and 2)	–2 V to 7 V
Peripheral side (see Note 1)0.5 V	to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±200 mA
Output high sink current, I _{SK} (V _O = 5.5 V and V _{CC} CABLE = 5.5 V)	65 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	
DL package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The ac input voltage pulse duration is limited to 40 ns if the amplitude is more negative than -0.5 V.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
V _{CC} CABLE	Supply voltage for the cable side, V _{CC}	; CABLE ≥ V _{CC}	4.5	5.5	V	
Vcc	Supply voltage		4.5	5.5	V	
		A, DIR, HD, and PERI LOGIC IN	V _{CC} ×0.7			
V	High-level input voltage	В	2		V	
VIH	nigri-iever input voltage	C14-C17	2.3		V	
		HOST LOGIC IN	2.6			
		A, DIR, HD, and PERI LOGIC IN		$V_{CC} \times 0.3$		
V _{IL}	Low-level input voltage	В		0.8	V	
		C14-C17		0.8	V	
		HOST LOGIC IN		1.6		
V.	long it voltage	Peripheral side	0	Vсс	V	
VI	Input voltage Open-drain output voltage	Cable side	0	5.5	V	
VO	Open-drain output voltage	B, Y, and PERI LOGIC OUT (HD low)	0	5.5	V	
		B and Y outputs (HD high)		-14		
^I ОН	High-level output current	A outputs and HOST LOGIC OUT		-8	mA	
		PERI LOGIC OUT		-0.5		
		B and Y outputs		14		
loL	Low-level output current	A outputs and HOST LOGIC OUT		8	mA	
		PERI LOGIC OUT		84		
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended V_{CC} CABLE = V_{CC} (unless otherwise noted) operating free-air temperature range,

	PARAMETER	TEST CONDITIONS	TEST CONDITIONS V _{CC} MIN TYP [†] MAX		UNIT			
		V _{thH} – V _{thL} for all inputs except the C inputs and HOST LOGIC IN	4.5 V to 5.5 V	0.4				
ΔV_t	Input hysteresis	V _{thH} - V _{thL} for the HOST LOGIC IN	5 V	0.3			V	
		V _{thH} - V _{thL} for the C inputs	5 V	0.8				
VIK	Input clamp diode voltage	I _I = -18 mA	3 V			-1.2	V	
	B and Y outputs	$I_{OH} = -14 \text{ mA (HD high)}$		3.73				
V	A outputs and HOST LOGIC OUT	$I_{OH} = -8 \text{ mA (HD high)}$	4.5 V	3.8			V	
VOH	A dulputs and 11031 LOGIC COT	I _{OH} = -50 μA		4.4			V	
	PERI LOGIC OUT	$I_{OH} = -0.5 \text{ mA}$	4.5 V	4.45				
	B and Y outputs	I _{OL} = 14 mA				0.77		
Voi	A outpute and HOST LOCIC OUT	I _{OL} = 50 μA	151/			0.1	V	
VOL	A outputs and HOST LOGIC OUT	I _{OL} = 8 mA	4.5 V			0.44	V	
	PERI LOGIC OUT	I _{OL} = 84 mA				0.7		
	Cianuta	VI = VCC	E E V			350	μΑ	
	C inputs	V _I = GND (pullup resistors)	5.5 V			- 5	mA	
t _I	B and C inputs	V _I = 5.5 V or GND	0 to 5.5 V			±5	mA	
	All inputs except the B or C inputs	V _I = V _{CC} or GND	5.5 V			±1	μΑ	
	D outpute	$V_{O} = V_{CC}$	5.5 V			350	μΑ	
	B outputs	V _O = GND (pullup resistors)	5.5 V		-	- 5	mA	
loz	A1–A8	$V_O = V_{CC}$ or GND	5.5 V			±20	μΑ	
	Open-drain Y outputs	V _O = GND (pullup resistors)	5.5 V			– 5	mA	
lo==··	R and V outputs	V _O = 5.5 V	0 to 2 \/			350	μΑ	
IOZPU	B and Y outputs	V _O = GND	0 to 2 V			– 5	mA	
lo====	B and V cutouta	V _O = 5.5 V	2 V to 0			350	μΑ	
IOZPD	B and Y outputs	V _O = GND	∠ v to u			– 5	mA	
	Power-down output leakage, Outputs B1 – B8, Y9 – Y13, and PERI LOGIC OUT	V _O = 5.5 V	0			100	۵	
Power-down input leakage, Inputs C14 – C17 and HOST LOGIC IN		V _I = 5.5 V	0			100	μΑ	
+		$V_I = V_{CC},$ $I_O = 0$	5.5 V			0.8	mA	
^I CC [‡]		$V_I = GND (12 \times pullup)$	0.5 v			70	IIIA	
C _i	All inputs	V _I = V _{CC} or GND	5 V		5		pF	
C _{io}	I/O ports	$V_O = V_{CC}$ or GND	5 V		9		pF	
ZO	Cable side	I _{OH} = –35 mA	5 V		45		Ω	
R pullup	Cable side	V _O = 0 V (in Hi Z)	5 V	1.15		1.65	kΩ	



[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ A maximum current of 170 μ A per pin is added to I_{CC} if the pullup resistor pin is above V_{CC} .

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

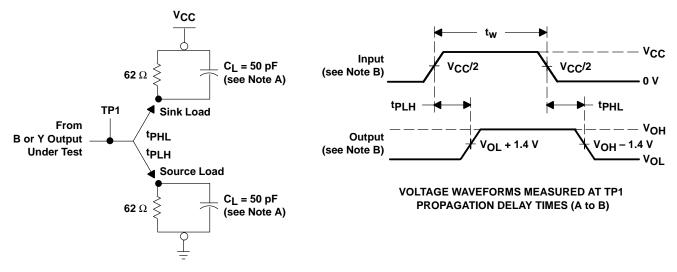
PAR	AMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	мах	UNIT
tPLH	Totom nois	A or B	B or A	2		30	
tPHL	Totem pole	AOIB	B OF A	2		30	ns
tPLH	Totom nole	Α	Y	2		30	ns
tPHL	Totem pole	A	1	2		30	110
^t PLH	Totem pole	С	А	2		30	ns
^t PHL	Totelli pole	C	ζ	2		30	10
^t PLH	Totem pole	PERI LOGIC IN	PERI LOGIC OUT	2		30	ns
^t PHL	Totelli pole	PERI LOGIC IN PERI LOGIC OUT		2		30	110
^t PLH	Totem pole	HOST LOGIC IN	HOST LOGIC OUT	2		30	ns
tPHL	Totelli pole	FIOST LOGIC IN	11031 20010 001	2		30	113
tslew	Totem pole	Cable-sid	e outputs	0.05		0.95	V/ns
t _{en}	Totem pole	HD	B, Y, and PERI LOGIC OUT	2		25	ns
^t dis	Totem pole	HD	B, Y, and PERI LOGIC OUT	2		25	ns
t _{en} -t _{dis}						10	ns
t _{en}		DIR	А	2		25	ns
			А	2		15	
^t dis		DIR	В	2		25	ns
t _r , t _f	Open drain	А	B or Y			30	ns
^t sk(o)		A or B	B or A		1	6	ns

[†] Skew is measured at 1/2 (V_{OH} + V_{OL}) for signals switching in the same direction.

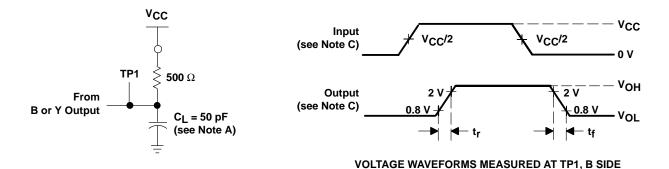
operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER		TEST C	ONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	Outputs enabled	$C_{L} = 0$,	f = 10 MHz	25	pF

PARAMETER MEASUREMENT INFORMATION



SLEW RATE A-TO-B OR A-TO-Y LOAD (Totem Pole)



A-TO-B LOAD OR A-TO-Y LOAD (Open Drain)

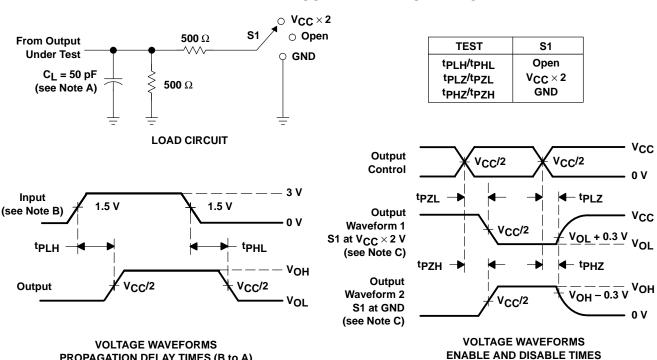
NOTES: A. C_L includes probe and jig capacitance.

- B. Input rise and fall times are 3 ns, 150 ns < pulse duration < 10 μs for both low-to-high and high-to-low transitions. Slew rate is measured between 0.4 V and 1.9 V for the rising edge and between 95% V_{CC} and 50% V_{CC} for the falling edge.
- C. Input rise and fall times are 3 ns. Rise and fall times (open drain) < 120 ns.
- D. The outputs are measured one at a time with one transition per measurement.

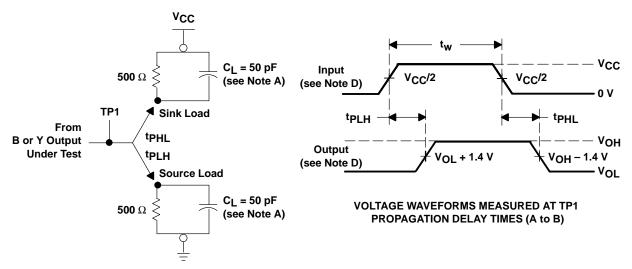
Figure 1. Load Circuits and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION



B-TO-A LOAD (Totem Pole)



A-TO-B LOAD OR A-TO-Y LOAD (Totem Pole)

- NOTES: A. C_I includes probe and jig capacitance.
 - B. Input rise and fall times are 3 ns.

PROPAGATION DELAY TIMES (B to A)

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. Input rise and fall times are 3 ns, 150 ns < pulse duration < 10 μs for both low-to-high and high-to-low transitions.
- E. The outputs are measured one at a time with one transition per measurement.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LV161284DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284
SN74LV161284DGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284
SN74LV161284DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284
SN74LV161284DL.A	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284
SN74LV161284DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284
SN74LV161284DLR.A	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161284

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV161284DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LV161284DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV161284DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LV161284DLR	SSOP	DL	48	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV161284DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LV161284DL.A	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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