

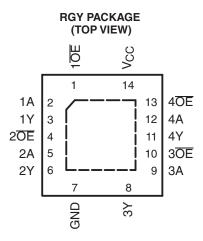
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QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

Check for Samples: SN74LV125A-Q1

FEATURES

- Qualified for Automotive Applications
- 2-V to 5.5-V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation



DESCRIPTION

The SN74LV125A-Q1 quadruple bus buffer gate is designed for 2-V to 5.5-V V_{CC} operation.

This device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | QFN – RGY | Reel of 3000 | SN74LV125AQRGYRQ1 | LV125Q |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



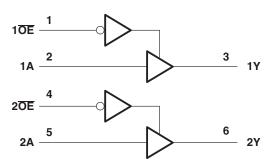
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

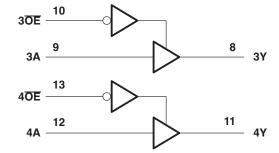


FUNCTION TABLE (EACH BUFFER)

| INPL | OUTPUT | |
|------|--------|---|
| ŌĒ | Α | Y |
| L | Н | Н |
| L | L | L |
| Н | Χ | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)





ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | · · · · · · · · · · · · · · · · · · · | | MIN | MAX | UNIT |
|----------------------|--|-----------------------|------|-----|------|
| V_{CC} | Supply voltage range | | -0.5 | 7 | V |
| VI | V _I Input voltage range ⁽²⁾ | | | | V |
| Vo | Voltage range applied to any output in the high-impeda | -0.5 | 7 | V | |
| Vo | Output voltage range ^{(2) (3)} | | | | V |
| I_{IK} | Input clamp current | V _I < 0 | | -20 | mA |
| I _{OK} | Output clamp current | V _O < 0 | | -50 | mA |
| Io | Continuous output current | $V_O = 0$ to V_{CC} | | ±35 | mA |
| | Continuous current through V _{CC} or GND | | | ±70 | mA |
| θ_{JA} | Package thermal impedance (4) | RGY package | | 47 | °C/W |
| T _{stg} | Storage temperature range | -65 | 150 | °C | |

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ This value is limited to 5.5 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-5.



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RECOMMENDED OPERATING CONDITIONS(1)

| | | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|--|-----------------------|-----------------------|------|--|
| V _{CC} | Supply voltage | | 4.5 | 5.5 | V | |
| | | V _{CC} = 2 V | 1.5 | | | |
| \ / | High level inner college | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | V _{CC} x 0.7 | | V | |
| V_{IH} | High-level input voltage | V _{CC} = 3 V to 3.6 V | V _{CC} x 0.7 | | V | |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | V _{CC} x 0.7 | | | |
| | | V _{CC} = 2 V | | 0.5 | | |
| V | Lauran in mark walka na | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | | V _{CC} x 0.3 | V | |
| V_{IL} | Low-level input voltage | V _{CC} = 3 V to 3.6 V | | V _{CC} x 0.3 | V | |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | | $V_{CC} \times 0.3$ | | |
| V_{I} | Input voltage | | 0 | 5.5 | V | |
| V | Output voltage | High or low state | 0 | V_{CC} | V | |
| v _O | | 3-state | 0 | 5.5 | v | |
| | | V _{CC} = 2 V | | -50 | | |
| | High lovel output ourrent | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | | -2 | mA | |
| I _{OH} | High-level output current | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ | | -8 | mA | |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | | -16 | | |
| | | $V_{CC} = 2 V$ | | 50 | | |
| | Low lovel output ourrent | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | | 2 | A | |
| l _{OL} | Low-level output current | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ | | 8 | mA | |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | | 16 | | |
| | | V _{CC} = 2.3 V to 2.7 V | | 200 | | |
| Δt/Δν | Input transition rise or fall rate | V _{CC} = 3 V to 3.6 V | | 100 | ns/V | |
| | | V _{CC} = 4.5 V to 5.5 V | | 20 | | |
| T _A | Operating free-air temperature | | -40 | 125 | °C | |

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|------------------|----------------------------------|-----------------|----------------------|-----|------|------|--|
| | I _{OH} = -50 μA | 2 V to 5.5 V | V _{CC} -0.1 | | | | |
| V | $I_{OH} = -2 \text{ mA}$ | 2.3 V | 2 | | | | |
| V _{OH} | $I_{OH} = -8 \text{ mA}$ | 3 V | 2.48 | | | V | |
| | $I_{OH} = -16 \text{ mA}$ | 4.5 V | 3.8 | | | | |
| | I _{OL} = 50 μA | 2 V to 5.5 V | | | 0.1 | | |
| V | I _{OH} = 2 mA | 2.3 V | | | 0.4 | V | |
| V_{OL} | I _{OH} = 8 mA | 3 V | | | 0.44 | | |
| | I _{OL} = 16 mA | 4.5 V | | | 0.55 | | |
| I _I | V _I = 5.5 V or GND | 0 to 5.5 V | | | ±1 | μА | |
| l _{OZ} | $V_O = V_{CC}$ or GND | 5.5 V | | | ±5 | μΑ | |
| I _{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V | | | 20 | μΑ | |
| I _{off} | V_I or $V_O = 0$ to 5.5 V | 0 | | | 5 | μΑ | |
| 6 | V V or CND | 3.3 V | 3.3 V 1.6 | | | | |
| C_{i} | $V_I = V_{CC}$ or GND | 5 V | | 1.6 | | pF | |

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM | TO (OUTPUT) | LOAD CAPACITANCE | T _A =25°C | T _{A=} -40°C to 125°C | UNIT |
|--------------------|---------|-------------|-----------------------|----------------------|-----------------------------------|------|
| | (INPUT) | (OUTPUT) | CAFACITANCE | MIN TYP MAX | MIN MAX | |
| t _{pd} | Α | Υ | | 8.7 16.5 | 1 18.5 | ns |
| t _{en} | ŌĒ | Υ | C | 8.8 16.5 | 1 18.5 | ns |
| t _{dis} | ŌĒ | Y | $C_L = 50 \text{ pF}$ | 7.3 18.2 | 1 20.5 | ns |
| t _{sk(o)} | | | | 2 | | ns |

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM | TO (OUTPUT) | LOAD | TA | = 25° | С | T _{A=} -40°C to 1 | 125°C | UNIT |
|--------------------|---------|-------------|-----------------------|-----|-------|------|-------------------------------|-------|------|
| | (INPUT) | (OUTPUT) | CAPACITANCE | MIN | TYP | MAX | MIN | MAX | |
| t _{pd} | А | Υ | | | 6.1 | 11.5 | 1 | 13 | ns |
| t _{en} | ŌĒ | Υ | C 50 pF | | 6.2 | 11.5 | 1 | 13 | ns |
| t _{dis} | ŌĒ | Υ | $C_L = 50 \text{ pF}$ | | 5.5 | 13.2 | 1 | 15 | ns |
| t _{sk(o)} | | | | | | 1.5 | | | ns |

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM | TO | LOAD CAPACITANCE | T _A =25°C | | T _{A=} -40°C to 1 | 25°C | UNIT |
|--------------------|---------|----------|-----------------------|----------------------|-----|-------------------------------|------|------|
| (INPL | (INPUT) | (OUTPUT) | CAPACITANCE | MIN TYP M | AX | MIN | MAX | |
| t _{pd} | Α | Υ | | 4.3 | 7.5 | | 10 | ns |
| t _{en} | OE | Υ | C 50 pF | 4.4 | 7.1 | | 10 | ns |
| t _{dis} | OE | Υ | $C_L = 50 \text{ pF}$ | 4 | 8.8 | | 11 | ns |
| t _{sk(o)} | | | | | 1 | | | ns |

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NOISE CHARACTERISTICS(1)

 V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

| | | MIN | TYP | MAX | UNIT |
|--------------------|---|------|------|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic V _{OL} | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V _{OL} | | -0.3 | -0.8 | V |
| V _{OH(V)} | Quiet output, minimum dynamic V _{OH} | | 3 | | V |
| V _{IH(D)} | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

⁽¹⁾ Characteristics are for surface-mount packages only.

OPERATING CHARACTERISTICS

 $T_A = 25^{\circ}C$

| PARAMETER | | | TEST CC | NDITIONS | V _{CC} | TYP | UNIT | |
|---|-----------------|-----------------|--------------|------------|-----------------|------|------|----|
| C Power discinstion conscitones | | Outpute enabled | $C_{L} = 50$ | f = 10 | 3.3 V | 15.5 | ۲ | |
| C _{pd} Power dissipation capacitance | Outputs enabled | pF, | - <u>L</u> | - <u>-</u> | MHz | 5 V | 17.6 | pF |

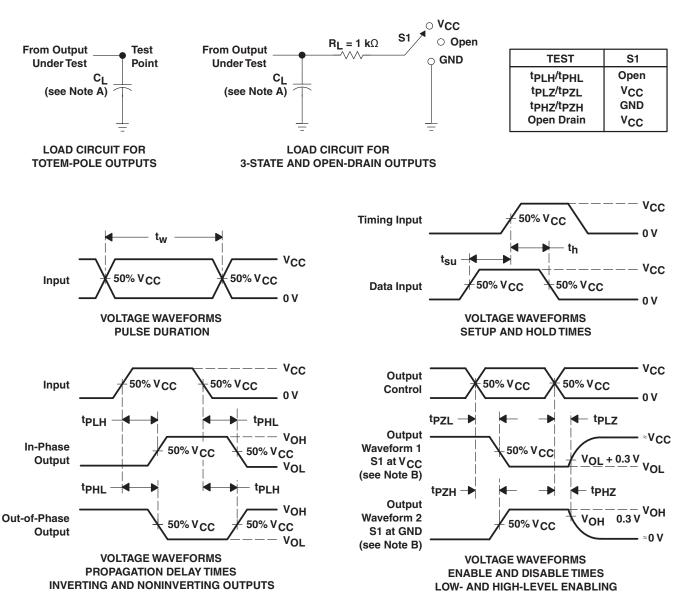
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristicsPRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

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PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|-----------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|------------------|
| SN74LV125AQRGYRQ1 | Active | Production | VQFN (RGY) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | LV125Q |
| SN74LV125AQRGYRQ1.A | Active | Production | VQFN (RGY) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | LV125Q |
| SN74LV125AQRGYRQ1.B | Active | Production | VQFN (RGY) 14 | 2000 LARGE T&R | - | Call TI | Call TI | -40 to 125 | |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV125A-Q1:

Catalog: SN74LV125A

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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NOTE: Qualified Version Definitions:

 $_{\bullet}$ Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74LV125AQRGYRQ1 | VQFN | RGY | 14 | 2000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) | |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|--|
| SN74LV125AQRGYRQ1 | VQFN | RGY | 14 | 2000 | 353.0 | 353.0 | 32.0 | |

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

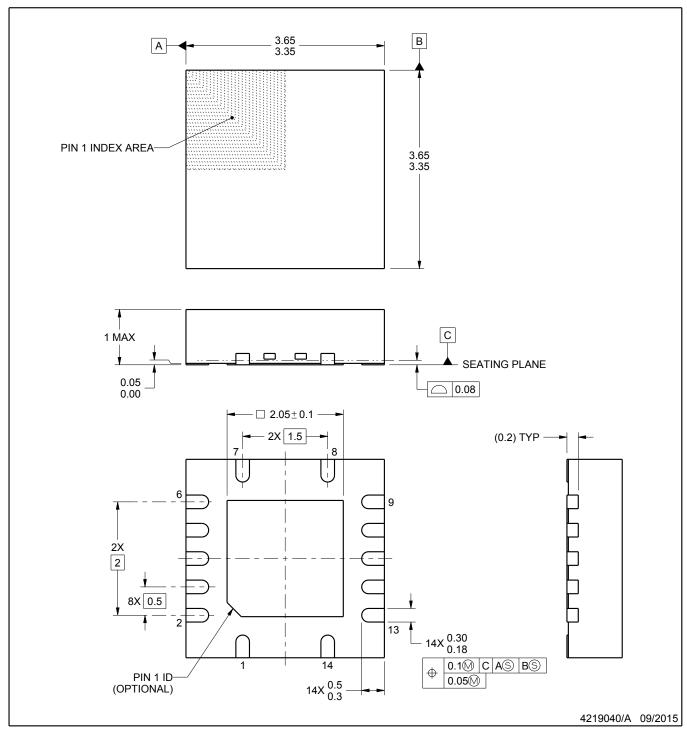
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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