







SN74LV125A SCES1240 - DECEMBER 1997 - REVISED MAY 2022

SN74LV125A Quadruple Bus Buffer Gates With 3-State Outputs

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{nd} of 6 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2.3 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- **ESD Protection Exceeds JESD 22**
 - 4000-V Human-Body Model
 - 200-V Machine Model
 - 2000-V Charged-Device Model

2 Applications

- Flow Meters
- Solid State Drives (SSDs): Enterprise
- Power Over Ethernet (PoE)
- Programmable Logic Controllers
- Motor Drives and Controls
- Electronic Points of Sale

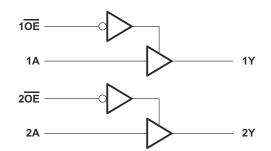
3 Description

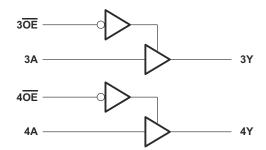
The SN74LV125A quadruple bus buffer gate is designed for 2-V to 5.5-V V_{CC} operation.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
	DGV (TVSOP, 14)	3.60 mm x 4.40 mm
	D (SOIC, 14)	8.65 mm × 3.90 mm
SN74LV125A	NS (SO, 14)	10.20 mm x 5.30 mm
	DB (SSOP, 14)	6.20 mm x 5.30 mm
	PW (TSSOP, 14)	5.00 mm x 4.40 mm

For all available packages, see the orderable addendum at the end of the data sheet.





Simplified Schematic

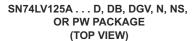


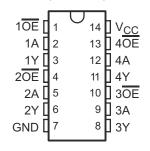
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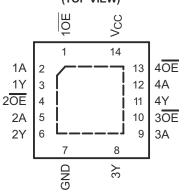


5 Pin Configuration and Functions





SN74LV125A ... RGY PACKAGE (TOP VIEW)



Pin Functions

	PIN	TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME	ITPE	DESCRIPTION
1	1 OE	I	Output Enable 1, Active Low
2	1A	1	1A Input
3	1Y	0	1Y Output
4	2 OE	I	Output Enable 2, Active Low
5	2A	I	2A Input
6	2Y	0	2Y Output
7	GND	_	Ground Pin
8	3Y	0	3Y Output
9	3A	I	3A Input
10	3 OE	I	Output Enable 3, Active Low
11	4Y	0	4Y Output
12	4A	I	4A Input
13	4 OE	1	Output Enable 4, Active Low
14	V _{CC}	_	Power Pin

⁽¹⁾ Signal Types: I = Input, O = Output, I/O = Input or Output.



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN ⁽¹⁾	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
VI	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Voltage range applied to any output in the high-in	npedance or power-off state ⁽²⁾	-0.5	7	V
Vo	Output voltage range ^{(2) (3)}		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V _{CC} or GND	·		±70	mA
Tj	Junction temperature		150	°C	
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MAX	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±4000	
V _(ESD) Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000	V	
		Machine Model (MM)	±200	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ This value is limited to 5.5-V maximum.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74LV125	5A			
			MIN	MAX	UNIT		
V _{CC}	Supply voltage		2	5.5	V		
		V _{CC} = 2 V	1.5				
. ,	Himb lavel in motoralta na	V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V		
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7				
		V _{CC} = 2 V		0.5			
.,	Low lovel input voltage	V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	V		
V_{IL}	Low-level input voltage	w-level input voltage $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ $V_{CC} \times 0.3$		V _{CC} × 0.3	V		
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3			
V _I	Input voltage		0	5.5	V		
V _O	Output voltage	High or low state	0	V _{CC}	V		
v _O		3-state	0	5.5	V		
		V _{CC} = 2 V		-50	μΑ		
ı	High-level output current	V _{CC} = 2.3 V to 2.7 V		-2			
Іон	righ-level output current	V _{CC} = 3 V to 3.6 V		-8	mA		
		V _{CC} = 4.5 V to 5.5 V		-16			
		V _{CC} = 2 V		50	μA		
	Lave lave Laveter of a command	V _{CC} = 2.3 V to 2.7 V		2			
l _{OL}	Low-level output current	V _{CC} = 3 V to 3.6 V		8	mA		
		V _{CC} = 4.5 V to 5.5 V		16			
		V _{CC} = 2.3 V to 2.7 V		200			
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3 V to 3.6 V		100	ns/V		
		V _{CC} = 4.5 V to 5.5 V		20			
T _A	Operating free-air temperature	•	-40	125	°C		

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

				5	SN74LV125	A			
	THERMAL METRIC(1)	D	DB	DGV	N	NS	PW	RGY	UNIT
		14 PINS							
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.7	105.0	127.6	89.2	89.6	119.8	55.0	
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.1	57.5	50.7	47.0	47.2	48.6	67.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.0	52.3	60.5	47.9	48.4	61.5	31.0	
ΨЈТ	Junction-to-top characterization parameter	18.9	19.1	6.1	14.1	14.0	5.7	2.6	°C/W
ΨЈВ	Junction-to-board characterization parameter	46.7	51.8	59.8	47.5	48.1	61.0	31.1	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	11.6	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	T _A :	= 25°C		-40°C to 85°C	-40°C to 1	25°C	UNIT	
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN MA	X MIN	MAX	UNII	
	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1	V _{CC} - 0.1			
V _{OH}	I _{OH} = -2 mA	2.3 V	2			2	2		V	
	I _{OH} = -8 mA	3 V	2.48			2.48	2.48			
	I _{OH} = -16 mA	4.5 V	3.8			3.8	3.8			
	I _{OL} = 50 μA	2 V to 5.5 V			0.1	0	1	0.1		
V _{OL}	I _{OL} = 2 mA	2.3 V			0.4	0	4	0.4	V	
	I _{OL} = 8 mA	3 V			0.44	0.4	4	0.44		
	I _{OL} = 16 mA	4.5 V			0.55	0.5	5	0.55		
l _l	V _I = 5.5 V or GND	0 to 5.5 V			±1	<u> </u>	1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±5	±	5	±5	μA	
I _{cc}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20	2	0	20	μA	
I _{off}	V_I or $V_O = 0$ to 5.5 V	0			5		5	5	μΑ	
C _i	V _I = V _{CC} or GND	3.3 V		1.6					pF	
C _i	AI - ACC OL GIAD	5 V		1.6					ρı	

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

		· .									
PARAMETER	FROM	то	LOAD	Т	T _A = 25°C			-40°C to 85°C		-40°C to 125°C	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{pd}	Α	Y			6.8 ⁽¹⁾	13 ⁽¹⁾	1	15.5	1	17	
t _{en}	ŌĒ	Y	C _L = 15 pF		7 ⁽¹⁾	13 ⁽¹⁾	1	15.5	1	17	ns
t _{dis}	ŌĒ	Y			5.1 ⁽¹⁾	14.7 ⁽¹⁾	1	17	1	18	
t _{pd}	Α	Y			8.7	16.5	1	18.5	1	20	
t _{en}	ŌĒ	Y	$C_1 = 50 \text{ pF}$		8.8	16.5	1	18.5	1	20	ns
t _{dis}	ŌĒ	Y	С[– 30 рі		7.3	18.2	1	20.5	1	21.5	115
t _{sk(o)}						2		2		2	

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range(unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM TO		LOAD	T,	T _A = 25°C			85°C	-40°C to 125°C		UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Y			4.8(1)	8(1)	1	9.5	1	11	
t _{en}	ŌĒ	Y	C _L = 15 pF		4.8(1)	8(1)	1	9.5	1	10.5	ns
t _{dis}	ŌĒ	Y			4.1 ⁽¹⁾	9.7 ⁽¹⁾	1	11.5	1	12.5	
t _{pd}	Α	Y			6.1	11.5	1	13	1	14.5	
t _{en}	ŌĒ	Y	$C_1 = 50 \text{ pF}$		6.2	11.5	1	13	1	14	ns
t _{dis}	ŌĒ	Y	оլ – 30 рі		5.5	13.2	1	15	1	16	115
t _{sk(o)}						1.5		1.5		1.5	

Product Folder Links: SN74LV125A

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM TO		LOAD	TA	T _A = 25°C			85°C	-40°C to	125°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT
t _{pd}	Α	Y			3.4 ⁽¹⁾	5.5 ⁽¹⁾	1	6.5	1	7.5	
t _{en}	ŌĒ	Y	C _L = 15 pF		3.4 ⁽¹⁾	5.1 ⁽¹⁾	1	6	1	7	ns
t _{dis}	ŌĒ	Y			3.2 ⁽¹⁾	6.8 ⁽¹⁾	1	8	1	9	
t _{pd}	Α	Y			4.3	7.5	1	8.5	1	9.5	
t _{en}	ŌĒ	Y	C = 50 pE		4.4	7.1	1	8	1	9	ns
t _{dis}	ŌĒ	Y	$C_L = 50 \text{ pF}$		4	8.8	1	10	1	11	115
t _{sk(o)}						1		1		1	

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics

 V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

	PARAMETER ⁽¹⁾	S	LINIT		
	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.4	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.3	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

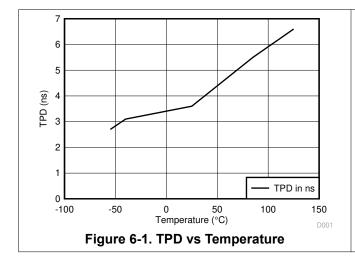
⁽¹⁾ Characteristics are for surface-mount packages only.

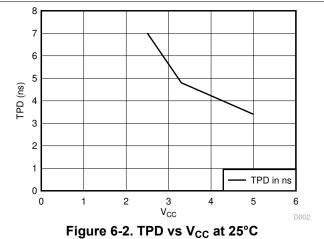
6.10 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER			ONDITIONS	V _{cc}	TYP	UNIT
_	Power dissipation capacitance	Outputs enabled	$C_1 = 50 \text{ pF},$	f = 10 MHz	3.3 V	15.5	
Power dissipation capacitance	Outputs enabled	C _L = 50 pr,	1 - 10 WILIZ	5 V	17.6	p⊦	

6.11 Typical Characteristics

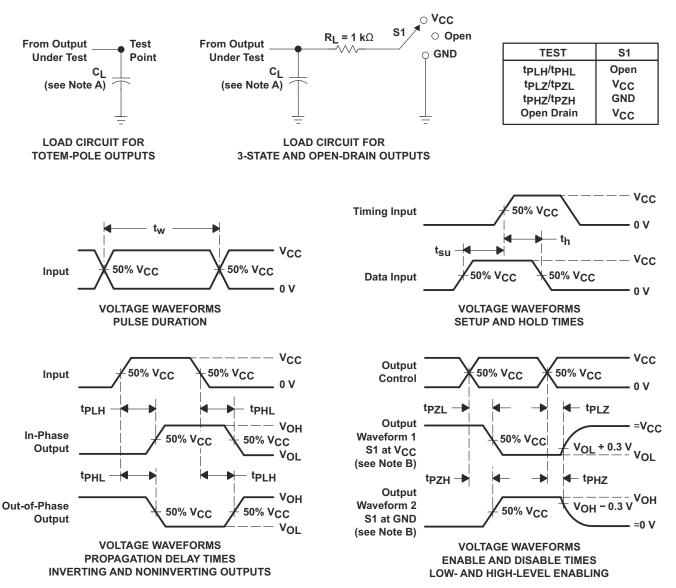






7 Parameter Measurement Information

7.1



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 3 ns. $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. tpLZ and tpHZ are the same as t_{dis}.
- F. tpzL and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit And Voltage Waveforms

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8 Detailed Description

8.1 Overview

The SN74LV125A quadruple bus buffer gate is designed for 2-V to 5.5-V V_{CC} operation.

These devices feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, tie \overline{OE} to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

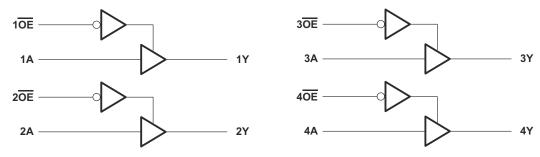


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

- · Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} Feature
 - Supports Live Insertion, Partial Power-Down Mode, and Back-Drive Protection

8.4 Device Functional Modes

Table 8-1. Function Table (Each Buffer)

INPU	TS ⁽¹⁾	OUTPUT ⁽²⁾
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	X	Z

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV125A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs are 5.5-V tolerant at any valid V_{CC} , making it ideal for translating down to V_{CC} .

9.2 Typical Application

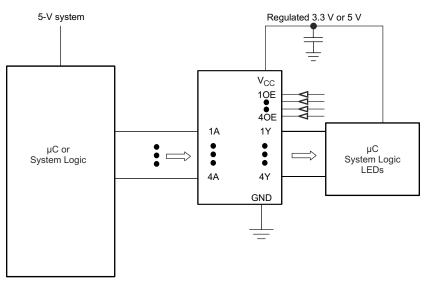


Figure 9-1. Typical Application Schematic

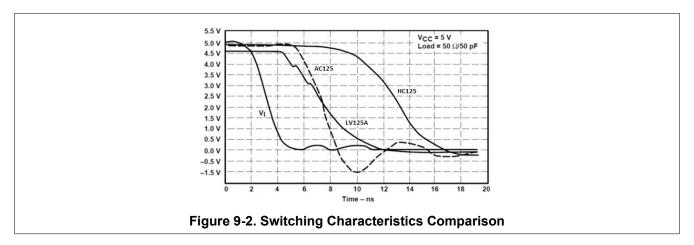
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - For rise time and fall time specifications, see Δt/ΔV in the Section 6.3 table.
 - For specified High and low levels, see V_{IH} and V_{II} in the Section 6.3 table.
- 2. Recommend Output Conditions
 - Load currents should not exceed 35 mA per output and 70 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 6.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

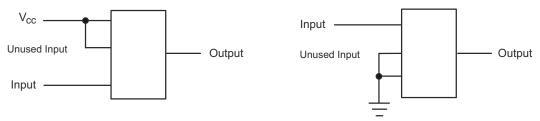


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN74LV125A	SN74LV125A Click here		Click here	Click here	Click here	

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LV125AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	LV125A
SN74LV125ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125ADBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125ADGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125ADGVR.A	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125AN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LV125AN
SN74LV125AN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LV125AN
SN74LV125ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV125A
SN74LV125ANSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV125A
SN74LV125APW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	LV125A
SN74LV125APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRE4	Active	Production	TSSOP (PW) 14	2000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRE4	Active	Production	TSSOP (PW) 14	2000 null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRE4.A	Active	Production	TSSOP (PW) 14	2000 null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRE4.A	Active	Production	TSSOP (PW) 14	2000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRG4	Active	Production	TSSOP (PW) 14	2000 null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRG4	Active	Production	TSSOP (PW) 14	2000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRG4.A	Active	Production	TSSOP (PW) 14	2000 null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWRG4.A	Active	Production	TSSOP (PW) 14	2000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LV125APWT	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	LV125A
SN74LV125ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV125A
SN74LV125ARGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV125A
SN74LV125ARGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV125A

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV125A:

Automotive: SN74LV125A-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV125ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV125ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV125ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV125APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV125ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV125ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV125ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV125ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV125ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV125APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV125ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV125AN.A	N	PDIP	14	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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