SDLS175 p2536, JANUARY 1980 - REVISED MARCH 1988

- · Will Not Trigger from Clear
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- . Overriding Clear Teminates Output Pulse
- 'LS422 Has Internal Timing Resistor

description

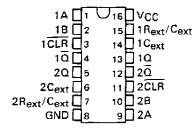
The 'LS422 and 'LS423 are identical to 'LS122 and 'LS123 except they cannot be triggered via clear.

These d-c triggered multivibrators feature output-pulse-width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The 'LS422 contains an internal timing resistor that allows the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

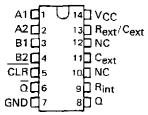
The 'LS422 and 'LS423 have enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond. The 'LS422 Rint is nominally 10 k ohms.

The SN54LS422 and SN54LS423 are characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LS422 and SN74LS423 are characterized for operation from 0°C to 70°C.

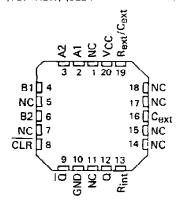
SN54LS423...J OR W PACKAGE SN74LS423...D OR N PACKAGE (TOP VIEW) (SEE NOTES 1 THRU 4)



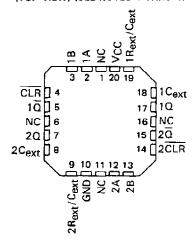
SN54LS422 ... J OR W PACKAGE SN74LS422 ... D OR N PACKAGE (TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS422 . . . FK PACKAGE (TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS423 . . . FK PACKAGE (TOP VIEW) (SEE NOTES 1 THRU 4)



- NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
 - 2. To use the internal timing resistor of 'LS422, connect $\rm R_{int}$ to $\rm V_{CC}$
 - For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circulted.
 - 4. To obtain variable pulse widths, connect an external variable resistance between Rint or Reaxt/Cext and VCC.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

description (continued)

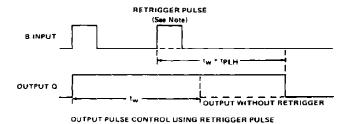
'LS422 FUNCTION TABLE

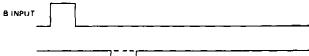
'LS423
FUNCTION TABLE

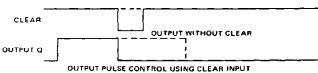
	OUT	צדטי				
CLEAR	Αı	A2	81	82	o	ā
L	Х	Х	×	×	L	Н
×	H	н	X	×	LŤ	нt
×	x	X	L	Х	LŤ	нt
×	×	×	X	L	L.	нŤ.
н	Ĺ.	Х	†	н	$\mathbf{\Gamma}$	Г
н	L	×	н	1	л	П
H	×	Ł	;	н	Λ	U
11	×	L	н	٠	л	ъ
	14	ţ	н	н	Л	¥
, н	1	1	н	Н	л	IJ
14	.	+4	H	н	Л	u.

INPL	JTS	OUTPUTS				
CLEAR	A	8	Q	ã		
L	×	×	L	H		
×	Н	×	LŤ	нt		
х	×	L	LŤ	нī		
н	L	t	J.	Л,		
н		н	л	ਪੁ		

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.



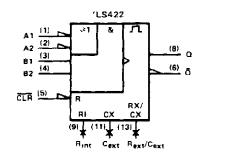


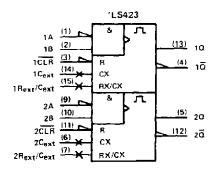


NOTE: Retrigger pulses starting before 0.22 C_{ext} (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output pulse will remain unchanged.

FIGURE 1-TYPICAL INPUT/OUTPUT PULSES

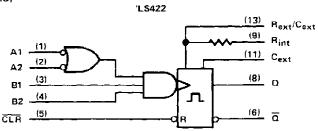
logic symbols†



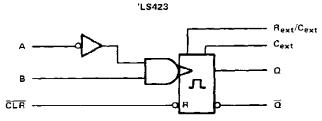


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

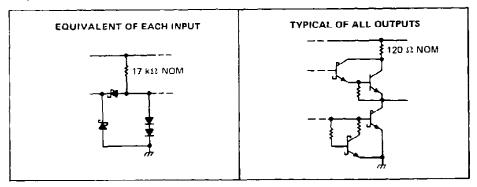


Rint is nominally 10 k ohms



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs





SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

		SN54LS'			SN74LS'			
	MIN	MOM	MAX	MIN	NOM	MAX	UNIT	
Supply voltage, VCC	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, IOH			-400			-40 0	μΑ	
Low-level output current, IOL			4			8	mΑ	
Pulse width, tw	40			40			ns	
External timing resistance, Rext	5		180	5		260	kΩ	
External capacitance, C _{ext}	No	restrict	ion	No	No restriction			
Wiring capacitance at Rext/Cext terminal			50		-	50	ρF	
Operating free-air temperature, TA	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	75	ST CONDITIONS†			SN54LS	;		SN74LS	·	UNIT
	FARAMETER	16:	ST COMOLITORS		MIN	TYP‡	MAX	MIN	TYP‡	MAX	ואוט
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage			·	1		0.7			0.8	V
VIK	Input clamp voltage	VCC = MIN.	l _I = -18 mA				-1.5			-1.5	V
Voн	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max	V _{IH} = 2 V, I _{OH} = 400 μA		2,5	3,5		2.7	3.5		V
V _Q L	Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max	V _{IH} = 2 V,	IOL = 4 mA		0,25	0.4		0.25 0.35	0.4 0.5	V
f _f	Input current at maximum input voltage	VCC = MAX,	V ₁ = 7 V				0.1			0.1	mΔ
ΉΗ	High-level input current	V _{CC} = MAX,	V ₁ = 2.7 V				20			20	μΑ
ΉL	Low-level input current	VCC = MAX,	V ₁ ≈ 0.4 V				-0.4			-0.4	mA
los	Short-circuit output current \$	V _{CC} = MAX			-20		-100	-20		-100	mA
lcc	Supply current (quiescent or triggered)	VCC = MAX,	See Note 6	'LS422 'LS423		6 12	11 20		6 12	11 20	mΑ

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. To measure VOH at Q, VOL at Q, or IOS at Q, ground Rext/Cext, apply 2 V to B and clear, and pulse A from 2 V to 0 V.

switching characteristics, VCC = 5 V, TA = 25°C, see note 7

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CON	MIN	TYP	MAX	UNIT	
	Α		_ ·- ·- ·- ·- ·			23	3 3	
tPLH -	8 Q					23	44	ns .
		C -0	B - E 1-O		32	45		
tPHL -	В		C _{ext} = 0, C _L = 15 pF,	$R_{ext} = 5 k\Omega,$ $R_{L} = 2 k\Omega$		34	56	ns ·
t _{PHL}		Q	C[* 15 pF,			20	27	
tPLH .	Clear	Q				28	45	ns:
twQ (min)	A or B	α				116	200	ns
Dw ¹	A or B	a	C _{ext} = 1000 pF, C _L = 15 pF,	$R_{ext} = 10 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$	4	4.5	5	μs

 $[\]P_{t_{\mathbf{WQ}}} = \text{width of pulse output Q.}$

NOTE 7: Load circuits and voltage waveforms are shown in Section 1.



 $^{^{\}ddagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

[§] Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

^{6.} With all outputs open and 4.5 V applied to all data and clear inputs, ICC is measured after a momentary ground, then 4.5 V, is applied to clock

TYPICAL APPLICATION DATA FOR 'LS422, 'LS423[†]

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{\rm ext} \leq 1000\,$ pF, use Figure 3. For $C_{\rm ext}$ between 0.1 nF and 1 μ F, the pulse width may be defined as:

with K obtained from Figure 4.

When $C_{\text{ext}} \ge 1 \,\mu\text{F}$, the output pulse width is defined as:

$$t_W \approx 0.33 \text{-RT} \cdot C_{ext}$$

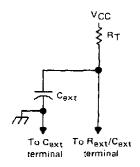
Where

RT is in kilohms (internal or external timing resistance)

Cext is in pF

tw is in nanoseconds

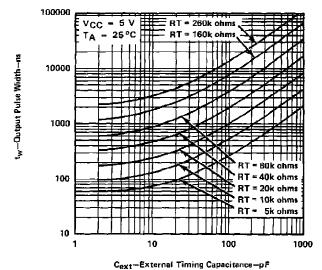
For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS422 and 'LS423, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.



TIMING COMPONENT CONNECTIONS FIGURE 2

'LS422, 'LS423 TYPICAL OUTPUT PULSE WIDTH vs

EXTERNAL TIMING CAPACITANCE

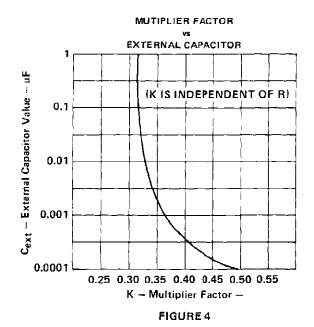


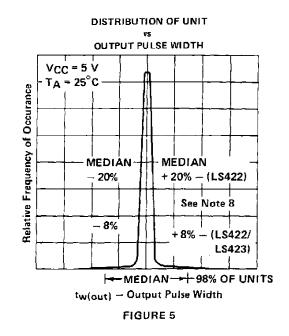
[†] This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 3

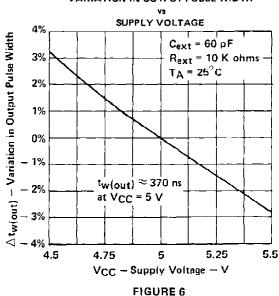


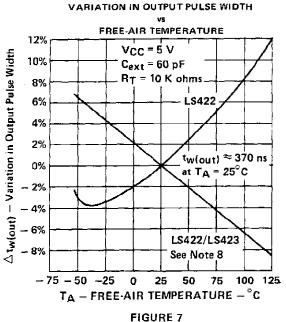
TYPICAL APPLICATION DATA FOR 'LS422, 'LS423 †





VARIATION IN OUTPUT PULSE WIDTH





NOTE 8: For the LS422, the internal timing resistor, $R_{\rm int}$ was used. For the LS422/423, an external timing resistor was used for $R_{\rm T}$. † Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS422 and SN54LS423 only.

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LS423D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS423
SN74LS423D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS423
SN74LS423N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS423N
SN74LS423N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS423N
SN74LS423NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS423
SN74LS423NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS423

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
L	SN74LS423NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
I	SN74LS423NSR	SOP	NS	16	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS423D	D	SOIC	16	40	507	8	3940	4.32
SN74LS423D.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS423N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS423N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS423N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS423N.A	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOP



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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