

SNx4HCT02 Quadruple 2-Input Positive-Nor Gates

1 Features

- Operating voltage range of 4.5V to 5.5V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 20-μA max I_{CC}
- Typical $t_{pd} = 10\text{ns}$
- $\pm 4\text{-mA}$ output drive at 5V
- Low input current of 1μA max
- Inputs are TTL-Voltage compatible

2 Description

These devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCT02D	SOIC (14)	8.65 mm × 3.90 mm
SN74HCT02N	PDIP (14)	19.31 mm × 6.35 mm
SN74HCT02NSR	SO (14)	10.20 mm × 5.30 mm
SN74HCT02PW	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



Table of Contents

1 Features	1	7.2 Functional Block Diagram.....	7
2 Description	1	7.3 Device Functional Modes.....	7
3 Revision History	2	8 Power Supply Recommendations	8
4 Pin Configuration and Functions	3	9 Layout	8
5 Specifications	4	9.1 Layout Guidelines.....	8
5.1 Absolute Maximum Ratings.....	4	10 Device and Documentation Support	9
5.2 Recommended Operating Conditions ⁽¹⁾	4	10.1 Documentation Support.....	9
5.3 Thermal Information.....	4	10.2 Receiving Notification of Documentation Updates.....	9
5.4 Electrical Characteristics.....	5	10.3 Support Resources.....	9
5.5 Switching Characteristics.....	5	10.4 Trademarks.....	9
5.6 Operating Characteristics.....	5	10.5 Electrostatic Discharge Caution.....	9
6 Parameter Measurement Information	6	10.6 Glossary.....	9
7 Detailed Description	7	11 Mechanical, Packaging, and Orderable Information	9
7.1 Overview.....	7		

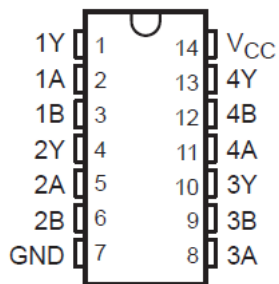
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

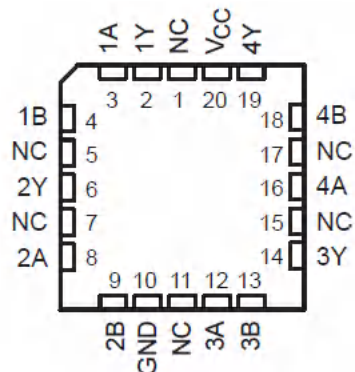
Changes from Revision F (February 2022) to Revision G (October 2022)	Page
• Increased R θ JA for packages: D (86 to 138.7); N (80 to 67); NS (76 to 93.3); PW (113 to 120.1)	4

Changes from Revision E (July 2003) to Revision F (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

4 Pin Configuration and Functions



D, N, NS, PW, J or W Package
14-Pin SOIC, PDIP, SO, TSSOP, CDIP, or CFP
Top View



FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})^{(2)}$		± 20	mA
I_{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})^{(2)}$		± 20	mA
I_O	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		± 25	mA
	Continuous current through V_{CC} or ground current			± 50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HCT02 ⁽²⁾			SN74HCT02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time				500			500	ns
T_A	Operating free-air temperature		-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number [SCBA004](#).
- (2) SN54HCT02 is in product preview.

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	138.7	67	93.3	120.1	°C/W
$R_{\theta JC} \text{ (top)}$	Junction-to-case (top) thermal resistance	93.8	55	50.9	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	46.7	53.8	63.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	49.1	35.1	17.8	6.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.3	46.5	53.3	62.5	°C/W
$R_{\theta JC} \text{ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	T _A = 25°C			SN54HCT00 ⁽³⁾		SN74HCT00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage	I _{OH} = –20 µA	4.5	4.4	4.499		4.4		4.4		V
		I _{OH} = –4 mA		3.98	4.3		3.7		3.84		
V _{OL}	Low-level output voltage	I _{OL} = 20 µA	5.5		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA			0.17	0.26		0.4		0.33	
I _I	Input hold current	V _I = V _{CC} or 0	5.5		±0.1	±100		±1000		±1000	nA
I _{CC}	Supply current	V _I = V _{CC} or 0. I _O = 0	5.5			2		40		20	µA
ΔI _{CC} ⁽²⁾	Supply-current change	One input at 0.5V or 2.4 V, Other inputs at 0 or V _{CC}	5.5		1.4	2.4		3		2.9	mA
C _i	Input capacitance		4.5 to 5.5		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

(3) SN54HCT02 is in product preview.

5.5 Switching Characteristics

C_L = 50 pF. See [Parameter Measurement Information](#)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V _{CC} (V)	T _A = 25°C			SN54HCT02 ⁽¹⁾		SN74HCT00		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Propagation delay	A or B	Y	4.5		11	20		30		25	ns
				5.5		10	18		27		22	
t _t	Transition time		Y	4.5		9	15		22		19	ns
				5.5		8	14		20		17	

(1) SN54HCT02 is in product preview.

5.6 Operating Characteristics

T_A = 25°C

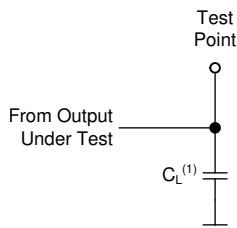
		Test Conditions	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	20	pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

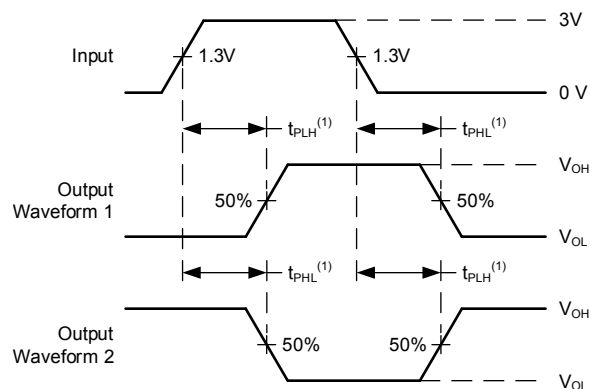
For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

These devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

7.2 Functional Block Diagram



7.3 Device Functional Modes

**Table 7-1. Function Table
(each gate)**

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCT02D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	HCT02
SN74HCT02DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HCT02
SN74HCT02DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT02
SN74HCT02DRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT02
SN74HCT02DRG4.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT02
SN74HCT02DT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	HCT02
SN74HCT02N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT02N
SN74HCT02N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT02N
SN74HCT02NE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT02N
SN74HCT02NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT02
SN74HCT02NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT02
SN74HCT02NSR.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT02
SN74HCT02PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	HT02
SN74HCT02PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HT02
SN74HCT02PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT02
SN74HCT02PWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT02
SN74HCT02PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT02
SN74HCT02PWT	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	HT02

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT02DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT02DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT02NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HCT02PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74HCT02PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT02PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT02PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT02PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT02DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCT02DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCT02NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HCT02PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74HCT02PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HCT02PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HCT02PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT02PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT02N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT02N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT02N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT02N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT02NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT02NE4	N	PDIP	14	25	506	13.97	11230	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



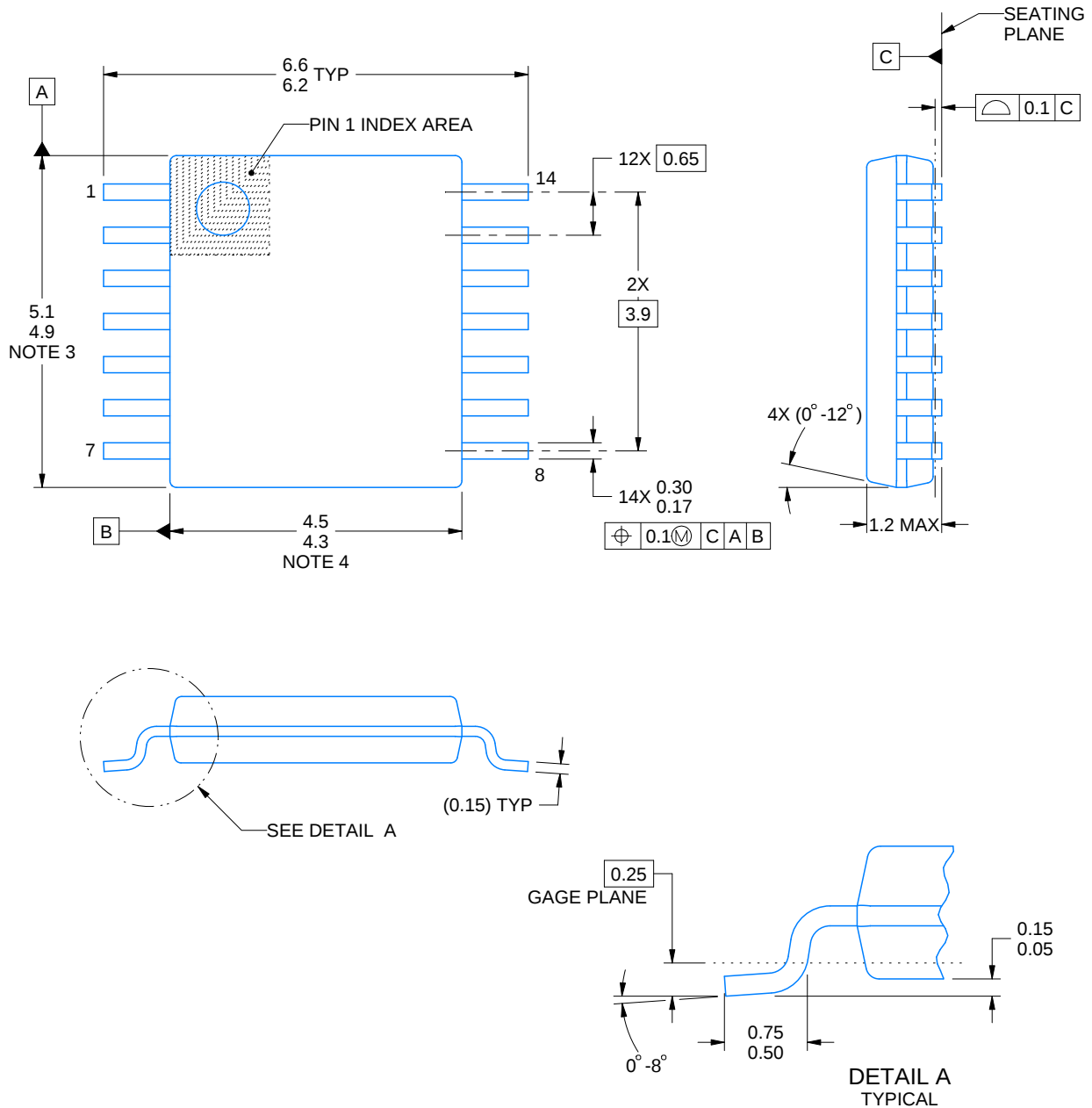
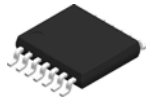
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated