







SN74HCS594-Q1 SCLS807E - JUNE 2020 - REVISED JULY 2023

SN74HCS594-Q1 Automotive 8-Bit Shift Register With Schmitt-Trigger Inputs and **Output Registers**

1 Features

- AEC-Q100 Qualified for automotive applications:
 - Device temperature grade 1: –40°C to +125°C, T_A
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C6
- Available in wettable flank QFN (WBQB) package
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input
- Low power consumption:
 - Typical I_{CC} of 100 nA
 - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 6 V

2 Applications

- Output expansion
- LED matrix control
- 7-segment display control
- 8-bit data storage

3 Description

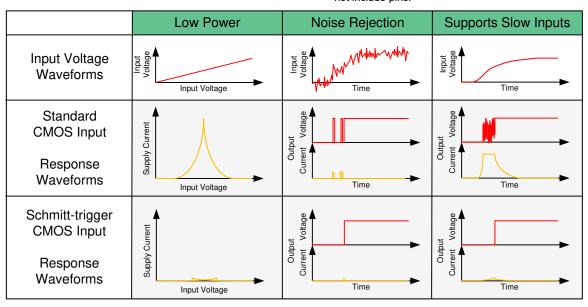
The SN74HCS594-Q1 device contains an 8-bit, serialin, parallel-out shift register that feeds an 8-bit D-type storage register. All inputs include Schmitt-triggers, eliminating any erroneous data outputs due to slowedged or noisy input signals. The storage register has parallel outputs. Separate clocks and direct overriding clear (SRCLR, RCLR) inputs are provided for both the shift and storage register. A serial output (QH') is provided for cascading.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register is one count pulse ahead of the storage register.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
	PW (TSSOP, 16)	5 mm × 6.4 mm	5 mm × 4.4 mm
	D (SOIC, 16)	9.9 mm × 6 mm	9.9 mm × 3.9 mm
SN74HCS594-Q1	BQB (WQFN, 16)	3.5 mm × 2.5 mm	3.5 mm × 2.5 mm
	DYY (SOT-23-THN, 16)	4.2 mm × 2 mm	4.2 mm × 2 mm
	WBQB (WQFN, 16)	3.6 mm × 2.6 mm	3.6 mm × 2.6 mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable
- The body size (length × width) is a nominal value and does not include pins.



Benefits of Schmitt-Trigger Inputs



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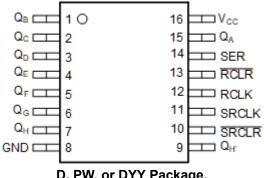
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

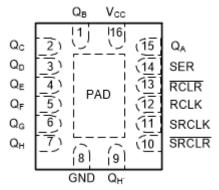
C	nanges from Revision D (December 2021) to Revision E (July 2023)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Updated Package Information table to include package leads	
•	Updated the Function Table	
_	hammed from Basisian C (June 2024) to Basisian B (Basambar 2024)	Dawa
C	hanges from Revision C (June 2021) to Revision D (December 2021)	Page
•	Added WBQB package information to Device Information table	
•	Added WBQB Package, pinout diagram and information to Pin Configuration and Functions	3
•	Added WBQB package to Thermal Information table	
•	Added Wettable Flanks section to Feature Description	
С	hanges from Revision B (March 2021) to Revision C (June 2021)	Page
•	Changed DYY package from product preview to production	
С	hanges from Revision A (February 2021) to Revision B (March 2021)	Page
•	Added DYY package information to Device Information table	1
•	Added DYY Package, pinout diagram and information to Pin Configuration and Functions	
•	Added DYY Package to Thermal Information table	
С	hanges from Revision * (June 2020) to Revision A (February 2021)	Page
•	Added BQB package information to Device Information	1
•	Added BQB Package, information to Pin Configuration and Functions	
	Added BQB Package to Thermal Information table	
•	Audeu DVD Fackage to Thermal Information table	5



5 Pin Configuration and Functions



D, PW, or DYY Package, 16-Pin SOIC, TSSOP, or SOT (Top View)



BQB or WBQB Package, 16-Pin WQFN (Top View)

Pin Functions

PIN		TYPE ⁽²⁾	DESCRIPTION			
NAME	NO.	ITPE(-)	DESCRIPTION			
Q _B	1	0	Q _B output			
Q _C	2	0	Q _C output			
Q _D	Q _D 3 Q _E 4		Q _D output			
Q _E			Q _E output			
Q _F	5	0	Q _F output			
Q_G	6	0	Q _G output			
Q _H	7	0	Q _H output			
GND	8	_	Ground			
Q _H '	9	0	Serial output, can be used for cascading			
SRCLR	10	I	Shift register clear, active low			
SRCLK	11	I	Shift register clock, rising edge triggered			
RCLK	12	I	Output register clock, rising edge triggered			
RCLR	13	I	Storage register clear, active low			
SER	14	I	Serial input			
Q _A	15	0	Q _A output			
V _{CC}	V _{CC} 16		Positive supply			
Thermal Pad ⁽¹⁾		_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.			

- (1) BQB and WBQB Package, only.
- (2) I = input, O = output



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$		±20	mA
I _{OK}	Output clamp current ⁽²⁾	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$		±20	mA
Io	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC}	or GND		±70	mA
TJ	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±4000	V
V(ESD)	Liectiostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	V

⁽¹⁾ AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
VI	Input voltage	0		V _{CC}	V
Vo	Output voltage	0		V _{CC}	V
T _A	Ambient temperature	-40		125	°C

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⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ Specified by design.



6.4 Thermal Information

	SN74HCS594-Q1						
	THERMAL METRIC ⁽¹⁾	PW (TSSOP)	D (SOIC)	BQB (WQFN)	DYY (SOT)	WBQB (WQFN)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.2	122.2	108.4	186.2	97.3	°C/W
R _θ JC(top)	Junction-to-case (top) thermal resistance	78.8	80.9	77.3	109.1	93.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	85.8	80.6	74.4	111.0	66.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.7	40.4	12.6	18.0	14.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85.5	80.3	74.5	110.9	66.4	°C/W
R _θ JC(bot)	Junction-to-case (bottom) thermal resistance	N/A	N/A	54.3	N/A	44.3	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

	PARAMETER	TEST CO	NDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
				2 V	0.7		1.5	
V _{T+}	Positive switching threshold			4.5 V	1.7		3.15	V
				6 V	2.1		4.2	
				2 V	0.3		1.0	
V _{T-}	Negative switching threshold			4.5 V	0.9		2.2	V
				6 V	1.2		3.0	
				2 V	0.2		1.0	
ΔV_T	Hysteresis (V _{T+} - V _{T-}) ⁽¹⁾			4.5 V	0.4		1.4	v
				6 V	0.6		1.6	
			I _{OH} = -20 μA	2 V to 6 V	V _{CC} - 0.1	V _{CC} - 0.002		
V _{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I _{OH} = -6 mA	4.5 V	4.0	4.3		V
			I _{OH} = -7.8 mA	6 V	5.4	5.75		
			I _{OL} = 20 μA	2 V to 6 V		0.002	0.1	
V _{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I _{OL} = 6 mA	4.5 V		0.18	0.30	V
			I _{OL} = 7.8 mA	6 V		0.22	0.33	
II	Input leakage current	$V_I = V_{CC}$ or 0	•	6 V		±100	±1000	nA
I _{CC}	Supply current	$V_I = V_{CC}$ or 0, I_C	_D = 0	6 V		0.1	2	μA
Ci	Input capacitance			2 V to 6 V			5	pF

(1) Specified by design.



6.6 Timing Characteristics

C₁ = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

	Operating free-air temperature (T _A)					e (T _A)		
	PARAMETER		Vcc	25°C	;	-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	
			2 V		32		17	
clock	Clock frequency		4.5 V		100		54	
			6 V		115		68	
			2 V	8		12		
		SRCLK or RCLK high or low	4.5 V	6		7		
	Pulse duration	riigii oi iow	6 V	6		7		
w	Pulse duration		2 V	7		12		ns
		SRCLR or RCLR low	4.5 V	6		7		
		low	6 V	6		7		
			2 V	11		16		
		SER before SRCLK↑	4.5 V	4		7		
		OROLR	6 V	4		5		
			2 V	15		24		
		SRCLK↑ before RCLK↑	4.5 V	5		9		
		TOEK!	6 V	5		7		
			2 V	16		27		
su	Setup time	SRCLR low before RCLK↑	4.5 V	7		10		ns
		T COLIN	6 V	5		8		
		SRCLR high	2 V	5		9		
		(inactive) before	4.5 V	3		5		
		SRCLK↑	6 V	3		4		
		RCLR high	2 V	8		12		
		(inactive) before	4.5 V	4		5		-
		RCLK↑	6 V	3		4		
			2 V	0		0		
า	Hold time	SER after SRCLK↑	4.5 V	0		0		ns
			6 V	0		0		



6.7 Switching Characteristics

 C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

					Op	Operating free-air temperature (T _A)					
	PARAMETER		FROM TO	o v _{cc}		25°C			-40°C to 125°C		
					MIN	TYP	MAX	MIN	TYP	MAX	
				2 V	32			17			
f _{max} Max switching frequency			4.5 V	100	,		54			MHz	
				6 V	115			68			
				2 V		19	30			45	
t _{pd}		SRCLK	Q _H '	4.5 V		7	11			17	
	Propagation delay			6 V		6	9			12	ns
		RCLK	RCLK Q _A - Q _H	2 V		19	30			45	
				4.5 V		7	11			17	
				6 V		6	9			12	
				2 V		18	27			55	
		SRCLR	Q _{H'}	4.5 V		7	11			17	1
	Propagation delay			6 V		6	9			15	
t _{PHL}	Fropagation delay			2 V		18	27			55	ns
		RCLR	Q _A - Q _H	4.5 V		7	11			17	
				6 V		6	9			15	
				2 V			9			16	
t _t	Transition-time	me /	Any output	4.5 V		,	5			9	ns
				6 V			4			8	

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_{\Delta} = 25^{\circ}$ C (unless otherwise noted).

OVCI O	ociating nee an temperature	range, typical values measure	a at 1A - 20	O (dilicos otriciwise rioted	<i>)</i> ·	
PARAMETER		TEST CONDITIONS	V _{CC}	MIN TYP	MAX	UNIT
C _{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V	40		pF



6.9 Typical Characteristics

 $T_A = 25^{\circ}C$

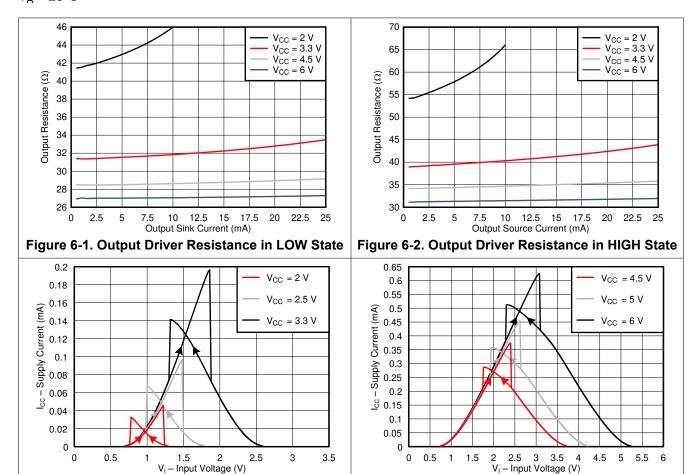


Figure 6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply

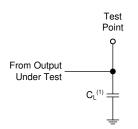
Figure 6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



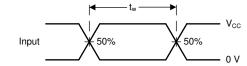


Figure 7-2. Voltage Waveforms, Pulse Duration

(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for Push-Pull Outputs

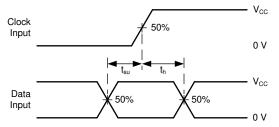
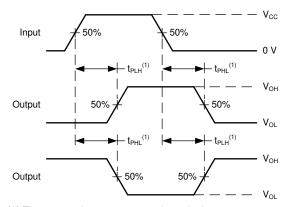
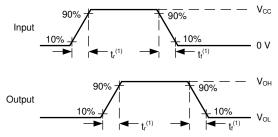


Figure 7-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 7-4. Voltage Waveforms Propagation Delays



(1) The greater between t_{r} and t_{f} is the same as t_{t} .

Figure 7-5. Voltage Waveforms, Input and Output Transition Times



8 Detailed Description

8.1 Overview

The SN74HCS594-Q1 is an 8-bit shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register. All inputs include Schmitt-triggers allowing for slow input transitions and providing more noise margin.

8.2 Functional Block Diagram

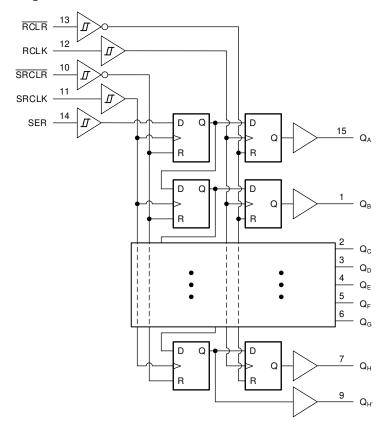


Figure 8-1. Logic Diagram (Positive Logic) for SN74HCS594-Q1

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V \div I$).

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The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

8.3.3 Clamp Diode Structure

As shown in Figure 8-2, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

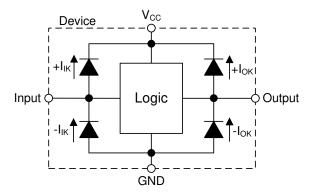


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

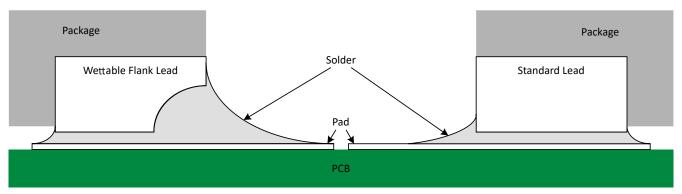


Figure 8-3. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 8-3, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.



8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74HCS594-Q1.

Table 8-1. Function Table

	Table 0-1. I diletion Table										
		INPUTS(1)		FUNCTION						
SER	SRCLK	SRCLR	RCLK	RCLR	IONOTION						
Х	Х	Х	Х	L	Output register is cleared						
Х	Х	L	Х	Х	Internal shift register is cleared						
H/L	1	Н	Х	Х	SER Data is loaded into first shift bit as H/L, data shifts from bit to bit within the internal shift register						
Х	Х	Н	1	Н	Data is transferred from internal shift register to output register						
H/L	1	Н	1	Н	When SRCLK and RCLK are synchronous, Data is transferred from internal shift register to output register, internal shift register first bit is loaded with SER data H/L and data shifts from bit to bit within internal shift register						
Х	↓, L, H	Н	Х	Х	Internal shift register remains in previous state						
Х	Х	Н	↓, L, H	Н	Output register remains in previous state						

⁽¹⁾ H = High Voltage Level, L = Low Voltage Level, X = Do Not Care



9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, the SN74HCS594-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74HCS594-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

There is no practical limitation to how many SN74HCS594-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, both registers need to be cleared. An RC can be connected to the \overline{SRCLR} and \overline{RCLR} pins as shown in the Figure 9-1 to initialize the shift and output registers to all zeros.

9.2 Typical Application

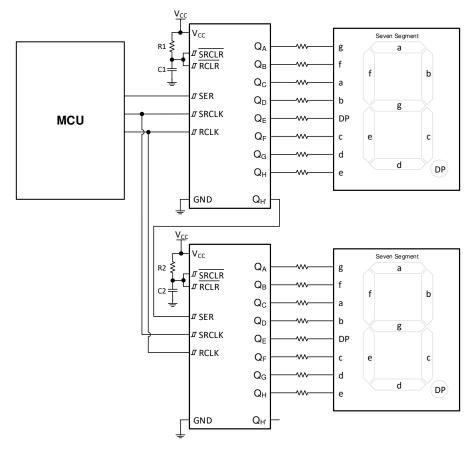


Figure 9-1. Typical Application Block Diagram



9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS594-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS594-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS594-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74HCS594-Q1 can drive a load with total resistance described by $R_L \ge V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear* and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74HCS594-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74HCS594-Q1 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the Feature Description section for additional information regarding the inputs for this device.



9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section
- 2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS594-Q1 to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.3 Application Curves

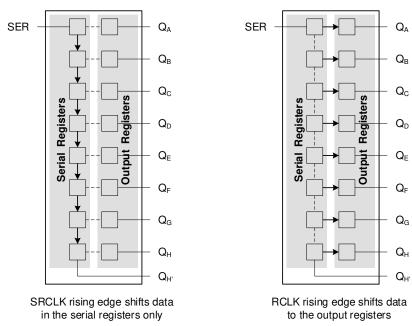


Figure 9-2. Simplified Functional Diagram Showing Clock Operation



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

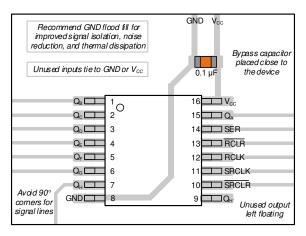


Figure 11-1. Example Layout for the SN74HCS594-Q1 in the PW Package



12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, HCMOS Design Considerations application report
- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, Designing With Logic application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74HCS594QBQBRQ1	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q
SN74HCS594QBQBRQ1.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q
SN74HCS594QDRQ1	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QDRQ1.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QDYYRQ1	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QPWRQ1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QPWRQ1.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QWBQBRQ1	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q
SN74HCS594QWBQBRQ1.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF SN74HCS594-Q1:

Catalog: SN74HCS594

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS594QBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74HCS594QDYYRQ1	SOT-23- THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74HCS594QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS594QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS594QBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74HCS594QDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74HCS594QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74HCS594QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



INDSTNAME



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



INDSTNAME



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



INDSTNAME



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- 5. Reference JEDEC Registration MO-345, Variation AA



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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