SCLS149C - DECEMBER 1982 - REVISED DECEMBER 2002

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max I<sub>CC</sub>
- Typical t<sub>pd</sub> = 8 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Lock Bus-Latch Capability
- True Logic

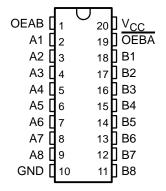
#### description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

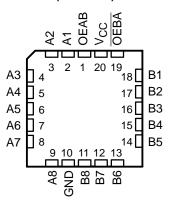
The 'HC623 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

OEAB and OEBA disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and OEBA. Each output reinforces its input in this transceiver configuration. When both OEAB and OEBA are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical.

#### SN54HC623...J OR W PACKAGE SN74HC623...DW, N, OR NS PACKAGE (TOP VIEW)



## SN54HC623 . . . FK PACKAGE (TOP VIEW)



#### ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
-40°C to 85°C	PDIP – N	Tube	SN74HC623N	SN74HC623N		
	COIC DW	Tube	SN74HC623DW	HC623		
-40°C to 85°C	SOIC - DW	Tape and reel	SN74HC623DWR	HC023		
	SOP - NS	Tape and reel	SN74HC623NSR	HC623		
	CDIP – J Tube		SNJ54HC623J	SNJ54HC623J		
–55°C to 125°C	CFP – W	Tube	SNJ54HC623W	SNJ54HC623W		
	LCCC – FK	Tube	SNJ54HC623FK	SNJ54HC623FK		

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



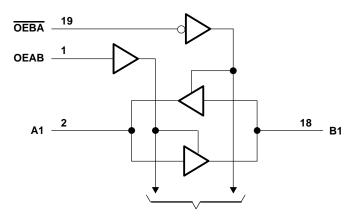
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#### **FUNCTION TABLE**

INP	UTS	ODEDATION
OEBA	OEAB	OPERATION
L	L	B data to A bus
Н	Н	A data to B bus
Н	L	Isolation
L	Н	B data to A bus, A data to B bus

#### logic diagram (positive logic)



**To Seven Other Transceivers** 

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		0.5 V to 7	V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see	ee Note 1)	±20 m.	Α
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CO</sub>	C) (see Note 1)	)      ±20 m.	Α
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$		±35 m.	Α
Continuous current through V <sub>CC</sub> or GND		±70 m	Α
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: DW package	58°C/V	Ν
	N package	69°C/V	Ν
	NS package	60°C/V	Ν
Storage temperature range, T <sub>stq</sub>		–65°C to 150°C	С

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 3)

			SN	154HC62	23	SN	174HC62	23	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
VIH	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		V <sub>CC</sub> = 6 V	4.2		ih	4.2			
		V <sub>CC</sub> = 2 V		Ą	0.5			0.5	
VIL	Low-level input voltage	V <sub>CC</sub> = 4.5 V		20	1.35			1.35	V
		VCC = 6 V		6	1.8			1.8	
٧ı	Input voltage		0 2	5	VCC	0		VCC	V
VO	Output voltage		0	) The state of the	VCC	0		VCC	V
		V <sub>CC</sub> = 2 V	Q		1000			1000	
Δt/Δν	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500			500	ns
		VCC = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		7507.00	NIDITIONS.		Т	A = 25°C	;	SN54H	C623	SN74H	IC623	
PAR	AMETER	TEST CO	NDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
				2 V	1.9	1.998		1.9		1.9		
Vон			$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		4.4		
		VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
			$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
			$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2	<sup>E</sup> h	5.34		
				2 V		0.002	0.1		0.1		0.1	
			I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1	4	0.1		0.1	
VOL		$V_I = V_{IH}$ or $V_{IL}$		6 V		0.001	0.1	40	0.1		0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26	20	0.4		0.33	
	_		$I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26	Ogy	0.4		0.33	
lį	OEAB or OEBA	$V_I = V_{CC}$ or 0		6 V		±0.1	±100	7	±1000		±1000	nA
loz	A or B	VO = VCC or 0		6 V		±0.01	±0.5		±10		±5	μΑ
Icc		$V_I = V_{CC}$ or 0,	I <sub>O</sub> = 0	6 V			8		160		80	μΑ
C <sub>i</sub>	OEAB or OEBA			2 V to 6 V		3	10		10		10	pF

# switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

	FROM	то		TA	λ = 25°C	;	SN54H	IC623	SN74H	C623	
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		29	105		160		130	
t <sub>pd</sub>	A or B	B or A	4.5 V		10	21		32		26	ns
·			6 V		8	18		27		22	
			2 V		112	210		315		265	
t <sub>en</sub>	OEBA	Α	4.5 V		27	42		63		53	ns
			6 V		20	36		54		45	
			2 V		40	150		225		190	
<sup>t</sup> dis	OEBA	Α	4.5 V		18	30		45		38	ns
			6 V		16	26	.<	38		32	
			2 V		112	210	Ź	315		265	
t <sub>en</sub>	OEAB	В	4.5 V		27	42	200	63		53	ns
			6 V		20	36	Q.	54		45	
			2 V		40	150		225		190	
t <sub>dis</sub>	OEAB	В	4.5 V		18	30		45		38	ns
			6 V		16	26		38		32	
			2 V		20	60		90		75	
t <sub>t</sub>		A or B	4.5 V		8	12		18		15	ns
			6 V		6	10		15		13	

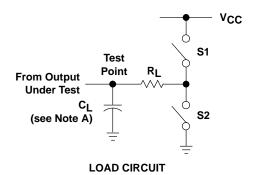
# switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)

	FROM	то		T,	\ = 25°C	;	SN54H	C623	SN74H	IC623		
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			2 V		44	135	135			170		
<sup>t</sup> pd	A or B	B or A	4.5 V		14	27		40		34	ns	
•			6 V		11	23		34		29		
			2 V		130	270		405		335		
	OEBA	Α	4.5 V		31	54		81		67	ns	
				6 V		23	46	Q	69		56	
t <sub>en</sub>			2 V		130	270	, '0,	405		335		
	OEAB	В	4.5 V		31	54	<sup>l</sup> q <sub>C</sub>	81		67	ns	
			6 V		23	46	40	69		56		
			2 V		45	210		315		265		
t <sub>t</sub>		A or B	4.5 V		17	42		63		53	ns	
			6 V		13	36		53		45		

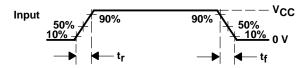
## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	No load	40	pF

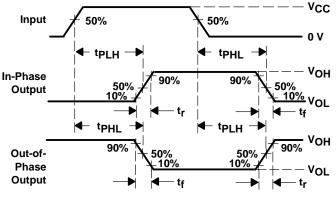
#### PARAMETER MEASUREMENT INFORMATION

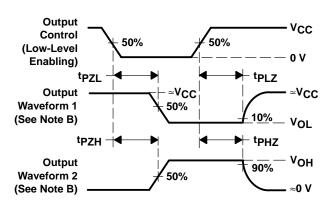


PARAI	METER	RL	CL	S1	S2
ton	tPZH	1 kO	50 pF	Open	Closed
ten t	<sup>t</sup> PZL	$ \begin{array}{c cccc} \hline  & 1 & k\Omega & \text{or} \\ \hline  & 150 & \text{pF} \end{array} $		Closed	Open
4	tPHZ 1 kΩ 50 pF		Open	Closed	
<sup>t</sup> dis	tPLZ	1 K22	50 pr	Closed	Open
t <sub>pd</sub> or	t <sub>t</sub>		50 pF or 150 pF	Open	Open



## VOLTAGE WAVEFORM INPUT RISE AND FALL TIMES





VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_{O} = 50 \Omega$ ,  $t_{f} = 6 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



www.ti.com 11-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74HC623DW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623
SN74HC623DW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623
SN74HC623N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC623N
SN74HC623N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC623N
SN74HC623NSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623
SN74HC623NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

www.ti.com 11-Nov-2025

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC623NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC623NSR	SOP	NS	20	2000	356.0	356.0	45.0

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HC623DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC623DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC623N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC623N.A	N	PDIP	20	20	506	13.97	11230	4.32

#### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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