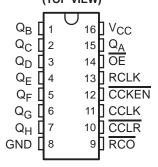
SCLS039F - DECEMBER 1982 - REVISED SEPTEMBER 2003

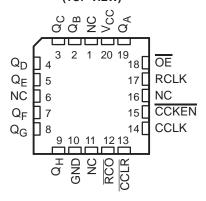
- 2-V to 6-V V<sub>CC</sub> Operation
- High-Current 3-State Parallel Register
   Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max I<sub>CC</sub>
- Typical t<sub>pd</sub> = 14 ns

SN54HC590A . . . J OR W PACKAGE SN74HC590A . . . D, DW, OR N PACKAGE (TOP VIEW)



- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- 8-Bit Counter With Register
- Counter Has Direct Clear

SN54HC590A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

### description/ordering information

The 'HC590A devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear (CCLR) and count-enable (CCKEN) inputs. A ripple-carry output (RCO) is provided for cascading. Expansion is accomplished easily for two stages by connecting RCO of the first stage to CCKEN of the second stage. Cascading for larger count chains can be accomplished by connecting RCO of each stage to the counter clock (CCLK) input of the following stage.

CCLK and the register clock (RCLK) inputs are positive-edge triggered. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

#### ORDERING INFORMATION

TA	PACI	KAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HC590AN	SN74HC590AN
		Tube of 40	SN74HC590AD	
4000 1- 0500	SOIC - D	Reel of 2500	SN74HC590ADR	HC590A
-40°C to 85°C		Reel of 250	SN74HC590ADT	
	0010 011	Tube of 40	SN74HC590ADW	1105004
	SOIC - DW	Reel of 2000	SN74HC590ADWR	HC590A
	CDIP – J		SNJ54HC590AJ	SNJ54HC590AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC590AW	SNJ54HC590AW
	LCCC - FK	Tube of 55	SNJ54HC590AFK	SNJ54HC590AFK

T Package drawings, standard packing quantities, thermal data, symbolization, and PCB design quidelines are available at www.ti.com/sc/package.



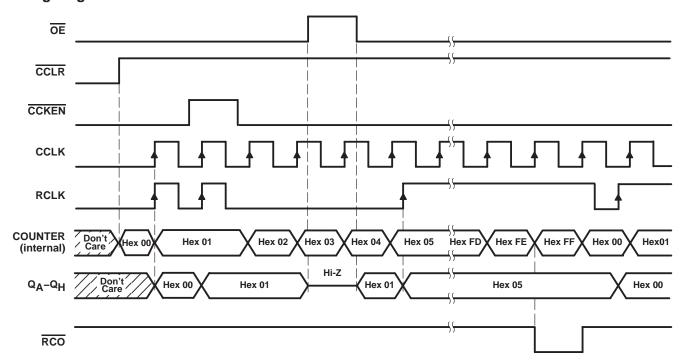
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



## SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS039F - DECEMBER 1982 - REVISED SEPTEMBER 2003

### timing diagram

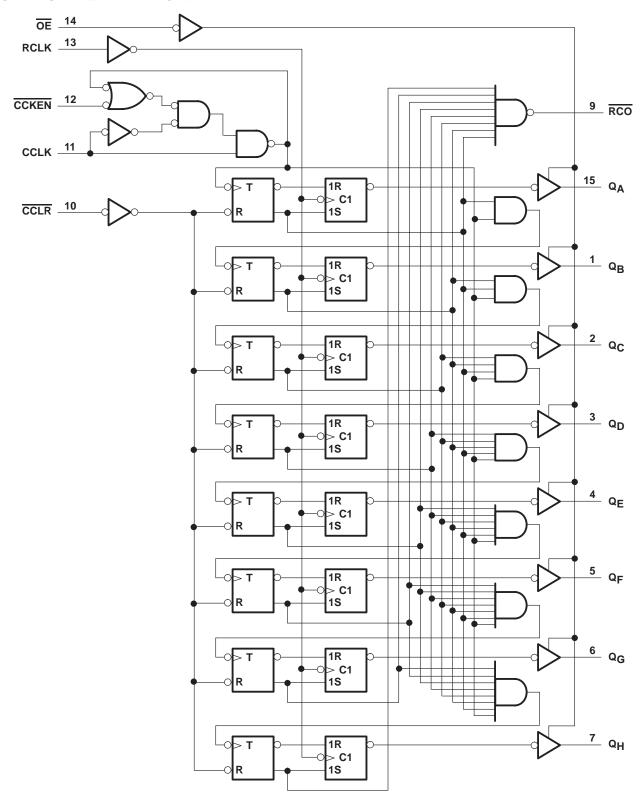


#### TIMING SEQUENCE

- 1. Clear Counter (asynchronous).
- 2. Count up: 0x01. Store 0x00 in register.
- 3. Inhibit counter clock (CCKEN = HIGH). Store 0x01 in register.
- 4. Count 0x02, 0x03.
- 5. 3-state the outputs
- 6. Count up: 0x04
- 7. Enable outputs.
- 8. Continue up: 0x059. Store 0x05 in register.
- 10. Continue counting: 0x06...0xFD, 0xFE, 0xFF, 0x00, etc.
- 11. Store 0x00 in register.



## logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.



SCLS039F - DECEMBER 1982 - REVISED SEPTEMBER 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see	ee Note 1)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCO	c) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )		±35 mA
Continuous current through V <sub>CC</sub> or GND		±70 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: D package	
	DW package	57°C/W
	N package	67°C/W
Storage temperature range, T <sub>sto</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			SN	54HC59	0A	SN	74HC590	)A	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2			
		V <sub>CC</sub> = 2 V			0.5			0.5	
VIL	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35			1.35	V
		VCC = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
٧o	Output voltage		0		VCC	0		VCC	V
		V <sub>CC</sub> = 2 V			1000			1000	
t <sub>t</sub> ‡	Input transition (rise and fall) time	V <sub>CC</sub> = 4.5 V			500			500	ns
		V <sub>CC</sub> = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

<sup>‡</sup> If this device is used in the threshold region (from V<sub>IL</sub>max = 0.5 V to V<sub>IH</sub>min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CCLK and RCLK inputs are not ensured while in the shift, count, or toggle operating modes.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		CONDITIONS	.,	Т	A = 25°C	;	SN54H	C590A	SN74H	C590A	
PARAMETER	TEST	CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
Voн	VI = VIH or VIL	$\overline{RCO}$ , $I_{OH} = -4 \text{ mA}$	45.7	3.98	4.3		3.7		3.84		V
		$Q_A-Q_H$ , $I_{OH}=-6$ mA	4.5 V	3.98	4.3		3.7		3.84		
		$\overline{RCO}$ , $I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
		$Q_A - Q_H$ , $I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
VOL	VI = VIH or VIL	$\overline{RCO}$ , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	V
		$Q_A-Q_H$ , $I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$\overline{RCO}$ , $I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
		$Q_A-Q_H$ , $I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
lį	VI = VCC or 0		6 V		±0.1	±100		±1000		±1000	nA
loz	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	μΑ
Icc	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF

## **SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS** WITH 3-STATE OUTPUT REGISTERS SCLS039F - DECEMBER 1982 - REVISED SEPTEMBER 2003

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			.,	T <sub>A</sub> = 1	25°C	SN54H	C590A	SN74H	C590A	
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		4		2.5		3.2	
fclock	Clock frequency		4.5 V		20		13		16	MHz
			6 V		24		16		19	
			2 V	125		200		155		
		CCLK or RCLK high or low	4.5 V	25		38		31		
	Dodge deserve		6 V	21		32		26		
t <sub>W</sub>	Pulse duration		2 V	100		150		125		ns
		CCLR low	4.5 V	20		30		25		
			6 V	17		26		21		
			2 V	100		150		125		
		CCKEN low before CCLK↑	4.5 V	20		30		25		
			6 V	17		26		21		
			2 V	100		150		125		
t <sub>su</sub>	Setup time	CCLR high (inactive) before CCLK↑	4.5 V	20		30		25		ns
			6 V	17		26		21		
			2 V	100		150		125		
		CCLK↑ before RCLK↑†	4.5 V	20		30		25		
			6 V	17		26		21		
	<u> </u>		2 V	50		75		60		
th	Hold time	CCKEN low after CCLK↑	4.5 V	10		15		12		ns
			6 V	9		13		11		

<sup>†</sup> This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.



# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

					SN	54HC590	0A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T,	ղ = 25°C	;		MAY	UNIT
	(1141 01)	(0011 01)		MIN	TYP	MAX	MIN	MAX	
			2 V	4	8		2.5		
f <sub>max</sub>			4.5 V	20	35		13		MHz
			6 V	24	40		16		
			2 V		80	150		225	
<sup>t</sup> pd	CCLK↑	RCO	4.5 V		20	31		45	ns
'			6 V		15	26		38	
			2 V		70	130		195	
<sup>t</sup> PLH	CCLR↓	RCO	4.5 V		18	28		39	ns
			6 V		14	23		33	
			2 V		70	140		210	
t <sub>pd</sub>	RCLK↑	Q	4.5 V		18	31		42	ns
			6 V		14	25		36	
			2 V		80	125		185	
t <sub>en</sub>	ŌĒ↓	Q	4.5 V		20	30		37	ns
			6 V		15	28		31	
			2 V		80	125		185	
<sup>t</sup> dis	ŌĒ↑	Q	4.5 V		20	30		37	ns
4.0			6 V		15	28		31	
			2 V		38	75		110	
		RCO	4.5 V		8	15		22	
*			6 V		6	13		19	
t <sub>t</sub> *			2 V		38	60		90	ns
		Q	4.5 V		8	12		18	
			6 V		6	10		15	

<sup>\*</sup> This parameter is not production tested for the SN54HC590A.

## **SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS** WITH 3-STATE OUTPUT REGISTERS SCLS039F - DECEMBER 1982 - REVISED SEPTEMBER 2003

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

					SN	74HC59	0A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T,	չ = 25°C	;	BAINI	BAAV	UNIT
	(1141 01)	(0011 01)		MIN	TYP	MAX	MIN	MAX	
			2 V	4	8		3.2		
f <sub>max</sub>			4.5 V	20	35		16		MHz
			6 V	24	40		19		
			2 V		80	150		190	
t <sub>pd</sub>	CCLK↑	RCO	4.5 V		20	30		38	ns
·			6 V		15	26		33	
			2 V		70	130		165	
t <sub>PLH</sub>	CCLR↓	RCO	4.5 V		18	26		33	ns
			6 V		14	22		28	
			2 V		70	140		175	
t <sub>pd</sub>	RCLK↑	Q	4.5 V		18	28		35	ns
·			6 V		14	24		30	
			2 V		80	125		155	
t <sub>en</sub>	ŌE↓	Q	4.5 V		20	25		31	ns
			6 V		15	21		26	
			2 V		80	125		155	
<sup>t</sup> dis	OE↑	Q	4.5 V		20	25		31	ns
			6 V		15	21		26	
			2 V		38	75		95	
		RCO	4.5 V		8	15		19	
			6 V		6	13		16	ns
t <sub>t</sub>			2 V		38	60		75	110
		Q	4.5 V		8	12		15	
			6 V		6	10		13	



# switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)

					SN	54HC59	0A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	TA	√ = 25°C	;	MINI	MAY	UNIT
	(1141 01)	(0011 01)		MIN	TYP	MAX	MIN	MAX	
			2 V		100	300		447	
<sup>t</sup> pd	RCLK↑	Q	4.5 V		24	60		90	ns
·			6 V		20	51		77	
			2 V		90	200		300	
t <sub>en</sub>	ŌĒ	Q	4.5 V		23	40		60	ns
			6 V		19	34		51	
			2 V		45	210		315	
t <sub>t</sub> *		Q	4.5 V		17	42		63	ns
			6 V		13	36		53	

<sup>\*</sup> This parameter is not production tested for the SN54HC590A.

## switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)

					SN	74HC59	0A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	TA	\ = 25°C	;	MIN	BAAV	UNIT
	( 51)	(0011 01)		MIN	TYP	MAX	IVIIIN	MAX	
			2 V		100	300		380	
<sup>t</sup> pd	RCLK↑	Q	4.5 V		24	60		76	ns
·			6 V		20	51		65	
			2 V		90	200		250	
t <sub>en</sub>	ŌĒ	Q	4.5 V		23	40		50	ns
			6 V		19	34		43	
			2 V		45	210		265	
t <sub>t</sub>		Q	4.5 V		17	42		53	ns
			6 V		13	36		45	

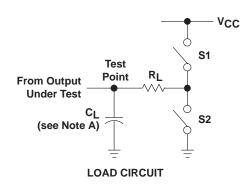
## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	250	pF

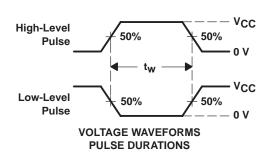


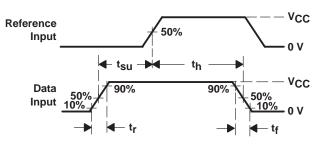
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### PARAMETER MEASUREMENT INFORMATION

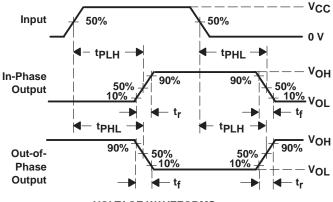


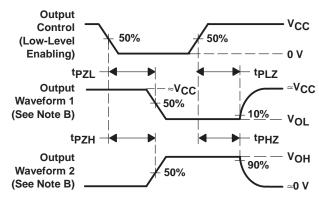
PARAI	METER	RL	CL	S1	S2
	tPZH	<b>1 k</b> Ω	50 pF or	Open	Closed
t <sub>en</sub>	tPZL	1 K22	150 pF	Closed	Open
	tPHZ	410		Open	Closed
<sup>t</sup> dis	tPLZ	<b>1 k</b> Ω	50 pF	Closed	Open
t <sub>pd</sub> or	t <sub>t</sub>		50 pF or 150 pF	Open	Open





**VOLTAGE WAVEFORMS** SETUP AND HOLD AND INPUT RISE AND FALL TIMES





**VOLTAGE WAVEFORMS** PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS** 

NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-89603012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89603012A SNJ54HC 590AFK
5962-8960301EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8960301EA SNJ54HC590AJ
5962-8960301FA	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8960301FA SNJ54HC590AW
SN54HC590AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC590AJ
SN54HC590AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC590AJ
SN74HC590AD	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC590A
SN74HC590ADR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A
SN74HC590ADR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A
SN74HC590ADT	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC590A
SN74HC590ADW	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-40 to 85	HC590A
SN74HC590ADWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A
SN74HC590ADWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A
SN74HC590AN	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC590AN
SN74HC590AN.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC590AN
SN74HC590ANE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC590AN
SNJ54HC590AFK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89603012A SNJ54HC 590AFK
SNJ54HC590AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89603012A SNJ54HC 590AFK
SNJ54HC590AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8960301EA SNJ54HC590AJ
SNJ54HC590AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8960301EA SNJ54HC590AJ

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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SNJ54HC590AW	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8960301FA SNJ54HC590AW
SNJ54HC590AW.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8960301FA SNJ54HC590AW

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54HC590A, SN74HC590A:

Catalog: SN74HC590A

## PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

Military: SN54HC590A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC590ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC590ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025



### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC590ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC590ADWR	SOIC	DW	16	2000	350.0	350.0	43.0

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-89603012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8960301FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC590AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC590AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC590AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC590AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC590ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC590ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC590AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC590AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC590AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54HC590AW.A	W	CFP	16	25	506.98	26.16	6220	NA

## D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- 5. Reference JEDEC registration MS-013.



SOIC



#### NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



#### NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## W (R-GDFP-F16)

## CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



**INSTRUMENTS** www.ti.com

#### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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