







SN54HC4020, SN74HC4020 SCLS158F - DECEMBER 1982 - REVISED FEBRUARY 2022

# SNx4HC4020 14-Bit Asynchronous Binary Counters

#### 1 Features

- Wide operating voltage range of 2 V to 6 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 80-µA max I<sub>CC</sub>
- Typical  $t_{pd}$  = 12 ns
- ±4-mA output drive at 5 V
- Low input current of 1 µA max

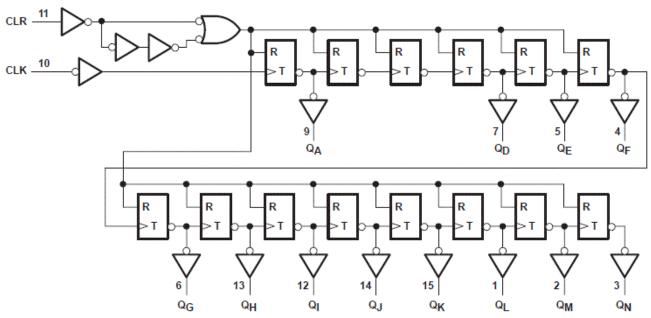
## 2 Description

The 'HC4020 devices are 14-stage binary ripple-carry counters that advance on the negative-going edge of the clock pulse. The counters are reset to zero (all outputs low) independently of the clock (CLK) input when the clear (CLR) input goes high.

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74HC4020D	SOIC (16)	9.90 mm × 3.90 mm
SN74HC4020N	PDIP (16)	19.31 mm × 6.35 mm
SN74HC4020NS	SO (16)	6.20 mm × 5.30 mm
SN74HC4020PW	TSSOP (16)	5.00 mm × 4.40 mm
SN54HC4020J	CDIP (16)	24.38 mm × 6.92 mm
SNJ54HC4020FK	LCCC (20)	8.89 mm × 8.45 mm
SNJ54HC4020W	CFP (16)	10.16 mm × 6.73 mm

For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

#### **Functional Block Diagram**



## **Table of Contents**

1 Features	1	7.2 Functional Block Diagram	8
2 Description	1	7.3 Device Functional Modes	8
3 Revision History	2	8 Power Supply Recommendations	9
4 Pin Configuration and Functions		9 Layout	
5 Specifications	4	9.1 Layout Guidelines	
5.1 Absolute Maximum Ratings		10 Device and Documentation Support	
5.2 Recommended Operating Conditions <sup>(1)</sup>	4	10.1 Documentation Support	. 10
5.3 Thermal Information	4	10.2 Receiving Notification of Documentation Updates.	.10
5.4 Electrical Characteristics	<mark>5</mark>	10.3 Support Resources	. 10
5.5 Timing Characteristics	5	10.4 Trademarks	. 10
5.6 Switching Characteristics	6	10.5 Electrostatic Discharge Caution	.10
5.7 Operating Characteristics		10.6 Glossary	.10
6 Parameter Measurement Information		11 Mechanical, Packaging, and Orderable	
7 Detailed Description	8	Information	. 10
7.1 Overview			

## **3 Revision History**

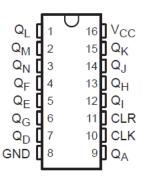
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision E (September 2003) to Revision F (February 2022)

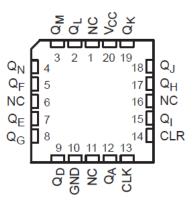
Page



## **4 Pin Configuration and Functions**



J, W, D, DB, N, NS, or PW Package 16-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP Top View



NC - No internal connection

FK Package 20-Pin LCCC Top View



## **5 Specifications**

#### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	$(V_I < 0 \text{ or } V_I > V_{CC})$		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±25	mA
	Continuous current through Vo	cc or GND		±50	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 Recommended Operating Conditions<sup>(1)</sup>

			SN	54HC4020		SN	74HC4020	)	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		V <sub>CC</sub> = 6 V	4.2			4.2			
		V <sub>CC</sub> = 2 V			0.5			0.5	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35			1.35	V
		V <sub>CC</sub> = 6 V			1.8			1.8	
VI	Input voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Vo	Output voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
		V <sub>CC</sub> = 2 V			1000			1000	
t <sub>t</sub>	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500			500	ns
		V <sub>CC</sub> = 6 V			400		,	400	
T <sub>A</sub>	Operating free-air temperature		-55		125	-40		85	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

#### 5.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
THERMAL I	METRIC	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	73	82	67	64	108	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



#### **5.4 Electrical Characteristics**

over recommended operating free-air temperature range (unelss otherwise noted)

	PARAMETER	TEST CONDITIONS(1)	V <sub>CC</sub>	T,	<sub>A</sub> = 25°C		SN54H0	C4020	SN74HC	4020	UNIT
	PARAMETER	TEST CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			2	1.9	1.998		1.9		1.9		
	V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = -20 μA	4.5	4.4	4.499		4.4		4.4		
V <sub>OH</sub>			6	5.9	5.999		5.9		5.9		V
		I <sub>OH</sub> = -4 mA	4.5	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = – 5.2 mA	6	5.48	5.8		5.2		5.34		
			2		0.002	0.1		0.1		0.1	
		I <sub>OL</sub> = 20 μA	4.5		0.001	0.1		0.1		0.1	
V <sub>OL</sub>	Low-level output voltage		6		0.001	0.1		0.1		0.1	V
		I <sub>OL</sub> = 4 mA	4.5		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6		0.15	0.26		0.4		0.33	
I <sub>I</sub>	Input hold current	V <sub>I</sub> = V <sub>CC</sub> or 0	6		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	Supply current	$V_I = V_{CC}$ or 0. $I_O = 0$	6			8		160		80	μA
Ci	Input capacitance		2 to 6		3	10		10		10	pF

<sup>(1)</sup>  $V_I = V_{IH}$  or  $V_{IL}$ , unless otherwise noted.

## **5.5 Timing Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

		<u> </u>	V 00	T <sub>A</sub> = 25	5°C	SN54HC	4020	SN74HC4	1020	UNIT
			V <sub>CC</sub> (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNII
			2		5.5		3.7		4.3	
f <sub>CLK</sub>	Clock frequency		4.5		28		19		22	MHz
			6		33		22		25	
		2	90		135		115			
		CLK high or low	4.5	18		27		23		
	Pulse duration		6	15		23		20		
t <sub>W</sub>	Puise duration		2	70		105		90		ns
		CLR high	4.5	14		21		18		
			6	12		18		25		
t <sub>su</sub>		2	60		90		75			
	Setup time, CLR inactive before CLK↓		4.5	12		18		15		ns
				10		15		13		



## **5.6 Switching Characteristics**

C<sub>L</sub> = 50 pF. See Parameter Measurement Information

PARAMETER	FROM	то	V 00	T,	λ = 25°C		SN54HC	4020	SN74HC4	4020	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			2	5.5	10		3.7		4.3		
f <sub>max</sub>			4.5	28	45		19		22		ns
			6	33	53		22		25		
	CLK		2		62	150		225		190	
t <sub>pd</sub>		CLK Q <sub>A</sub>	4.5		16	30		45		38	ns
			6		12	26		38	-	32	
			2		63	140		210		175	
t <sub>PHL</sub>	CLR	Any	4.5		17	28		42		35	ns
			6		13	24		36		30	
			2		28	75		110		95	
t <sub>t</sub>		Any	4.5		8	15		22		19	ns
			6		6	13		19		16	

# **5.7 Operating Characteristics**

T<sub>A</sub> = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	88	pF

 $V_{CC}$ 

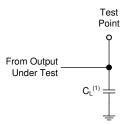
0 V

#### **6 Parameter Measurement Information**

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_t$  < 6 ns.

For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C<sub>L</sub> includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

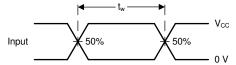
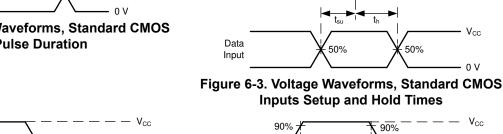
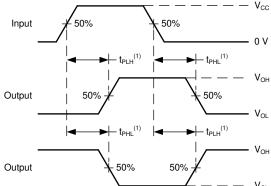


Figure 6-2. Voltage Waveforms, Standard CMOS **Inputs Pulse Duration** 



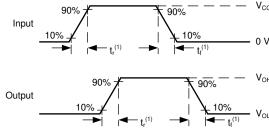
Clock

Input



(1) The greater between t<sub>PLH</sub> and t<sub>PHL</sub> is the same as t<sub>pd</sub>.

Figure 6-4. Voltage Waveforms, Propagation **Delays for Standard CMOS Inputs** 



50%

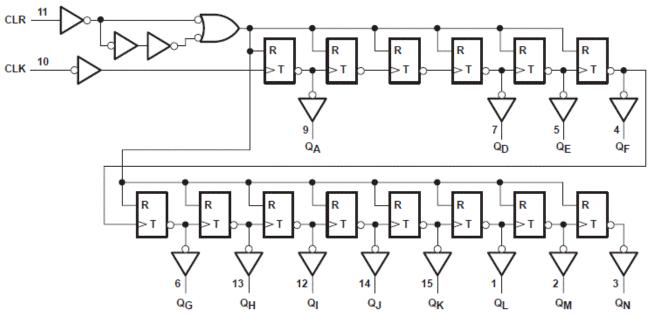
(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ . Figure 6-5. Voltage Waveforms, Input and Output **Transition Times for Standard CMOS Inputs** 

## 7 Detailed Description

#### 7.1 Overview

The 'HC4020 devices are 14-stage binary ripple-carry counters that advance on the negative-going edge of the clock pulse. The counters are reset to zero (all outputs low) independently of the clock (CLK) input when the clear (CLR) input goes high.

#### 7.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Figure 7-1. Functional Block Diagram

#### 7.3 Device Functional Modes

# Function Table (each buffer)

INI	PUTS	FUNCTION			
CLK	CLR	FUNCTION			
1	L	No change			
<b>1</b>	L	Advance to next stage			
X	Н	All outputs L			



## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

#### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### **10.1 Documentation Support**

#### 10.1.1 Related Documentation

#### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 10.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com

9-Nov-2025

## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
85003012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85003012A SNJ54HC 4020FK
8500301EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA SNJ54HC4020J
8500301FA	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301FA SNJ54HC4020W
SN54HC4020J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC4020J
SN54HC4020J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC4020J
SN74HC4020D	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC4020
SN74HC4020DR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4020N
SN74HC4020N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4020N
SN74HC4020NSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PW	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	HC4020
SN74HC4020PWR	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PWRG4	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PWT	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	HC4020
SNJ54HC4020FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85003012A SNJ54HC 4020FK
SNJ54HC4020FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85003012A SNJ54HC 4020FK
SNJ54HC4020J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA SNJ54HC4020J
SNJ54HC4020J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA SNJ54HC4020J



9-Nov-2025 www.ti.com

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SNJ54HC4020W	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301FA SNJ54HC4020W
SNJ54HC4020W.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301FA SNJ54HC4020W

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54HC4020, SN74HC4020:

Catalog: SN74HC4020

## PACKAGE OPTION ADDENDUM

www.ti.com 9-Nov-2025

Military: SN54HC4020

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

www.ti.com 10-Oct-2025

#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4020DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4020NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC4020PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4020PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4020PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



www.ti.com 10-Oct-2025



\*All dimensions are nominal

7 till dillitoriolorio di o riorininal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4020DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC4020NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC4020PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC4020PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC4020PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 10-Oct-2025

#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
85003012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8500301FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC4020N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4020N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4020N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4020N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC4020FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC4020FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC4020W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54HC4020W.A	W	CFP	16	25	506.98	26.16	6220	NA

# D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# W (R-GDFP-F16)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



**INSTRUMENTS** www.ti.com

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOP



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



#### NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



#### NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025