







SN54HC245, SN74HC245

SCLS131F - DECEMBER 1982 - REVISED AUGUST 2022

SNx4HC245 Octal Bus Transceivers With 3-State Outputs

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads
- Low Power Consumption, 80-µA Max I_{CC}
- Typical t_{pd} = 12 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 µA Max
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products. Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Servers
- PCs and Notebooks
- **Network Switches**
- Wearable Health and Fitness Devices
- Telecom Infrastructures
- Electronic Points of Sale

3 Description

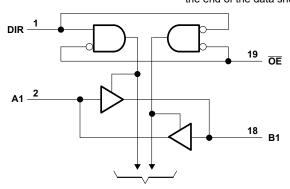
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
	DB (SSOP, 20)	7.20 mm × 5.30 mm		
	DW (SOIC, 20)	12.80 mm × 7.50 mm		
SNx4HC245	N (PDIP, 20)	24.33 mm × 6.35 mm		
	NS (SO, 20)	12.60 mm × 5.30 mm		
	PW (TSSOP, 20)	6.50 mm × 4.40 mm		

For all available packages, see the orderable addendum at the end of the data sheet.



To Seven Other Channels Logic Diagram (Positive Logic)



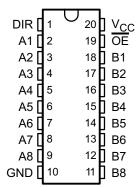
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4 Revision History		
NOTE: Page numbers for previous revisions may diff	er from page numbers in the current version.	
Changes from Revision E (September 2015) to Re	vision F (August 2022)	Page

•	Added Device Comparison section, Thermal Informationsection, ESD Ratings section, Application and Implementation section, Power Supply Recommendations section, and Layout section					
С	hanges from Revision D (August 2003) to Revision E (July 2015)	Page				
•	Added Device Comparison section, Thermal Information section, ESD Ratings section, Application and					
	Implementation section, Power Supply Recommendations section, and Layout section	1				
•	Added Military Disclaimer to Features list	1				
•	Updated FK package pinout drawing	3				



5 Pin Configuration and Functions



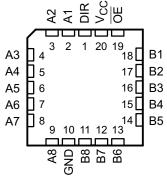


Figure 5-1. DB, DGV, DW, N, J, W, or PW Package 20-Pin SSOP, TVSOP, SOIC, PDIP CDIP, CFP, or TSSOP Top View

Figure 5-2. FK Package 20-Pin LCCC Top View

	PIN	TYPE(1)	D=20010=1011
NO.	NAME	- IYPE(")	DESCRIPTION
1	DIR	I/O	Direction Pin
2	A1	I/O	A1 Input/Output
3	A2	I/O	A2 Input/Output
4	A3	I/O	A3 Input/Output
5	A4	I/O	A4 Input/Output
6	A5	I/O	A5 Input/Output
7	A6	I/O	A6 Input/Output
8	A7	I/O	A7 Input/Output
9	A8	I/O	A8 Input/Output
10	GND	_	Ground Pin
11	B8	I/O	B8 Input/Output
12	B7	I/O	B7 Input/Output
13	B6	I/O	B6 Input/Output
14	B5	I/O	B5 Input/Output
15	B4	I/O	B4 Input/Output
16	В3	I/O	B3 Input/Output
17	B2	I/O	B2 Input/Output
18	B1	I/O	B1 Input/Output
19	OE	I/O	Output Enable
20	VCC	_	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I _{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC} or GND			±70	mA
T _{stg}	Storage temperature		-65	150	°C
TJ	Junction Temperature			150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN	154HC24	5	SN74HC245		UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 6 V	4.2	-		4.2			
	Low-level input voltage	V _{CC} = 2 V			0.5			0.5	
-		$V_{CC} = 4.5 \text{ V}$			1.35			1.35	V
		V _{CC} = 6 V			1.8			1.8	
VI	Input voltage	·	0		V_{CC}	0		V_{CC}	V
Vo	Output voltage		0	-	V_{CC}	0		V_{CC}	V
		V _{CC} = 2 V			1000			1000	
Δt/Δν	Input transition rise and fall time	V _{CC} = 4.5 V			500			500	ns
		V _{CC} = 6 V			400			400	
T _A	Operating free-air temperature		-55		125	-40		85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

		SNx4HC245							
	THERMAL METRIC(1)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	UNIT		
				20 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.1	77.0	57.0	74.1	99.7	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	53.9	41.5	48.6	40.6	34.0	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	47.2	44.8	38.0	41.6	50.7	°C/W		
ΨЈТ	Junction-to-top characterization parameter	16.5	16.8	25.4	14.8	1.8	°C/W		
ΨЈВ	Junction-to-board characterization parameter	46.8	44.3	37.8	41.2	50.1	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAME	TED	TEST CONDITIONS		V _{CC}	T,	_A = 25°C	;	SN54H	C245	SN74HC245		UNIT
	PARAIVIE	IEK	IESI CC	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
					2 V	1.9	1.998		1.9		1.9		
				I _{OH} = -20 µA	4.5 V	4.4	4.499		4.4		4.4		
			V _I = V _{IH}	μ, ,	6 V	5.9	5.999		5.9		5.9		
V _{OH}	High-Level Out	out Voltage	or V _{IL}	I _{OH} = -6 mA	4.5 V	3.98	4.3		3.7		3.84		V
				I _{OH} = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
				I _{OL} = 20 μΑ	2 V		0.002	0.1		0.1		0.1	
					4.5 V		0.001	0.1		0.1		0.1	
				F	6 V		0.001	0.1		0.1		0.1	
V _{OL}	V _{OL} Low-Level Outp	out Voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	V
				I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I _I	Input Current	DIR or OE	V _I = V _{CC}	or 0	6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	Off-State (High- Impedance State) Output Current	A or B	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	μΑ
I _{CC}	Supply Current $V_1 = V_{CC} I_{C}$ or 0,		I _O = 0	6 V			8		160		80	μΑ	
Ci	Input Capacitance	DIR or OE			2 V to 6 V		3	10		10		10	pF



6.6 Switching Characteristics, $C_L = 50 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM	то	v	T _A = 25°C			SN54HC245		SN74HC24	5	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V _{CC}	MIN	TYP	MAX	MIN N	IAX	MIN	MAX	UNII
			2 V		40	105		160		130	
t_{pd}	A or B	B or A	4.5 V		15	21		32		26	ns
			6 V		12	18		27		22	
			2 V		125	230		340		290	290 58 ns
t _{en}	ŌĒ	A or B	4.5 V		23	46		68		58	
			6 V		20	39		58		49	
			2 V		74	200		300		250	
$t_{\sf dis}$	ŌĒ	A or B	4.5 V		25	40		60		50	ns
			6 V		21	34		51		43	
			2 V		20	60		90		75	
t _t		A or B	4.5 V		8	12		18		15	ns
			6 V		6	10		15		13	

6.7 Switching Characteristics, $C_L = 150 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

	FROM	то	V _{CC}	T _A = 25°C			SN54HC245	SN74HC245		
PARAMETER	(INPUT)	(OUTPUT	UTPUT)	MIN	TYP	MAX	MIN MA	X MIN	MAX	UNIT
			2 V		54	135	2	00	170	
t _{pd}	A or B	B or A	4.5 V		18	27		10	34	ns
			6 V		15	23	:	34	29	
			2 V		150	270	4)5	335	
t _{en}	ŌĒ	A or B	4.5 V		31	54		31	67	ns
			6 V		25	46		69	56	
			2 V		45	210	3	5	265	
t _t		A or B	4.5 V		17	42		33	53	ns
			6 V		13	36		53	45	

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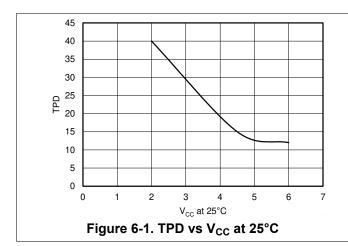
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6.8 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	No load	40	pF

6.9 Typical Characteristics



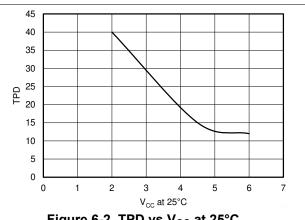
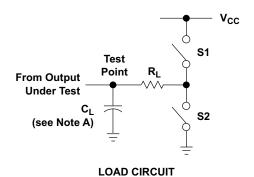


Figure 6-2. TPD vs V_{CC} at 25°C

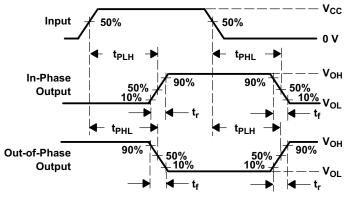


7 Parameter Measurement Information

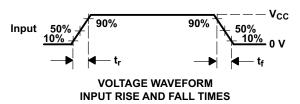
7.1

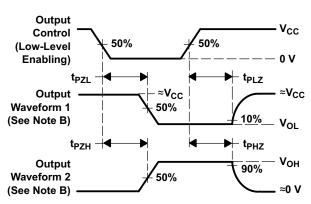


PARA	PARAMETER		CL	S1	S2	
	t _{PZH}	1 k Ω	50 pF or	Open	Closed	
t _{en}	t _{PZL}	1 K22	150 pF	Closed	Open	
•	t _{PHZ}	1 kΩ	50 pF	Open	Closed	
t _{dis}	t _{PLZ}	1 K22	50 pr	Closed	Open	
t _{pd} or t _t		-	50 pF or 150 pF	Open	Open	



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- A. C_I includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

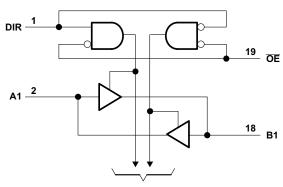
Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SNx4HC245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



To Seven Other Channels

Logic Diagram (Positive Logic)

8.3 Feature Description

The SNx4HC245 devices have a wide operating VCC range from 2 V to 6 V with slower edge rates to minimize output ringing.

8.4 Device Functional Modes

Table 8-1 lists the function modes of the SNx4HC245.

Table 8-1. Function Table

INPU	TS ⁽¹⁾	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	Х	Isolation				

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HC245 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

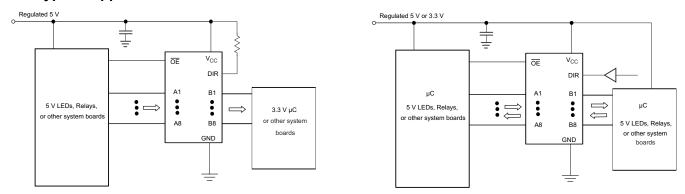


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs: See ($\Delta t/\Delta V$) in the Section 6.3.
 - Specified high and low levels: See (V_{IH} and V_{IL}) in the Section 6.3.
- 2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curve

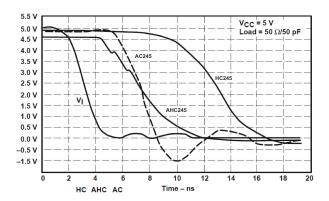


Figure 9-2. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 6.3.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

11.2 Layout Example

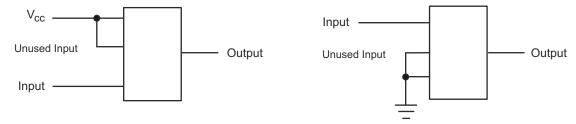


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC245	Click here	Click here	Click here	Click here	Click here
SN74HC245	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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31-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-8408501VRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8408501VR A SNV54HC245J
5962-8408501VRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8408501VR A SNV54HC245J
5962-8408501VSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8408501VS A SNV54HC245W
5962-8408501VSA.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8408501VS A SNV54HC245W
84085012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84085012A SNJ54HC 245FK
8408501RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501RA SNJ54HC245J
8408501SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501SA SNJ54HC245W
JM38510/65503BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65503BRA
JM38510/65503BRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65503BRA
JM38510/65503BSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65503BSA
JM38510/65503BSA.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65503BSA
M38510/65503BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65503BRA
M38510/65503BSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type -55 to 125		JM38510/ 65503BSA
SN54HC245J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC245J
SN54HC245J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC245J
SN74HC245DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74HC245DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245DBRG4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	HC245
SN74HC245DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245DWRE4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245DWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC245N
SN74HC245N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC245N
SN74HC245NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245NSRE4	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245PW	Obsolete	Production	TSSOP (PW) 20	-	=	Call TI	Call TI	-40 to 85	HC245
SN74HC245PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245PWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245
SN74HC245PWT	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	HC245
SNJ54HC245FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84085012A SNJ54HC 245FK
SNJ54HC245FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84085012A SNJ54HC 245FK
SNJ54HC245J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501RA SNJ54HC245J
SNJ54HC245J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501RA SNJ54HC245J
SNJ54HC245W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501SA SNJ54HC245W
SNJ54HC245W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501SA SNJ54HC245W

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- (1) Status: For more details on status, see our product life cycle.
- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Catalog: SN74HC245, SN54HC245

Military: SN54HC245

Space: SN54HC245-SP

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

OTHER QUALIFIED VERSIONS OF SN54HC245, SN54HC245-SP, SN74HC245:



PACKAGE OPTION ADDENDUM

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- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC245NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC245DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74HC245DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC245NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74HC245PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74HC245PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8408501VSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-8408501VSA.A	W	CFP	20	25	506.98	26.16	6220	NA
84085012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8408501SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/65503BSA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/65503BSA.A	W	CFP	20	25	506.98	26.16	6220	NA
M38510/65503BSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74HC245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC245N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC245FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC245FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC245W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54HC245W.A	W	CFP	20	25	506.98	26.16	6220	NA

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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