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SN74GTLPH306 8-BIT LVTTL-TO-GTLP BUS TRANSCEIVER

SCES284E-OCTOBER 1999-REVISED APRIL 2005

FEATURES

- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC[™] Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels
- LVTTL Interfaces Are 5-V Tolerant
- Medium-Drive GTLP Outputs (50 mA)
- LVTTL Outputs (-24 mA/24 mA)
- GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on A-Port Data Inputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGV, DW, OR PW PACKAGE (TOP VIEW) OE 24 [DIR 2 23 V_{REF} V_{CC} 22 B1 Α1 A2 🛮 4 21 B2 А3 20 B3 ∐ 5 Α4 19 B4 **∐** 6 GND 18 **∏** GND 17 **∏** B5 A5 A6 16 B6 119 15 B7 Α7 14 🛮 B8 11 Α8 13 GND GND 1 12

DESCRIPTION/ORDERING INFORMATION

The SN74GTLPH306 is a medium-drive, 8-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OECTM circuitry, and TI-OPCTM circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω .

GTLP is the Texas Instruments (TITM) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH306 is given only at the preferred higher-noise-margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2 \text{ V}$ and $V_{REF} = 0.8 \text{ V}$) or GTLP ($V_{TT} = 1.5 \text{ V}$ and $V_{REF} = 1 \text{ V}$) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T _A	PACK	(AGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
4000 (0500	SOIC - DW	Tube	SN74GTLPH306DW	GTLPH306	
	SOIC - DVV	Tape and reel	SN74GTLPH306DWR	GILFH300	
-40°C to 85°C	TSSOP - PW	Tape and reel	SN74GTLPH306PWR	GH306	
	TVSOP - DGV	Tape and reel	SN74GTLPH306DGVR	GH306	

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL DESCRIPTION

The SN74GTLPH306 is an 8-bit bus transceiver and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{\text{OE}}$ can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

For A-to-B data flow, when \overline{OE} is low and DIR is high, the B outputs take on the logic value of the A inputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except \overline{OE} and DIR are low.

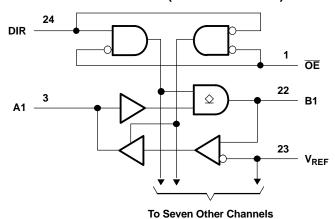
FUNCTION TABLE

INP	UTS	OUTDUT	MODE				
ŌĒ DIR		OUTPUT	MODE				
Н	Х	Z	Isolation				
L	L	B data to A port	True transporent				
L	Н	A data to B port	True transparent				





LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
	land delta a a mana (2)	A port and control inputs	-0.5	7	\ <i>/</i>
VI	Input voltage range ⁽²⁾	B port and V _{REF}	-0.5	4.6	V
	Voltage range applied to any output in the	A port	-0.5	7	V
Vo	high-impedance or power-off state (2)	B port	-0.5	4.6	V
	Compart into any output in the law state	A port		48	Λ
I _O	Current into any output in the low state	B port		100	mA
Io	Current into any A port output in the high state (3))		48	mA
	Continuous current through each V _{CC} or GND			±100	mA
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
		DGV package		86	
θ_{JA}	Package thermal impedance (4)	DW package		46	°C/W
		PW package		88	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽³⁾ This current flows only when the output is in the high state and $V_O > V_{CC}$.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions (1)(2)(3)(4)

			MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage		3.15	3.3	3.45	V	
V	Termination voltage	GTL	1.14	1.2	1.26	V	
V_{TT}	Termination voltage	GTLP	1.35	1.5	1.65	V	
V	Deference voltage	GTL	0.74	0.8	0.87	V	
V_{REF}	Reference voltage	GTLP	0.87	1	1.1	V	
V	lanut valtaga	B port			V _{TT}	V	
VI	Input voltage	Except B port		V _{CC}	5.5	V	
V	High level input valtage	B port	V _{REF} + 0.05			V	
V _{IH}	High-level input voltage	Except B port	2			v	
V	Low lovel input voltage	B port			$V_{REF} - 0.05$	V	
V_{IL}	Low-level input voltage	Except B port			0.8	V	
I _{IK}	Input clamp current				-18	mA	
I _{OH}	High-level output current	A port			-24	mA	
	Laveland autout annuat	A port			24	A	
I _{OL}	Low-level output current	B port			50	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled			10	ns/V	
Δt/ΔV _{CC}	Power-up ramp rate		20			μs/V	
T _A	Operating free-air temperature		-40		85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

⁽²⁾ Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

⁽⁴⁾ V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.



Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

P	ARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IK}		V _{CC} = 3.15 V,	I _I = -18 mA			-1.2	V	
		V _{CC} = 3.15 V to 3.45 V,	I _{OH} = -100 μA	V _{CC} - 0.2				
V_{OH}	A port	V _{CC} = 3.15 V	I _{OH} = -12 mA	2.4			V	
		V _{CC} = 3.13 V	$I_{OH} = -24 \text{ mA}$	2				
		$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	$I_{OL} = 100 \mu A$			0.2		
	A port	V _{CC} = 3.15 V	I _{OL} = 12 mA			0.4		
V_{OL}		V _{CC} = 3.15 V	I _{OL} = 24 mA			0.5	V	
	P port	V - 2.15 V	$I_{OL} = 40 \text{ mA}$			0.4		
	B port	V _{CC} = 3.15 V	$I_{OL} = 50 \text{ mA}$			0.55		
	A-port and		$V_I = 0$ or V_{CC}			±5		
I ₁ ⁽²⁾	control inputs	V _{CC} = 3.45 V	$V_1 = 5.5 V$			±20	μΑ	
	B port		$V_{I} = 0 \text{ to } 1.5 \text{ V}$			±5		
I _{BHL} ⁽³⁾	A port	V _{CC} = 3.15 V,	$V_{I} = 0.8 \ V$	75			μΑ	
I _{BHH} ⁽⁴⁾	A port	V _{CC} = 3.15 V,	$V_I = 2 V$	-75			μΑ	
I _{BHLO} ⁽⁵⁾	A port	$V_{CC} = 3.45 \text{ V},$	$V_I = 0$ to V_{CC}	500			μΑ	
I _{BHHO} ⁽⁶⁾	A port	$V_{CC} = 3.45 \text{ V},$	$V_I = 0$ to V_{CC}	-500			μΑ	
		$V_{CC} = 3.45 \text{ V}, I_{C} = 0,$	Outputs high			20		
I_{CC}	A or B port	V_{I} (A-port or control input) = V_{CC} or GND,	Outputs low			20	+	
		V_I (B port) = V_{TT} or GND	Outputs disabled			20		
ΔI _{CC} ⁽⁷⁾		V _{CC} = 3.45 V, One A-port or control input at \ Other A-port or control inputs at V _{CC} or GND			1.5	mA		
C _i	Control inputs	V _I = 3.15 V or 0			4.5	5	рF	
C	A port	V _O = 3.15 V or 0			7.5	9	nE.	
C _{io}	B port	V _O = 1.5 V or 0			7.5	9	pF	

- (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
- For I/O ports, the parameter I_I includes the off-state output leakage current. The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
- The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to VIHmin.
- An external driver must source at least I_{BHLO} to switch this node from low to high. An external driver must sink at least I_{BHHO} to switch this node from high to low.
- This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

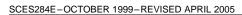
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
l _{off}	$V_{CC} = 0$,	V_1 or $V_0 = 0$ to 5.5 V			10	μΑ
I _{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V},$	$V_0 = 0.5 \text{ V to 3 V},$	OE = 0		±30	μΑ
I _{OZPD}	$V_{CC} = 1.5 \text{ V to } 0,$	$V_0 = 0.5 \text{ V to 3 V},$	OE = 0		±30	μΑ

Hot-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 1.5 V			10	μΑ
I _{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V},$	$V_0 = 0.5 \text{ V to } 1.5 \text{ V},$	$\overline{OE} = 0$		±30	μΑ
I _{OZPD}	$V_{CC} = 1.5 \text{ V to } 0,$	$V_0 = 0.5 \text{ V to } 1.5 \text{ V},$	$\overline{OE} = 0$		±30	μΑ

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Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

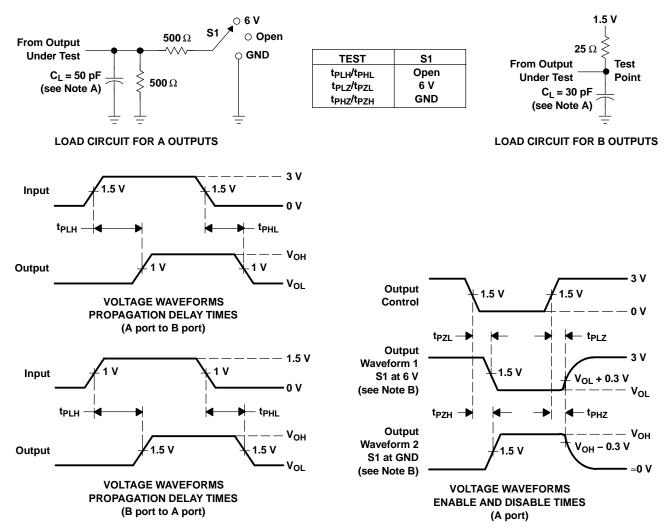
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT	
t _{PLH}	A	В	1		7.5	ns	
t _{PHL}	^	Б	1		7.5	115	
t _{en}	OE	В	1		8		
t _{dis}	- OE	Б	1		8	ns	
t _r	Rise time, B outpu		2.2		ns		
t _f	Fall time, B output	Fall time, B outputs (80% to 20%)					
t _r	Rise time, A outpu	ts (10% to 90%)		4.1		ns	
t _f	Fall time, A output	s (90% to 10%)		3.3		ns	
t _{PLH}	В	^	1		7		
t _{PHL}	Б	A	1		7	ns	
t _{en}	- OE	^	1		8		
t _{dis}	JE	A	1		8	ns	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.





PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, Z_0 = 50 Ω , t_r \approx 2 ns, t_f \approx 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

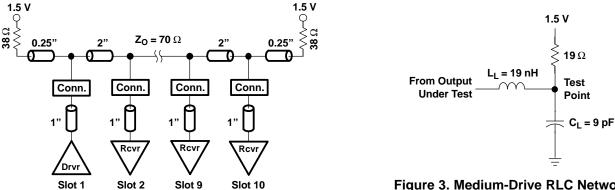


Figure 2. Medium-Drive Test Backplane

Figure 3. Medium-Drive RLC Network

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5 \text{ V}$ and $V_{RFF} = 1 \text{ V}$ for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP ⁽¹⁾	UNIT	
t _{PLH}	Λ	В	3.6		
t _{PHL}	A	В	4.1	ns	
t _{en}	ŌĒ	В	4.4	ns	
t _{dis}	OE	Ь	4.6		
t _r	Rise time, B outpu	1.2	ns		
t _f	Fall time, B output	s (80% to 20%)	2.2	ns	

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. All values are derived from TI-SPICE models.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow (5)		(6)
SN74GTLPH306DGVR	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306
SN74GTLPH306DGVR.B	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306
SN74GTLPH306DGVRG4	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306
SN74GTLPH306DGVRG4.B	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306
SN74GTLPH306DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLPH306
SN74GTLPH306DW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLPH306
SN74GTLPH306DWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLPH306
SN74GTLPH306DWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLPH306
SN74GTLPH306PW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306
SN74GTLPH306PW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306
SN74GTLPH306PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306
SN74GTLPH306PWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GH306

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH306DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74GTLPH306DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74GTLPH306PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH306DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74GTLPH306DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74GTLPH306PWR	TSSOP	PW	24	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74GTLPH306DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74GTLPH306DW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74GTLPH306PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74GTLPH306PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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