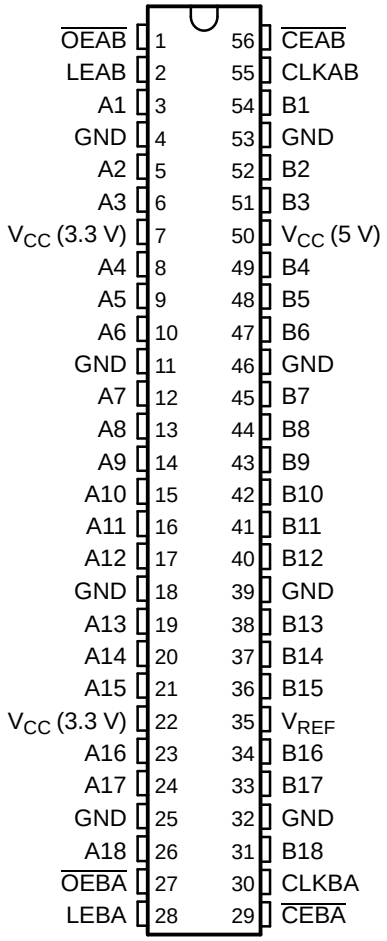
SN54GTL16612, SN74GTL16612
18-BIT LVTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVERS

SCBS480K – JUNE 1994 – REVISED JULY 2005

FEATURES

- **Members of Texas Instruments Widebus™ Family**
- **UBT™ Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Translate Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Support Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **Identical to '16601 Function**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

SN54GTL16612 . . . WD PACKAGE
SN74GTL16612 . . . DGG OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'GTL16612 devices are 18-bit UBT™ transceivers that provide LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. They combine D-type flip-flops and D-type latches to allow for transparent, latched, clocked, and clock-enabled modes of data transfer identical to the '16601 function. The devices provide an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using these devices at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

V_{CC} (5 V) supplies the internal and GTL circuitry while V_{CC} (3.3 V) supplies the LVTTL output buffers.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable(LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ also is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74GTL16612DL	GTL16612
		Tape and reel	SN74GTL16612DLR	
	TSSOP – DGG	Tape and reel	SN74GTL16612DGGR	GTL16612
–55°C to 125°C	CFP – WD	Tube	SNJ54GTL16612WD	SNJ54GTL16612WD

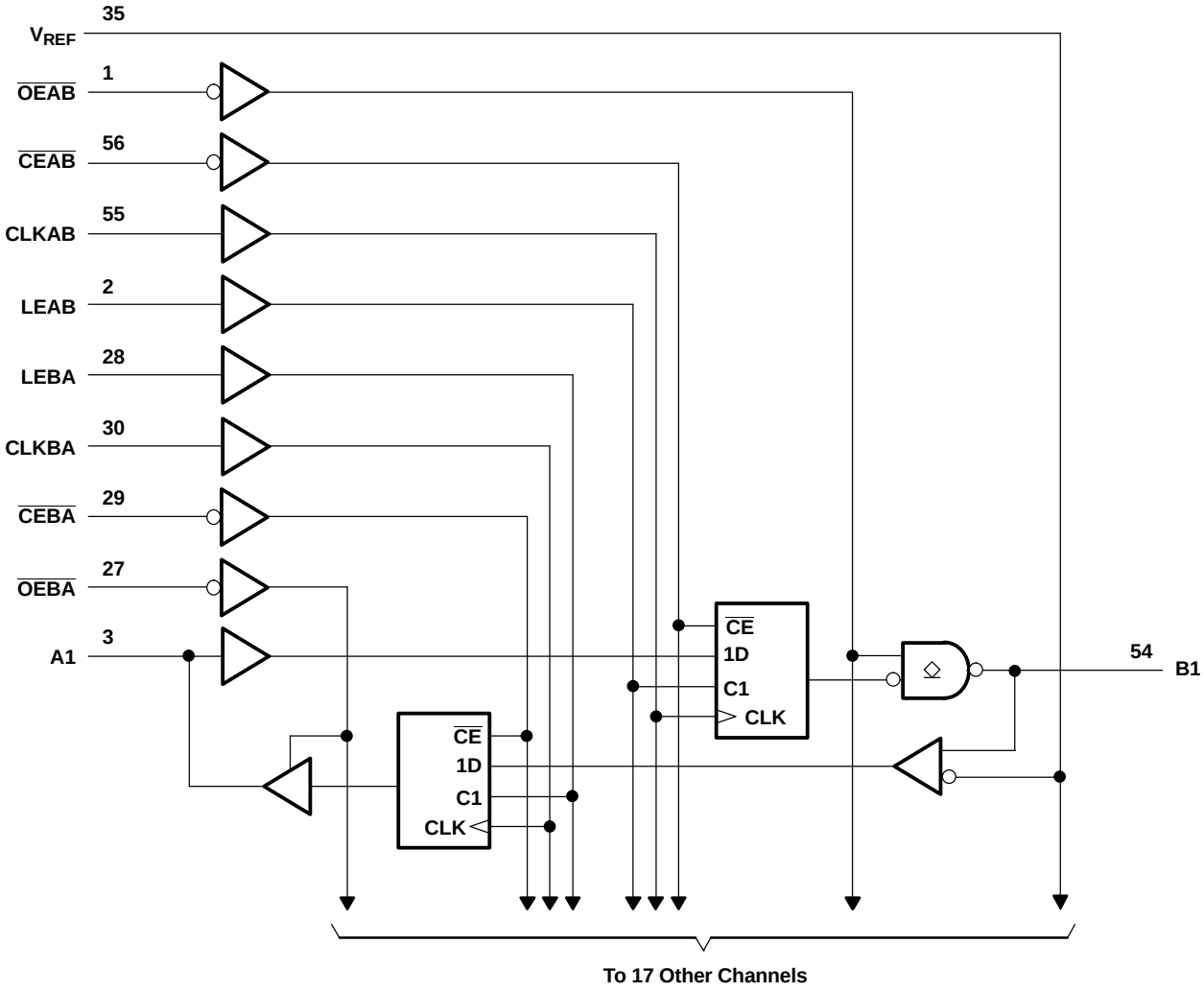
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE(1)

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0(2)	Latched storage of A data
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
(2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
(3) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	3.3 V	–0.5	4.6	V
		5 V	–0.5	7	
V_I	Input voltage range(2)	A-port and control inputs	–0.5	7	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high or power-off state(2)	A port	–0.5	7	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		128	mA
		B port		80	
I_O	Current into any A-port output in the high state(3)			64	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)	DGG package		64	°C/W
		DL package		56	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)(2)(3)(4)

			SN54GTL16612			SN74GTL16612			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	4.75	5	5.25	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}			V_{TT}	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V_{REF} + 50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF} – 50 mV			V_{REF} – 50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–32			–32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			40			40	
T_A	Operating free-air temperature		–55		125	–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16612			SN74GTL16612			UNIT
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} (3.3 V) = 3.15 V to 3.45 V, V_{CC} (5 V) = 4.75 V to 5.25 V	I_{OH} = –100 µA	V_{CC} (3.3 V) – 0.2			V_{CC} (3.3 V) – 0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = –8 mA	2.4			2.4			
			I_{OH} = –32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.6			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V, I_{OL} = 40 mA				0.5			0.4	
I_I	Control inputs	V_{CC} (3.3 V) = 0 or 3.45 V, V_{CC} (5 V) = 0 or 5.25 V	V_I = 5.5 V			10			10	µA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			1000			20	
			V_I = V_{CC} (3.3 V)			1			1	
			V_I = 0			–30			–30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			1000			100	µA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
			V_I = 0 to V_{CC} (3.3 V)(2)			±500			±500	
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 3 V				1			1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 1.2 V				10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0.5 V				–1			–1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0.4 V				–10			–10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC}(3)		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, A-port or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V				1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			3.5	12		3.5		pF
C_{io}	A port	V_O = 3.15 V or 0			12	18		12		pF
	B port					10			5	

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (unless otherwise noted) (see Figure 1)

			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			95		95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t_{su}	Setup time	A before CLKAB↑	1.3		1.3		ns
		B before CLKBA↑	3.4		2.5		
		A before LEAB↓	1.2		0		
		B before LEBA↓	1		1		
		$\overline{CEAB}$ before CLKAB↑	2.1		2		
		$\overline{CEBA}$ before CLKBA↑	2.6		2.2		
t_h	Hold time	A after CLKAB↑	2.9		1.6		ns
		B after CLKBA↑	4.1		0.3		
		A after LEAB↓	4.5		4		
		B after LEBA↓	4.3		3.6		
		$\overline{CEAB}$ after CLKAB↑	2		0.8		
		$\overline{CEBA}$ after CLKBA↑	1.1		1.1		

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.8	4.5	1.5	2.8	4.1	ns
t_{PHL}			1	2.5	4.5	1.3	2.5	4	
t_{PLH}	LEAB	B	1	3.6	5.5	2	3.6	5.3	ns
t_{PHL}			1	3.5	6	1.9	3.5	5.4	
t_{PLH}	CLKAB	B	1	3.7	5.5	2.3	3.7	5.3	ns
t_{PHL}			1	3.4	5.5	1.9	3.4	5.4	
t_{en}	$\overline{OEAB}$	B	1	3.3	5.5	2	3.3	5.5	ns
t_{dis}			1	3.4	5.5	2	3.4	5.1	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.3			1.3		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.5			0.5		ns
t_{PLH}	B	A	2	4.1	6.9	2.1	4.1	6.3	ns
t_{PHL}			1	2.9	5.1	1.2	2.9	4.6	
t_{PLH}	LEBA	A	2	3.7	6.1	2.3	3.7	5.7	ns
t_{PHL}			1	3	5.1	1.8	3	4.8	
t_{PLH}	CLKBA	A	2	3.8	6.4	2.5	3.8	6.1	ns
t_{PHL}			2	3.3	5.6	2.3	3.3	5.2	
t_{en}	$\overline{OEBA}$	A	1	5	7.5	2.3	5	7.4	ns
t_{dis}			2	4.3	6.9	2.5	4.3	6.4	

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (unless otherwise noted) (see Figure 1)

			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			95		95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t_{su}	Setup time	A before CLKAB↑	1.3		1.3		ns
		B before CLKBA↑	3.2		2.3		
		A before LEAB↓	1.2		0		
		B before LEBA↓	1.3		1.3		
		$\overline{CEAB}$ before CLKAB↑	2.1		2		
		$\overline{CEBA}$ before CLKBA↑	2.6		2.2		
t_h	Hold time	A after CLKAB↑	2.9		1.6		ns
		B after CLKBA↑	4.4		0.3		
		A after LEAB↓	4.5		4		
		B after LEBA↓	4.3		3.6		
		$\overline{CEAB}$ after CLKAB↑	2		0.8		
		$\overline{CEBA}$ after CLKBA↑	1.1		1.1		

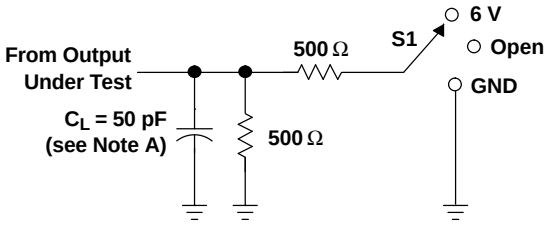
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

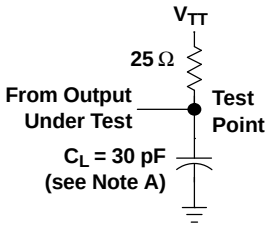
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.8	4.5	1.5	2.8	4.1	ns
t_{PHL}			1	2.5	4.6	1.3	2.5	4.1	
t_{PLH}	LEAB	B	1	3.6	5.5	2	3.6	5.3	ns
t_{PHL}			1	3.5	6.1	1.9	3.5	5.5	
t_{PLH}	CLKAB	B	1	3.7	5.5	2.3	3.7	5.3	ns
t_{PHL}			1	3.4	5.6	1.9	3.4	5.5	
t_{PLH}	$\overline{OEAB}$	B	1	3.4	5.5	2	3.4	5.1	ns
t_{PHL}			1	3.3	5.6	2	3.3	5.6	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.5			1.5		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.8			0.8		ns
t_{PLH}	B	A	1.9	4	6.9	2	4	6.3	ns
t_{PHL}			0.9	2.8	4.9	1.1	2.8	4.4	
t_{PLH}	LEBA	A	2	3.7	6.1	2.3	3.7	5.7	ns
t_{PHL}			1	3	5.1	1.8	3	4.8	
t_{PLH}	CLKBA	A	2	3.8	6.4	2.5	3.8	6.1	ns
t_{PHL}			2	3.3	5.6	2.3	3.3	5.2	
t_{en}	$\overline{OEBA}$	A	1	5	7.5	2.3	5	7.4	ns
t_{dis}			2	4.3	6.9	2.5	4.3	6.4	

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

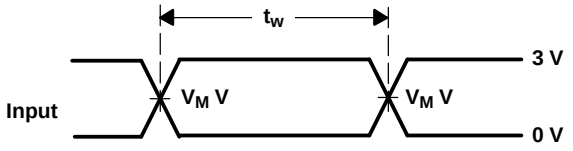
PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.2 V, V_{REF} = 0.8 V for GTL and V_{TT} = 1.5 V, V_{REF} = 1 V for GTL+



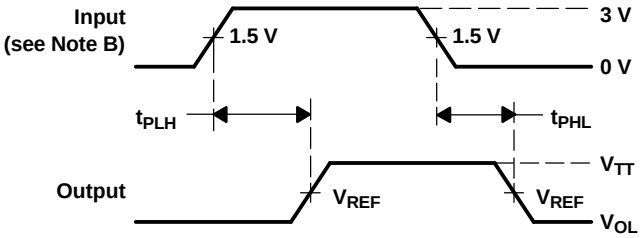
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



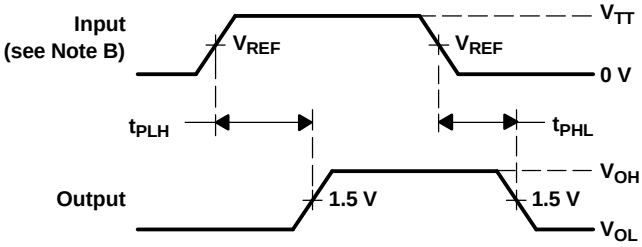
LOAD CIRCUIT FOR A OUTPUTS | **LOAD CIRCUIT FOR B OUTPUTS**



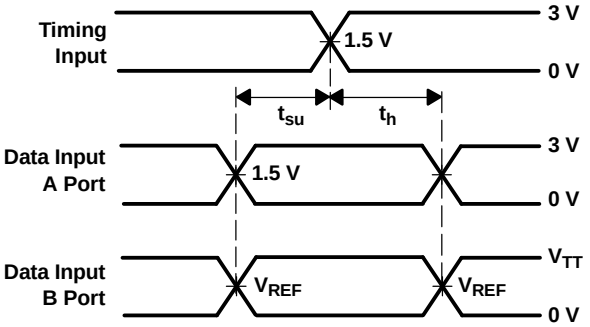
VOLTAGE WAVEFORMS
PULSE DURATION
(V_M = 1.5 V for A port and V_{REF} for B port)(1)



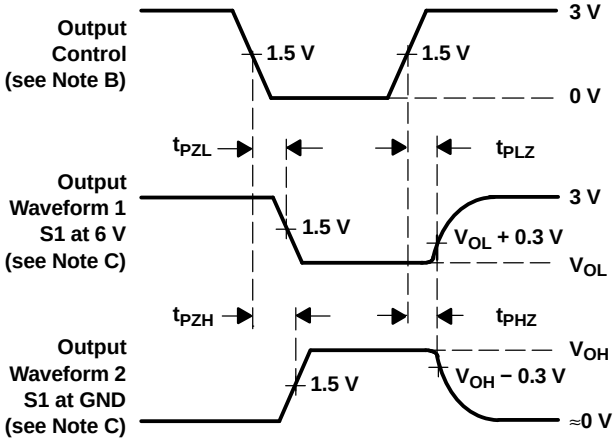
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)(1)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)(1)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

(1) All control inputs are TTL levels.

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74GTL16612DGGR	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16612
SN74GTL16612DGGR.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16612
SN74GTL16612DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16612
SN74GTL16612DL.B	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16612

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

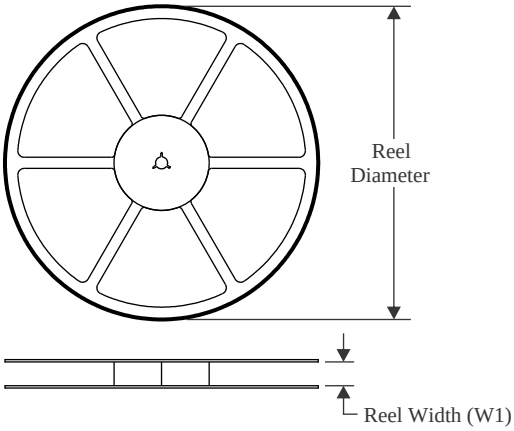
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

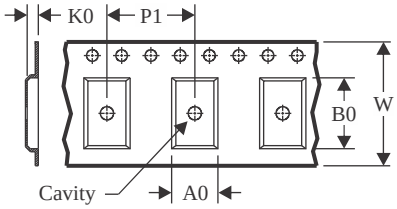
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

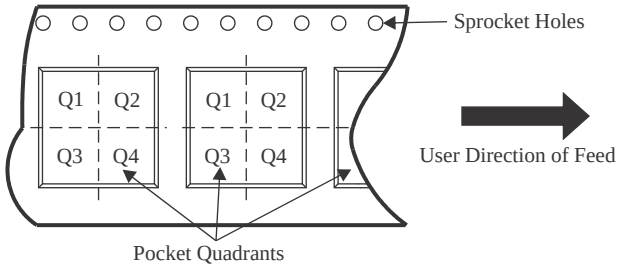


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

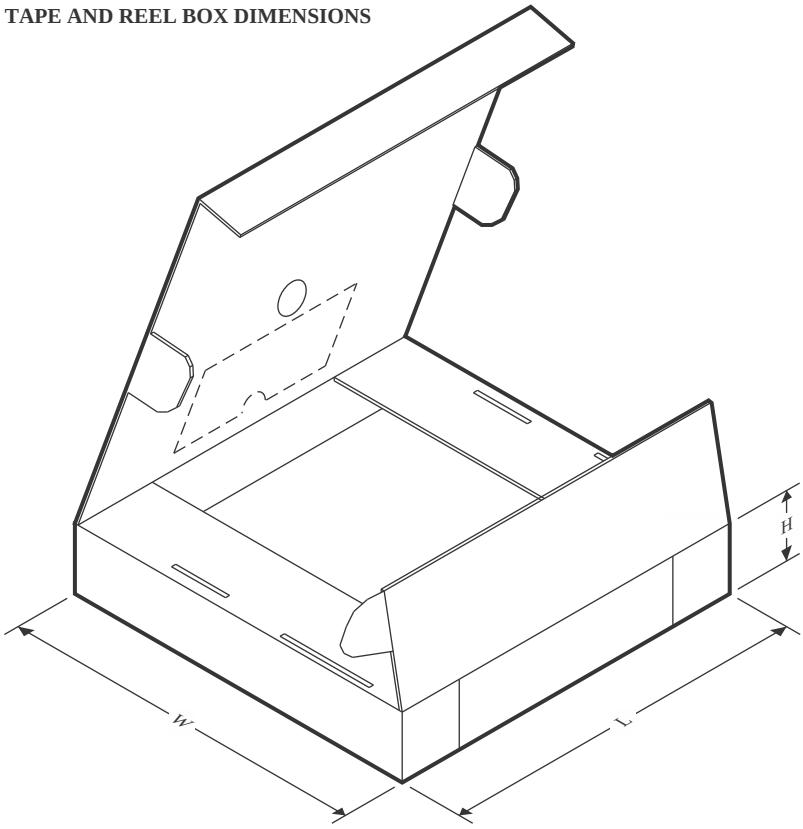
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL16612DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

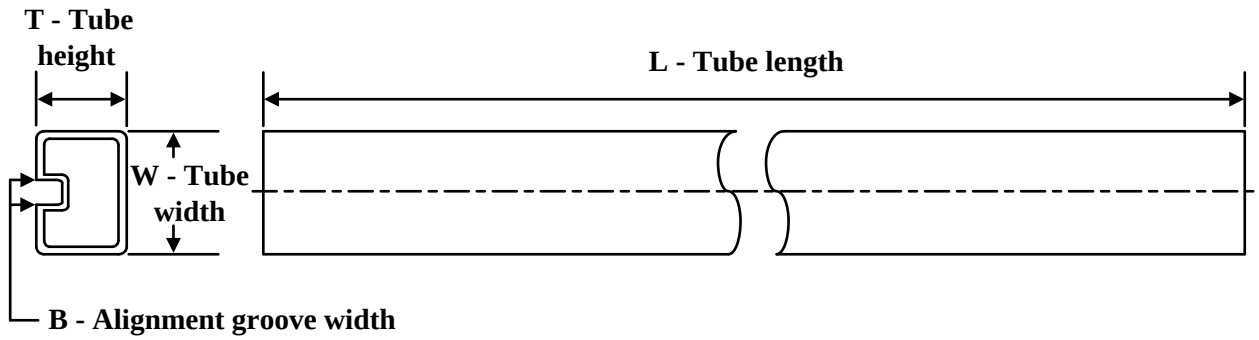
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL16612DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0

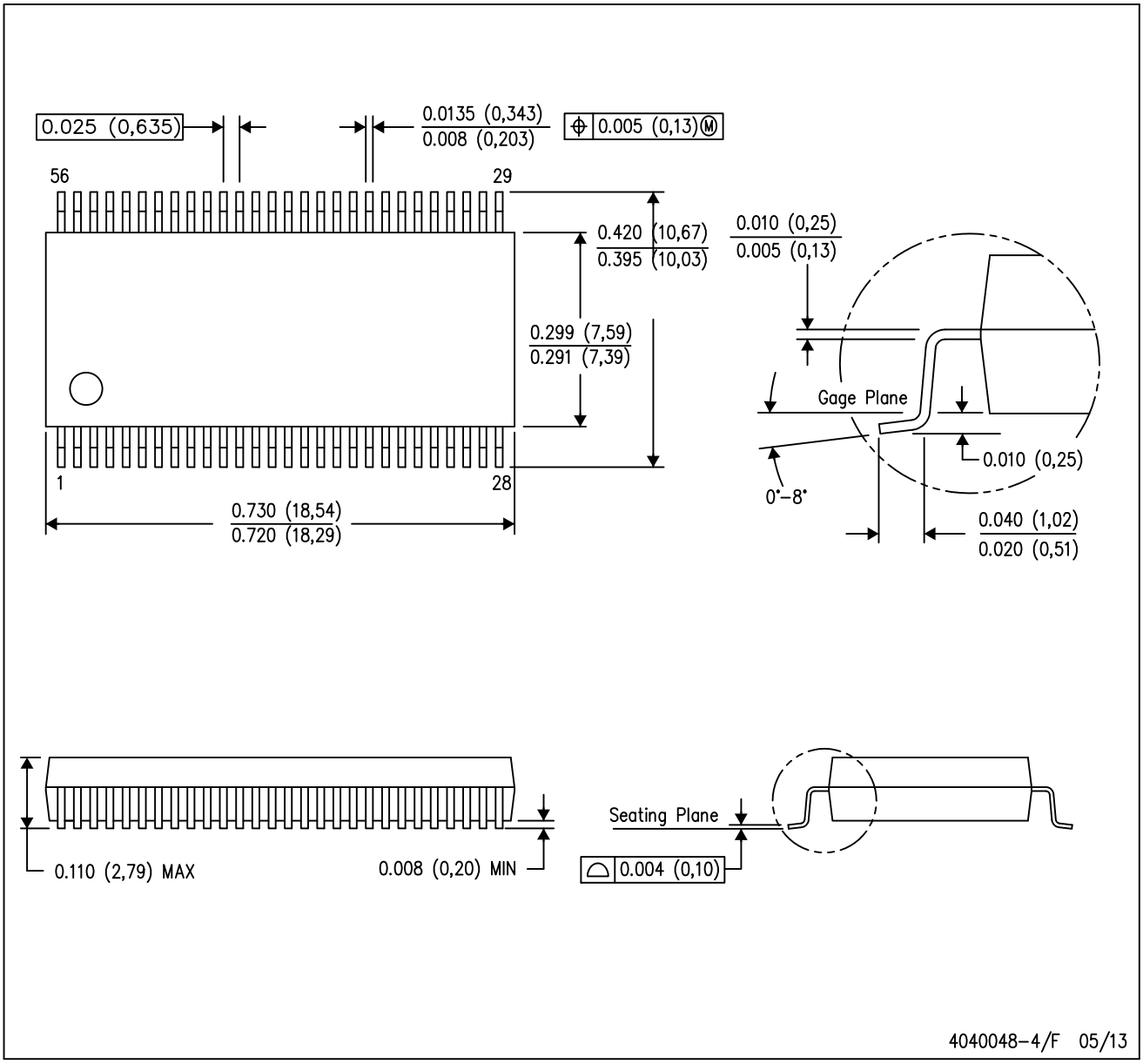
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74GTL16612DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74GTL16612DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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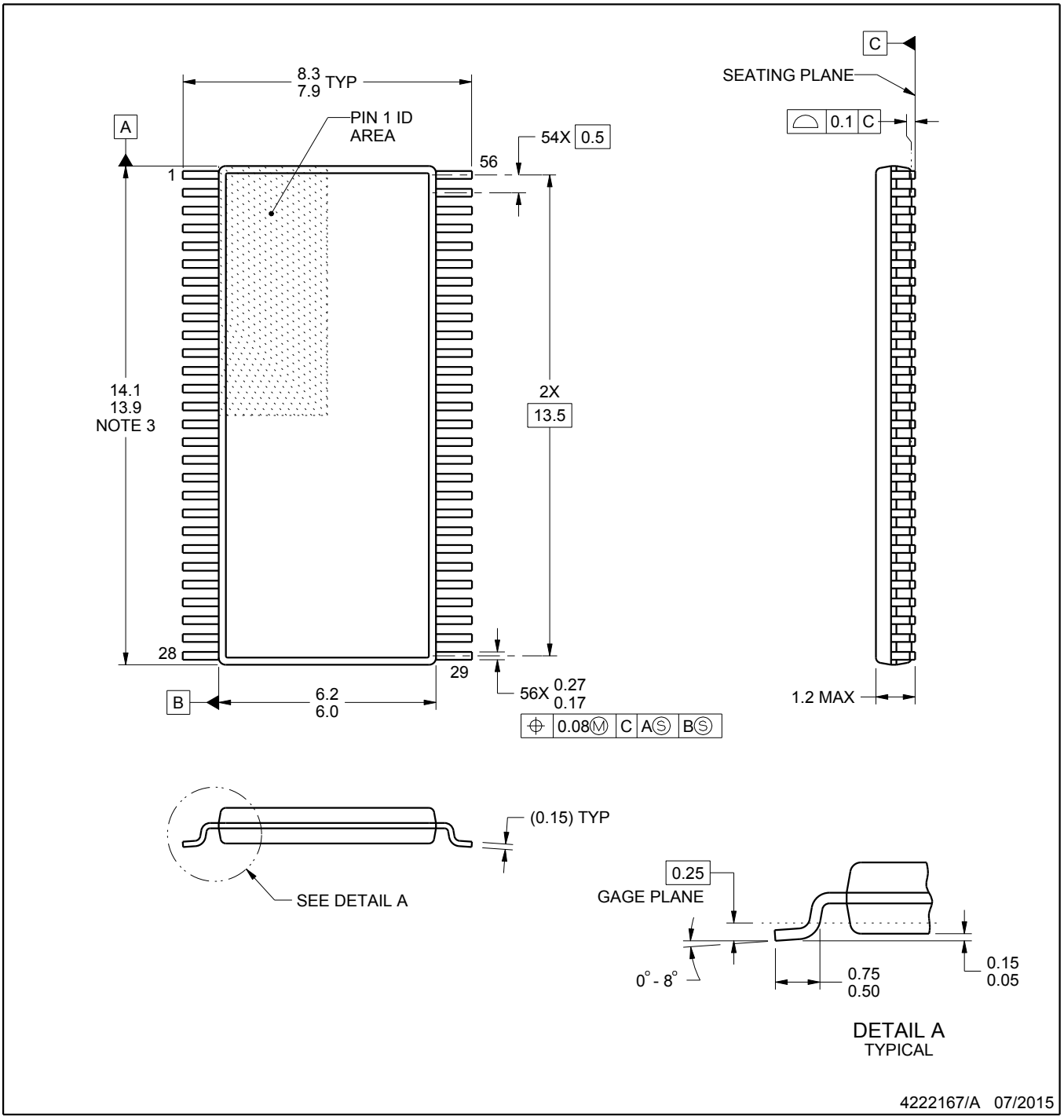
PACKAGE OUTLINE

DGG0056A

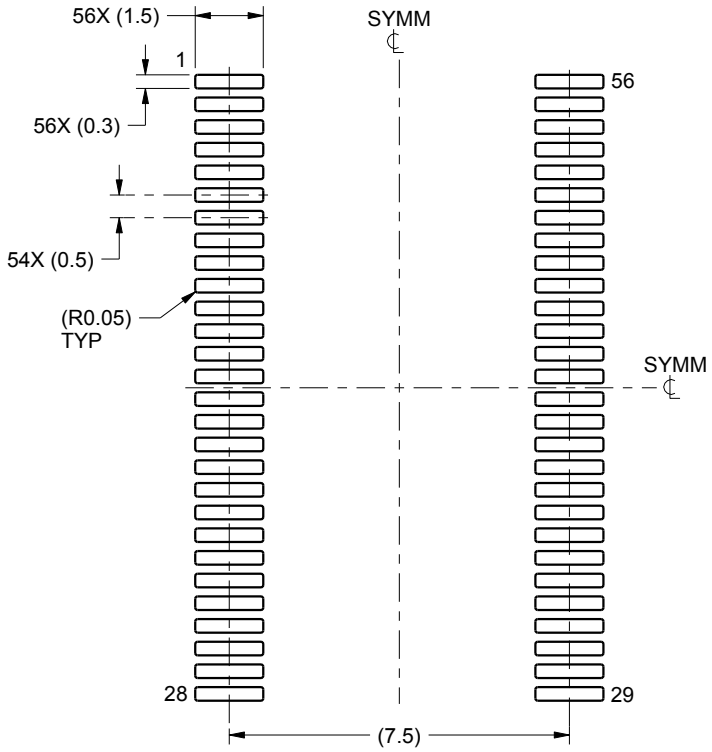
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

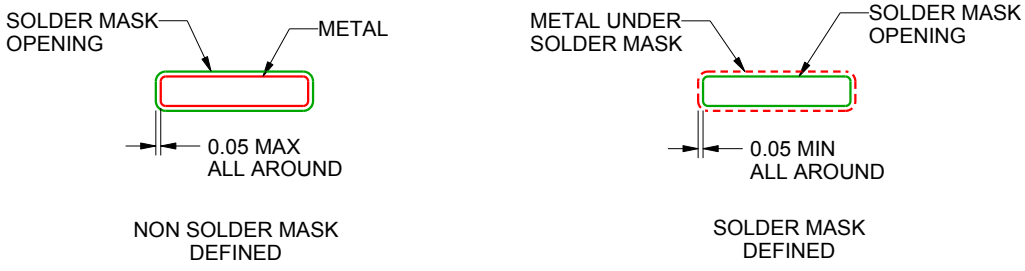


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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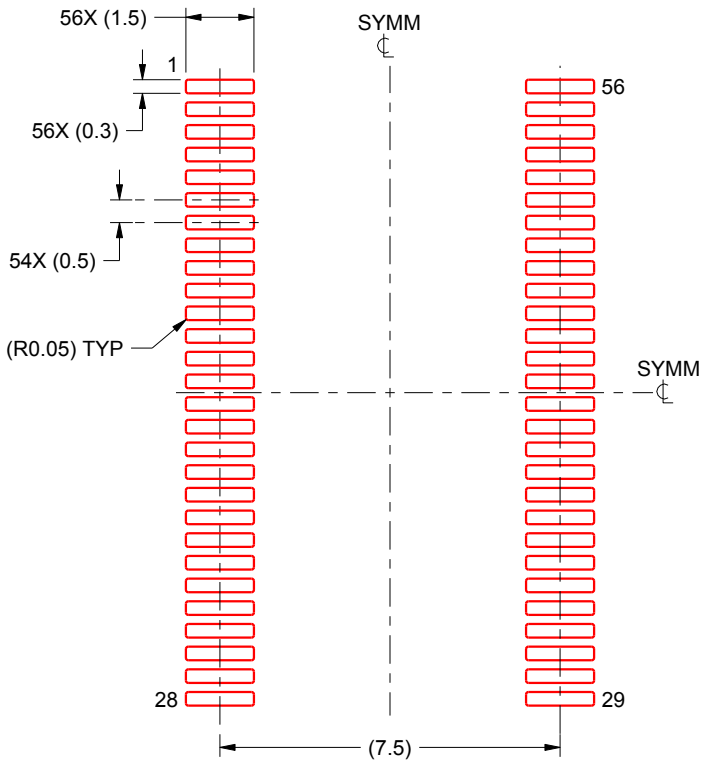
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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