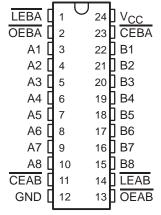
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- 3-State True Outputs
- Back-to-Back Registers for Storage
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages and Standard Plastic 300-mil DIPs

description

The SN74F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow. The A outputs are characterized to sink 24 mA while the B outputs are characterized to sink 64 mA.

DB, DW, OR NT PACKAGE (TOP VIEW)



The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. Having CEAB low and LEAB low makes the A-to-B latches transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and OEBA inputs.

The SN74F543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74F543 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE†

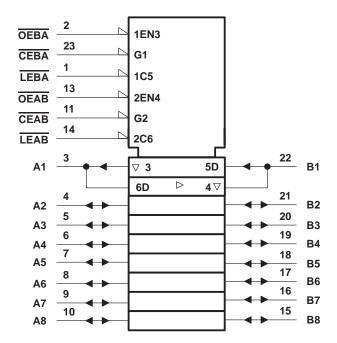
	INPUTS							
CEAB	LEAB	OEAB	Α	В				
Н	Х	Х	Χ	Z				
X	Χ	Н	Χ	Z				
L	Н	L	Χ	в ₀ ‡				
L	L	L	L	L				
L	L	L	Н	Н				

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.



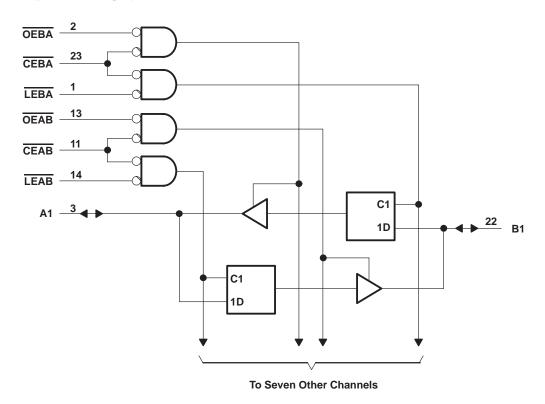
[‡] Output level before the indicated steady-state input conditions were established.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (excluding I/O ports) (see Note 1)	1.2 V to 7 V
Input current range, I _{IK}	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Voltage range applied to any output in the high state	0.5 V to V _{CC}
Current into any output in the low state: A1-A8	48 mÅ
B1-B8	128 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage			0.8	V	
lıK	Input clamp current			-18	mA	
lau	High level output ourrent	A1-A8			-3	mA
ЮН	High-level output current B1 – B8	B1-B8			-15	IIIA
la.	Low-level output current	A1-A8			24	mA
lOL	Low-level output current			64	IIIA	
TA	Operating free-air temperature	_	0		70	°C

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS				UNIT	
٧ıK		$V_{CC} = 4.5 \text{ V},$	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$				V	
	A1-A8		$I_{OH} = -1 \text{ mA}$	2.5	3.4			
	AT-AO	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	$I_{OH} = -3 \text{ mA}$	2.4	3.3			
Vон	B1-B8	V _{CC} = 4.5 V	$I_{OH} = -3 \text{ mA}$	2.4	3.3		V	
	D1-D0		$I_{OH} = -15 \text{ mA}$	2	3.1			
	Any output	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -1 \text{ mA to } -3 \text{ mA}$	2.7				
\/o;	A1-A8	V _{CC} = 4.5 V	I _{OL} = 24 mA		0.3	0.5	V	
VOL	B1-B8	VCC = 4.5 V	I _{OL} = 64 mA		0.42	0.55	V	
1.	OE, LE, and CE	V FV	V _I = 7 V			0.1	mA	
l _l	A and B ports	V _{CC} = 5.5 V	V _I = 5.5 V			1	IIIA	
. +	OE, LE, and CE	V	V 2.7 V			20		
I _{IH} ‡	A and B ports	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			70	μΑ	
. +	OE, LE, and CE	V _{CC} = 5.5 V,	V _I = 0.5 V			-1.2	mA	
I _{IL} ‡	A and B ports	vCC = 5.5 v,	V = 0.5 V			-0.65	IIIA	
	A1-A8	V F	V- 0	-60		-150	A	
IOS [§] B1-B8		vCC = 5.5 v,	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0$			-225	mA	
ICCH		V _{CC} = 5.5 V			67	100	mA	
ICCL	·	V _{CC} = 5.5 V			83	125	mA	
I _{CCZ}		V _{CC} = 5.5 V			83	125	mA	

timing requirements

		$V_{CC} = 5 \text{ V},$ $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $T_A = MIN \text{ to MAX}$				UNIT	
			MIN	MAX	MIN	MAX	
t _W	Pulse duration	5		5		ns	
t _{su}	Setup time, data before latch enable	High or low	3		3.5		ns
th	Hold time, data after latch enable	High or low	3		3.5		ns

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	C _L R _L	C = 5 V, = 50 pF = 500 Ω = 25°C	,	$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = \text{MIN t}$	UNIT		
			MIN	TYP	MAX	MIN	MAX	
^t PLH	A or B	B or A	2.2	5.1	7.5	2.2	8.5	ns
^t PHL	AOID	BULK	2.2	4.6	6.5	2.2	7.5	115
t _{PLH}	LEBA	А	3.7	8.1	11	4.1	12.5	no
t _{PHL}	LEBA		3.7	8.1	11	4.1	12.5	ns
t _{PLH}	LEAB	В	3.7	8.1	11	4.1	12.5	20
^t PHL	LEAB	В	3.7	8.1	11	4.1	12.5	ns
^t PZH	0 0	A or D	2.2	6.6	9	2.2	10	
t _{PZL}	OE or CE	A or B	3.2	7.1	10.5	3.2	12	ns
^t PHZ	OE or CE	A or B	1.7	5.6	8	1.7	9	20
tPLZ	OE OF CE	AUID	1.7	5.1	7.5	1.7	8.5	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74F543DBR	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543
SN74F543DBR.A	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543
SN74F543DW	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	0 to 70	F543
SN74F543DWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543
SN74F543DWR.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F543DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74F543DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F543DBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74F543DWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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