

# SN74F543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SDFS025B – D2942, MARCH 1987 – REVISED OCTOBER 1993

- 3-State True Outputs
- Back-to-Back Registers for Storage
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages and Standard Plastic 300-mil DIPs

## description

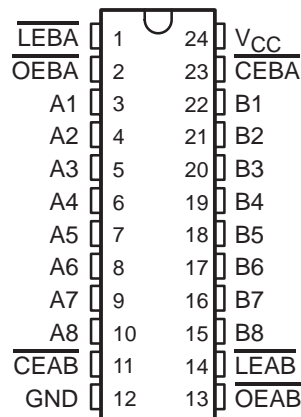
The SN74F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ( $\overline{LEAB}$  or  $\overline{LEBA}$ ) and output enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow. The A outputs are characterized to sink 24 mA while the B outputs are characterized to sink 64 mA.

The A-to-B enable ( $\overline{CEAB}$ ) input must be low in order to enter data from A or to output data from B. Having  $\overline{CEAB}$  low and  $\overline{LEAB}$  low makes the A-to-B latches transparent; a subsequent low-to-high transition of  $\overline{LEAB}$  puts the A latches in the storage mode. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs.

The SN74F543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74F543 is characterized for operation from 0°C to 70°C.

DB, DW, OR NT PACKAGE  
(TOP VIEW)



FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^\ddagger$
L	L	L	L	L
L	L	L	H	H

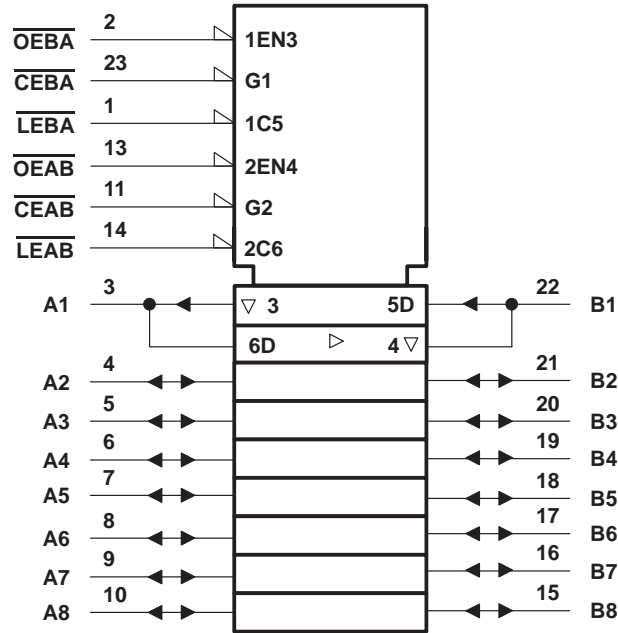
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .

‡ Output level before the indicated steady-state input conditions were established.

# SN74F543 OCTAL REGISTERED TRANSCIEVER WITH 3-STATE OUTPUTS

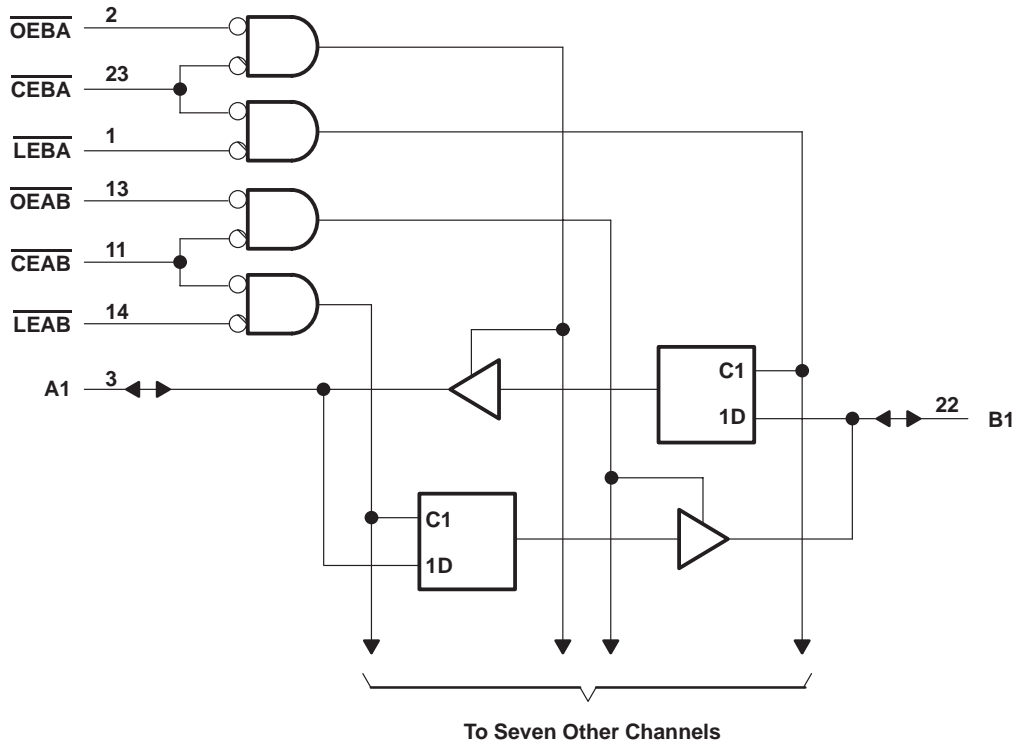
SDFS025B – D2942, MARCH 1987 – REVISED OCTOBER 1993

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



**SN74F543**  
**OCTAL REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SDFS025B – D2942, MARCH 1987 – REVISED OCTOBER 1993

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (excluding I/O ports) (see Note 1) .....	–1.2 V to 7 V
Input current range, $I_{IK}$ .....	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state .....	–0.5 V to 5.5 V
Voltage range applied to any output in the high state .....	–0.5 V to $V_{CC}$
Current into any output in the low state: A1–A8 .....	48 mA
B1–B8 .....	128 mA
Operating free-air temperature range .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			–18	mA
$I_{OH}$	High-level output current	A1–A8		–3	mA
		B1–B8		–15	
$I_{OL}$	Low-level output current	A1–A8		24	mA
		B1–B8		64	
$T_A$	Operating free-air temperature	0		70	°C



# SN74F543

## OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SDFS025B – D2942, MARCH 1987 – REVISED OCTOBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	A1–A8	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.5	3.4		V
			$I_{OH} = -3\text{ mA}$	2.4	3.3		
	B1–B8		$I_{OH} = -3\text{ mA}$	2.4	3.3		
			$I_{OH} = -15\text{ mA}$	2	3.1		
Any output		$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -1\text{ mA to } -3\text{ mA}$	2.7			
$V_{OL}$	A1–A8	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 24\text{ mA}$		0.3	0.5	V
	B1–B8		$I_{OL} = 64\text{ mA}$		0.42	0.55	
$I_I$	$\overline{OE}$ , $\overline{LE}$ , and $\overline{CE}$	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$			0.1	mA
	A and B ports		$V_I = 5.5\text{ V}$			1	
$I_{IH}‡$	$\overline{OE}$ , $\overline{LE}$ , and $\overline{CE}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
	A and B ports					70	
$I_{IL}‡$	$\overline{OE}$ , $\overline{LE}$ , and $\overline{CE}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-1.2	mA
	A and B ports					-0.65	
$I_{OS}§$	A1–A8	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$			-60	mA
	B1–B8					-100	
$I_{CCH}$		$V_{CC} = 5.5\text{ V}$			67	100	mA
$I_{CCL}$		$V_{CC} = 5.5\text{ V}$			83	125	mA
$I_{CCZ}$		$V_{CC} = 5.5\text{ V}$			83	125	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

### timing requirements

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $T_A = \text{MIN to MAX}¶$		UNIT
		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	5		5		ns
$t_{su}$	Setup time, data before latch enable		High or low	3	3.5	ns
$t_h$	Hold time, data after latch enable		High or low	3	3.5	ns

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN74F543**  
**OCTAL REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SDFS025B – D2942, MARCH 1987 – REVISED OCTOBER 1993

**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	2.2	5.1	7.5	2.2	8.5	ns
t <sub>PHL</sub>			2.2	4.6	6.5	2.2	7.5	
t <sub>PLH</sub>	$\overline{LEBA}$	A	3.7	8.1	11	4.1	12.5	ns
t <sub>PHL</sub>			3.7	8.1	11	4.1	12.5	
t <sub>PLH</sub>	$\overline{LEAB}$	B	3.7	8.1	11	4.1	12.5	ns
t <sub>PHL</sub>			3.7	8.1	11	4.1	12.5	
t <sub>PZH</sub>	$\overline{OE}$ or $\overline{CE}$	A or B	2.2	6.6	9	2.2	10	ns
t <sub>PZL</sub>			3.2	7.1	10.5	3.2	12	
t <sub>PHZ</sub>	$\overline{OE}$ or $\overline{CE}$	A or B	1.7	5.6	8	1.7	9	ns
t <sub>PLZ</sub>			1.7	5.1	7.5	1.7	8.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74F543DBR</a>	Active	Production	SSOP (DB)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543
SN74F543DBR.A	Active	Production	SSOP (DB)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543
<a href="#">SN74F543DW</a>	Obsolete	Production	SOIC (DW)   24	-	-	Call TI	Call TI	0 to 70	F543
<a href="#">SN74F543DWR</a>	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543
SN74F543DWR.A	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F543DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74F543DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F543DBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74F543DWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated