Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## <sup>l</sup>description

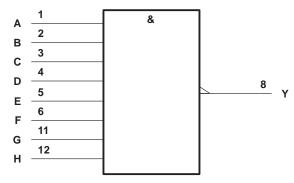
These devices contain a single 8-input NAND gate. They perform the Boolean functions  $Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D} \bullet \overline{E} \bullet \overline{F} \bullet \overline{G} \bullet \overline{H} \text{ or } Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} \text{ in positive logic.}$ 

The SN54F30 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74F30 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE** 

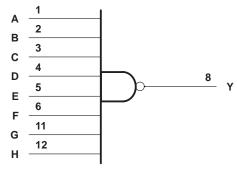
INPUTS A-H	OUTPUT Y
All inputs H	L
One or more inputs L	Н

## logic symbol†

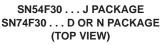


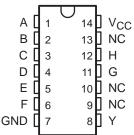
 $<sup>\</sup>ensuremath{^{\dagger}}$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

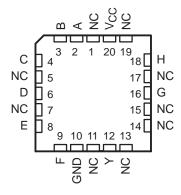


Pin numbers shown are for the D, J, and N packages.





SN54F30 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	$\dots$ $-0.5$ V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	$\dots$ $-1.2\ V$ to 7 $V$
Input current range	-30 mA to 5 mA
Voltage range applied to any output in the high state	$-0.5 \text{ V to V}_{CC}$
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F30	−55°C to 125°C
SN74F30	$0^{\circ}$ C to $70^{\circ}$ C
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54F30			9	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ΙΙΚ	Input clamp current			-18			-18	mA
ІОН	High-level output current			- 1			- 1	mA
l <sub>OL</sub>	Low-level output current			20			20	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEG	TEST CONDITIONS				5	UNIT		
PARAMETER	153	or CONDITIONS	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
Vari	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		V
VOH	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -1 \text{ mA}$				2.7			V
$V_{OL}$	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 20 \text{ mA}$		0.3	0.5		0.3	0.5	V
lj	$V_{CC} = 5.5 \text{ V},$	$V_I = 7 V$			0.1			0.1	mA
lіН	$V_{CC} = 5.5 \text{ V},$	$V_{I} = 2.7 V$			20			20	μΑ
I <sub>IL</sub>	$V_{CC} = 5.5 \text{ V},$	$V_{I} = 0.5 V$			- 0.6			- 0.6	mA
l <sub>OS</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-60		-150	-60		-150	mA
ICCH	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0		0.7	1.5		0.7	1.5	mA
ICCL	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 4.5 V		2.2	4		2.2	4	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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## switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>I</sub> R <sub>I</sub>	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$			$V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX <sup>†</sup> SN54F30 SN74F30			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A thru H		1	3.1	5	1	6	1	5.5	ne
<sup>t</sup> PHL	Aullun	'	1	2.6	4.5	1	6	1	5	ns

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.

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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-88708012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88708012A SNJ54F 30FK
5962-8870801CA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870801CA SNJ54F30J
5962-8870801DA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870801DA SNJ54F30W
SN54F30J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54F30J
SN54F30J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54F30J
SN74F30D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	F30
SN74F30DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F30
SN74F30DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F30
SN74F30N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F30N
SN74F30N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F30N
SN74F30NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F30
SN74F30NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F30
SNJ54F30FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88708012A SNJ54F 30FK
SNJ54F30FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88708012A SNJ54F 30FK
SNJ54F30J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870801CA SNJ54F30J
SNJ54F30J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870801CA SNJ54F30J
SNJ54F30W	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870801DA SNJ54F30W
SNJ54F30W.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870801DA SNJ54F30W

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- (1) Status: For more details on status, see our product life cycle.
- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54F30, SN74F30:

Catalog: SN74F30

Military: SN54F30

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F30DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74F30NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F30DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74F30NSR	SOP	NS	14	2000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-88708012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8870801DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74F30N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F30N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F30N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74F30N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54F30FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F30FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F30W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54F30W.A	W	CFP	14	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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