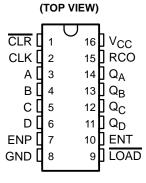
D. DB. OR N PACKAGE

SDFS056B - MARCH 1987 - REVISED AUGUST 2001

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for N-Bit Cascading
- Fully Synchronous Operation for Counting

description

This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when



so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load (LOAD) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is asynchronous, and a low logic level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs to low, regardless of the levels of CLK, $\overline{\text{LOAD}}$, ENP, and ENT.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F161A features a fully independent clock circuit. Changes at ENP, ENT, or $\overline{\text{LOAD}}$ that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	PDIP – N	Tube	SN74F161AN	SN74F161AN		
0°C to 70°C	SOIC - D	Tube	SN74F161AD	F161A		
0-0 10 70-0	30IC = D	Tape and reel	SN74F161ADR	FIOTA		
	SSOP – DB	Tape and reel	SN74F161ADBR	F161A		

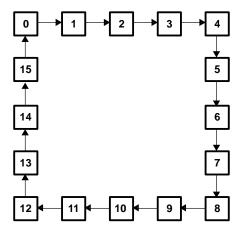
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



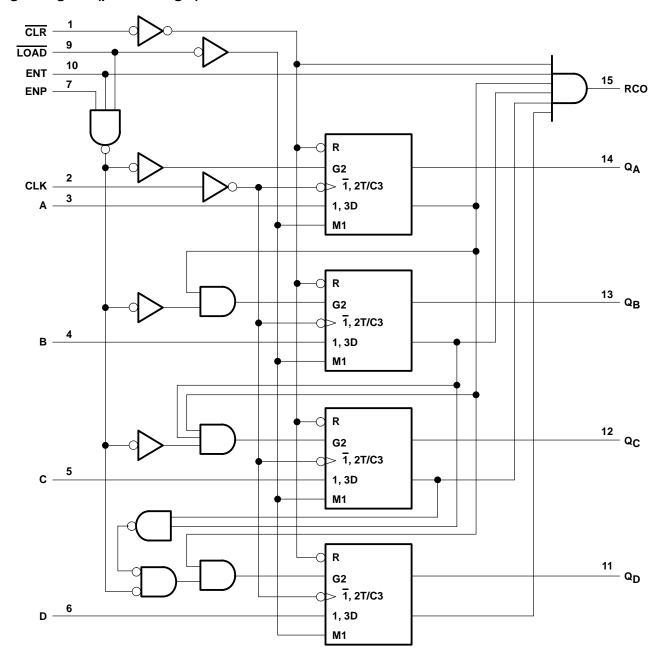
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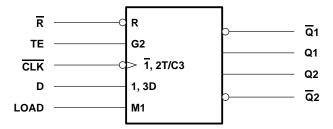
state diagram



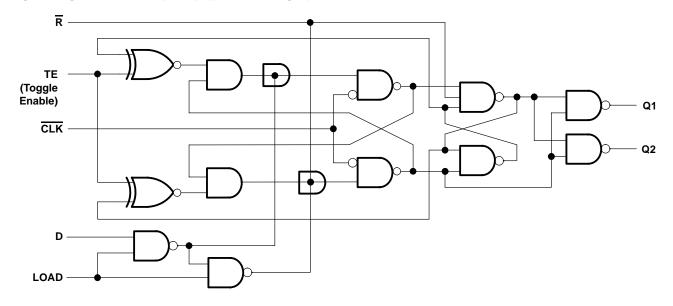
logic diagram (positive logic)



logic symbol, each flip-flop



logic diagram, each flip-flop (positive logic)

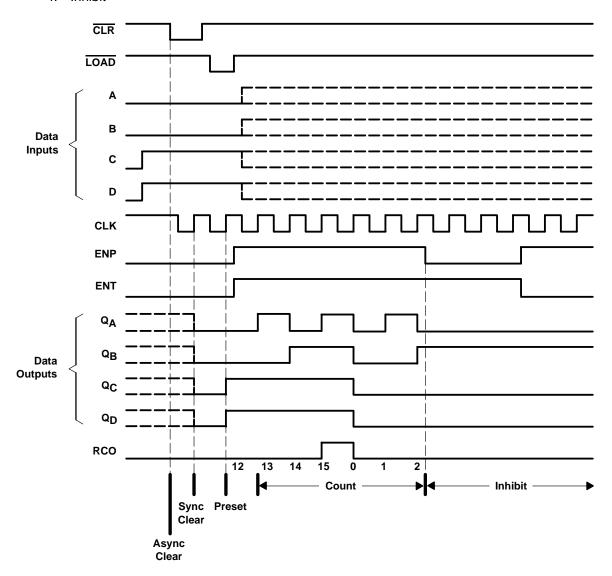




typical clear, preset, count, and inhibit sequences

The following timing sequence is illustrated below:

- 1. Clear outputs to zero
- 2. Preset to binary 12
- 3. Count to 13, 14, 15, 0, 1, and 2
- 4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		\dots -0.5 V to 7 V
Input voltage range, V _I (see Note 1)		\dots -1.2 V to 7 V
Input current range		-30 mA to 5 mA
Voltage range applied to any output in the high	state	\dots -0.5 V to V _{CC}
Current into any output in the low state		40 mA
Package thermal impedance, θ_{JA} (see Note 2):	: D package	73°C/W
•	DB package	82°C/W
	N package	67°C/W
Storage temperature range, T _{sta}		. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
l _{IK}	Input clamp current			-18	mA
ЮН	High-level output current			-1	mA
lOL	Low-level output current			20	mA
TA	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TE	TEST CONDITIONS				
٧ıK		$V_{CC} = 4.5 \text{ V},$	$I_{ } = -18 \text{ mA}$			-1.2	V
V		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.5	3.4		V
VOH		$V_{CC} = 4.75 V$,	$I_{OH} = -1 \text{ mA}$	2.7			V
V _{OL}		$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.3	0.5	V
I _I		V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
Ι _{ΙΗ}		V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
	ENP, CLK, A, B, C, D					- 0.6	
I _{IL}	ENT, LOAD	V _{CC} = 5.5 V,	$V_{ } = 0.5 V$			- 1.2	mA
	CLR					- 0.6	
los§		$V_{CC} = 5.5 V$,	V _O = 0	-60		-150	mA
Icc		V _{CC} = 5.5 V			37	55	mA

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} =	= 5 V, 25°C	MIN	MAX	UNIT	
				MIN	MAX				
fclock	Clock frequency			0	100	0	90	MHz	
		CLK high or low (loading)		5		5			
.	Pulse duration	CLK (counting)	High	4		4		ne	
t _W	ruise duration	CER (Counting)	Low	6		7		ns	
		CLR low	5		5				
		Data before CLK↑	High or low	5		5			
		LOAD before CLK↑	High	11		11.5			
t _{su}	Setup time	LOAD before CLK	Low	8.5		9.5		ns	
		ENP and ENT before CLK↑	High	11		11.5			
		ENF and ENT before CERT	Low	5		5			
		Data after CLK↑	High or low	2		2			
.	Hold time	LOAD after CLK↑	High	2		2		ne	
^t h	i ioiu liitie	LOAD after CLK	Low	0		0		ns	
		ENP and ENT after CLK↑	High or low	0		0			
t _{su}	Inactive-state setup time, C	LR high before CLK↑†		6		6		ns	

[†] Inactive-state setup time also is referred to as recovery time.

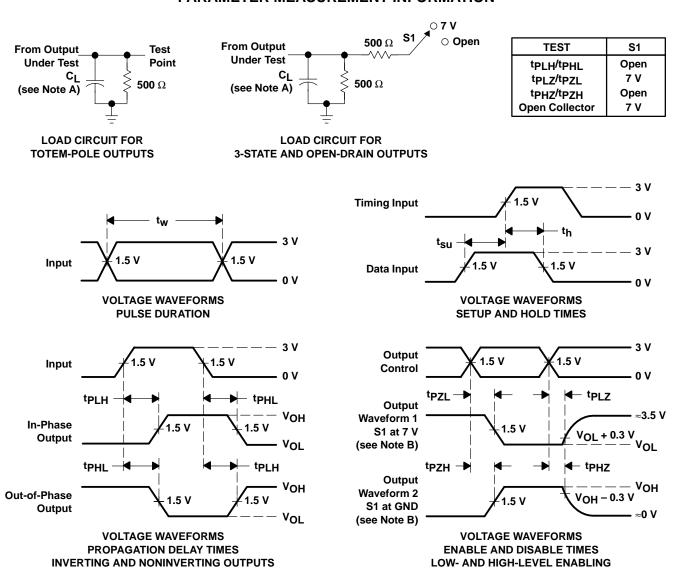
switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L	CC = 5 \ _ = 50 P _ = 500 \ _ = 25°C	F, 2,	V _{CC} = 4.5 V C _L = 50 R _L = 50 T _A = MIN TC	UNIT		
			MIN	TYP	MAX	MIN	MAX		
f _{max}			100	120		90		MHz	
^t PLH	OLK (LOAD bimb)	A=O	2.7	5.1	7.5	2.7	8.5	20	
^t PHL	CLK (LOAD high)	Any Q	2.7	7.1	10	2.7	11	ns	
^t PLH	OLK (1.OAB ()	A O	3.2	5.6	8.5	3.2	9.5		
^t PHL	CLK (LOAD low)	Any Q	3.2	5.6	8.5	3.2	9.5	ns	
^t PLH	CLK	DCO	4.2	9.6	14	4.2	15	20	
^t PHL	CLN	RCO	4.2	9.6	14	4.2	15	ns	
^t PLH	CNIT	DCO	1.7	4.1	7.5	1.7	8.5	20	
^t PHL	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns	
4	OL D	Any Q	4.7	8.6	12	4.7	13		
^t PHL	CLR	RCO	3.7	7.6	10.5	3.7	11.5	ns	

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 4: Load circuits and waveforms are shown in Figure 1.



PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$, duty cycle = 50%.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74F161AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	0 to 70	F161A
SN74F161ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F161A
SN74F161ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F161A
SN74F161AN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F161AN
SN74F161AN.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F161AN
SN74F161ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F161A
SN74F161ANSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F161A

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 31-Oct-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74F161ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F161ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74F161ANSR	SOP	NS	16	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74F161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F161AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F161AN.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOP



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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